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HANDBOOK OF MODELING FOR CIRCUIT ANALYSIS INCLUDING RADIATION EFFECTS

R. Simon

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Final Report

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This technical report has been reviewed and is approved for publication.

Robert G. Simon

ROBERT SIMON
Project Officer

FOR THE COMMANDER

Gerald P. Chapman

GERALD P. CHAPMAN
Major, USAF
Chief, Transient Radiation Effects Br

Donald A. Dowler

DONALD A. DOWLER
Colonel, USAF
Chief, Electromagnetics Division

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This handbook is a compilation and organization of previous research in computer modeling of semiconductor devices. It is designed to serve as a reference for the analyst who must analyze the effects of nuclear radiation on electronic circuits. It uses a modular approach wherein the analyst uses the simplest model which will yield the desired accuracy. The latest technology in representing second order effects is included in the handbook. The organization of the handbook proceeds from diodes to transistors, MOSFETs, IFETs,

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20. ABSTRACT (Continued)

SCRs, UJTs, transformers and integrated circuits. The final chapter presents examples of computer aided analyses.

PREFACE

This handbook was prepared by The BDM Corporation, 2600 Yale Blvd., SE, Albuquerque, New Mexico 87106, for the Air Force Weapons Laboratory (ELP), Kirtland Air Force Base, New Mexico, under contract F26601-77-C-0026. The BDM authors were P. A. Young, D. R. Alexander, and R. J. Antinone. Mr. Robert G. Simon (ELP) was the AFWL Project Officer. Although the handbook is a result of an Air Force contract, it was recommended and funded by The Defense Nuclear Agency.

The emphasis on radiation effects inclusive models reflects the long-term support of The Defense Nuclear Agency in providing analytical and design tools for nuclear hardened DOD systems.

The Bipolar Transistor chapter was based largely on I. Getreu's *Modeling The Bipolar Transistor*. The UJT and JFET models were taken from J. C. Bowers and S. R. Sedore's *SCEPTRE: A Computer Program for Circuit and System Analysis*. Many other less extensively used sources are listed as references at the end of appropriate chapters.

This handbook is the culmination of several years' effort by many persons and organizations in modeling of semiconductor circuits for computer-aided analysis of radiation effects. It has been prepared as a result of conferences with many analysts which revealed the need for a single authoritative reference in the techniques for modeling various circuit elements. This handbook is not a listing of models by device type; rather it illustrates the path to be followed in generating models of the necessary complexity for the particular analysis at hand.

The handbook is published in loose-leaf binder format to facilitate adding new material as it becomes available. The handbook compliments and should be used in conjunction with the TREE (Transient Radiation Effects on Electronics) Handbook, DNA 1420H, and the TREE Preferred Procedures, DNA 2028H.

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CHAPTER I
INTRODUCTION

CHAPTER I

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CHAPTER I
INTRODUCTION

A. OVERVIEW

The purpose of this modeling handbook is to provide an organized approach to the application of radiation effect inclusive semiconductor models to problems requiring computer aided circuit analysis and design. Over the past 10 to 15 years, several investigators have made significant progress in developing computer oriented models for the different semiconductor technologies. These models incorporate improved representations of both electrical effects and radiation effects. They are documented in several excellent technical reports which give detailed discussion of derivation and application procedures. Unfortunately, many of these reports are not readily available to analysts who wish to apply the models to a specific problem. Even if the analyst has access to the reports, he is often confronted with the rather formidable task of wading through the derivation in order to sift out the application information for the model. This is especially distressing to the inexperienced analyst who may waste valuable time struggling with material which is not germane to his problem.

The intent of this handbook is to alleviate the two problems identified above. First, it presents the results of several model development programs in a single volume. Hopefully, this will be effective in dispersing the results of these programs to a much broader community of users than has previously been possible. No new or original material is presented in this document. Therefore, the analyst who feels that additional information is required can check the references indicated throughout the handbook. In general, the authors of these references have expended considerable effort in giving the details of the model development. The omission of these derivations from this handbook simply reflects the limitations inherent in such a document, and does not imply that they are not important. Investigators wishing to extend the capabilities of any

model are encouraged to consult the original documentation rather than relying on the abbreviated material presented in the handbook.

The second intent of this modeling handbook is to provide an organized structure for the application of the various models. This structure is the only original contribution of the handbook's authors. The reader should note that this document is not designed to be read sequentially. Only chapter I, the introduction, will be of general interest to all readers. The remainder of the chapters are meant to be stand-alone sections which are oriented toward specific technologies and their models. A brief examination of the table of contents will demonstrate the basic structure of the handbook organization. Note that the first few chapters are organized by technology. These include chapters on bipolar diode models, bipolar transistor models, MOS models, and miscellaneous device technologies (SCR, transformer, UJT, JFET). They are followed by a chapter on simplified modeling of analog and digital integrated circuits. The simplified IC modeling techniques are applicable to either bipolar or MOS technologies. The final chapter presents specific example problems and the modeling techniques used in their solution. The general trend of the modeling handbook is from specific device models toward more general IC and subsystem models.

Within each individual chapter the organization proceeds from the basic, first order electrical model toward the more extensive models incorporating radiation effects and second order electrical effects. Division within the chapters is made according to physical phenomena whenever possible. The analyst who requires only a gross electrical representation of a particular device to solve a problem need only consult the first section of the appropriate chapter. If greater sophistication in the model is required, subsequent sections must be consulted.

An attempt has been made to apply a parallel structure in each chapter section. This is accomplished by developing eight major subsection headings. These include:

(1) Description

(2) Advantages

(3) Cautions

(4) Characteristics

(5) Defining Equations

(6) Parameter List

(7) Parameterization

    (a) Definition

    (b) Typical Value

    (c) Measurement

    (d) Example (measurement & specification sheet)

(8) Computer Example

The description subsection provides a qualitative discussion of the electrical or radiation effect to be discussed. The modeling handbook is not meant to be a treatise on semiconductor physics. However, the variations in model characteristics must be understood in terms of the physical properties they are attempting to represent. The description subsection is intended to provide the physical context of the model without a detailed derivation. Appropriate references are given to technical publications dealing with the underlying physical phenomena.

The advantages subsection presents the primary reasons for application of the model to be discussed. For some physical phenomena such as reverse breakdown, there are multiple modeling techniques which may be implemented. In such cases, the merits of the different approaches are discussed in terms of their effect on desired results. There should always be some reason for the analyst's choice of a specific modeling approach. Hopefully, a clear statement of advantages will help to direct that choice.

Every model has a definite range of applicability which the analyst must be careful not to exceed. Knowledge of model limitations is especially important in computer aided design. In general, the computer can be relied on to perform calculations accurately; however, the analyst has total responsibility for thinking. The cautions subsection has been included to remind the analyst of the limitations of each model and to encourage him to think about how these limitations may affect the results.

The characteristics subsection includes a schematic of the model topology and a qualitative representation of the electrical response of the model. The topology includes elements and polarities required for proper implementation of the model. The electrical representation may take the form of an I/V plot, a voltage versus time plot, or a current versus time plot. The unique qualities of the model response are highlighted for emphasis. These diagrams are useful in orienting the analyst to the mathematical description of the model elements in the following subsection.

The defining equations subsection presents the mathematical description of the effect being modeled. The equations are presented without proof or derivation. Their purpose is to demonstrate the relationship of the various model parameters in a format which is familiar to engineers. Implementation of the equations in a computer code often obscures the parameteric relationship due to the necessity for eliminating singularities and other numerical difficulties.

The parameter list immediately follows the defining equations. It provides a definition for all key parameters and gives the nomenclature to be used in subsequent references. Care has been taken to insure that a clear, consistent nomenclature has been used throughout the handbook. Whenever possible, this nomenclature is consistent with the nomenclature in the technical literature.

The parameterization subsection presents techniques for assigning numerical values to each parameter used in the model. The predictions or simulations based on a model will never be more accurate than the data used to parameterize the model. Thus, there is no reason to select an elegant model if there is insufficient data available for the selection of parameter values. Each parameter included in the parameterization list is precisely defined and a typical value is given. The typical value serves the purpose of allowing the analyst to get a model running on the computer with parameters that bear some relationship to reality. It also gives him a frame of reference for judging the numerical values which he derives from measured or specification sheet data. Specific

measurement schemes and data reduction procedures are recommended for each parameter and schematic diagrams are given for equipment arrangement. Numerical examples are provided for determining the parameter value from measurements and from specification sheet data. Actual photographs of device response or tabularized data from the measurement scheme are provided and reduced to the final parameter quantity. Specification sheets are included and appropriate entries are selected for parameter estimates. A comparison of the numerical values derived from measurement and from the specification sheet gives the analyst an indication of the relative accuracy of the different parameterization sources.

A code implementation subsection is included in each chapter to provide the analyst with information on how the basic mathematical formulation of the model must be modified for incorporation in a computer aided circuit analysis and design (CAD) code. Five different CAD codes have been considered in this subsection, including SCEPTRE, NET-2, SPICE2, TRAC, and CIRCUS. The last four of these codes have "built-in" models which may be parameterized in various ways to yield different levels of model complexity. Unfortunately, the same nomenclature has not been used in each of the codes. This tends to obscure the basic similarities in the model capabilities. To key the different code models to the nomenclature and model levels addressed in the handbook, a table is provided which gives the entire parameter list for each model from the five codes and which indicates those parameters to be parameterized and those to be defaulted. Thus, if the analyst wishes to use the first order MOS electrical model described in this handbook with the NET-2 code, table IV-2 will demonstrate how he should encode the NET-2 parameter list.

The code implementation subsection also provides notes on the effect of code implementation on the model characteristics. The necessity for avoiding singularities and other numerical problems has been noted earlier. Eliminating these problems is often done by altering their functional forms. These altered functions may give results which are slightly

different from those expected by the analyst in certain operating regions. These modifications and their implications are called out as notes in this subsection.

The computer example is the final subsection in each of the modeling sections. Its purpose is to demonstrate the model characteristics developed in the preceding material. Emphasis is placed on using very simple circuits which exercise an individual component model. Often "curve tracer" programs are used to demonstrate that the modeled performance is indeed similar to that desired and anticipated from the parameterization procedure. This feedback from the computer to the analyst is an essential verification of model operation which should always be required before incorporating the model in a more complex circuit.

The organization of the modeling sections discussed above is quite modular. Hopefully, this approach will facilitate the use of the handbook by both the novice and the expert. The novice should be able to identify the type of effect he wishes to represent and follow an orderly procedure for selecting, parameterizing, and implementing an appropriate model on the code available to him. The expert should be able to use the handbook as a quick reference to refresh his memory on limitations of various models or to review model conversion procedures from one code to another. The intent of the handbook authors was to accurately reproduce the developments made by several investigators in the field of semiconductor modeling in an organizational format which will facilitate the application of their results.

B. APPLICATION RECOMMENDATIONS

Modern computer aided circuit analysis and design codes and the models which have been developed for use with them can be extremely powerful and versatile tools for the investigation of radiation effects on devices, circuits, and subsystems. However, their proper application requires attention to some general guidelines if their results are to be valid and economically justifiable. A list of such guidelines undoubtedly

would vary considerably if compiled by different authors, but hopefully the list of statements and discussion offered below incorporates the most important aspects of computer model usage.

(1) Determine why you are making a computer aided circuit analysis.

(2) Select an appropriate model.

(3) Know the difference between simulation and prediction.

(4) Know the limitations of parameterization data.

(5) Verify the models.

(6) Understand the results.

Computer aided circuit analysis is expensive in terms of model parameterization measurements, analyst's time, and computer rental. It should be viewed as one of several alternative tools available for examination of radiation effects on devices, circuits, or subsystems. Often, sound engineering analysis procedures can be applied with justifiable, simplifying assumptions to yield results which are as valid as any computer generated solution. A healthy initial response to any analysis requirement is to examine ways to avoid computer aided analysis. However, there is a significant class of problems which defy reasonable manual analysis techniques. In these problems, the variables of elements may be closely coupled such that several responses must be considered simultaneously. In such cases, the expanded recordkeeping ability of the computer is essential to the analysis. Also included in the class of problems requiring CAD tools are those which contain highly nonlinear elements or elements which are driven into nonlinear modes by radiation exposure. Certainly, an exhaustive list of problems requiring CAD and modeling tools would consume more space than is available here. The point to be made is that, although such a list is extensive, it is a definite subset of all radiation effect problems. An analysis should never be performed "just to see how the circuit works." The results of such an analysis are almost certain to be misleading and will undoubtedly be expensive.

Closely associated with the determination of the rationale for computer aided analysis is the requirement for selecting an appropriate model. Never select a sophisticated model when a simple model will

suffice. To assist in selecting an appropriate model, the analyst should force himself to make quantitative answers to questions such as:

(1) What is the range of operating characteristics which the model must represent?

(2) What accuracy is acceptable?

(3) Are the time constants of the model comparable to those of the circuit?

(4) Is the device a switch or an amplifier in this application?

Numerous other questions might be added to the list, but the point is that the analyst must make a definite series of decisions in selecting a model. Good scientific procedure suggests that these decisions be as quantitative as possible and that they be documented. Selecting a model which covers several decades of current characteristics, when only a single point on the operating characteristic is required, is wasteful of paramterization time, analysis effort, and computer time. Furthermore, it is likely to introduce errors which could have been avoided with a less sophisticated model. The analyst is cautioned to consider that the model may be driven over a wider range of operating characteristics in a radiation simulation than that experienced under normal operating conditions.

Once the decision has been reached that a computer aided analysis is required and a model has been selected, the analyst should know whether he is making a simulation or a prediction. The distinction between the two is vital for the interpretation of the results. All models represent simulations at some level of response. For example, if a transistor model is parameterized from curve tracer measurements, then it can only be expected to simulate those measurements when exercised by the computer analysis code. This model can never be correctly said to "predict" transistor performance. A number of simulation type transistor models can be combined to predict a circuit response. However, that prediction will only be valid so long as the simulations of the transistors are appropriate for their operating conditions. One of the most frequent and potentially disasterous mistakes made in computer aided circuit analysis

is the inadvertent extrapolation of models beyond their range of simulation validity. These mistakes are insidious because the computer code will continue to generate results despite their lack of validity; only the continued attention of the analyst can prevent this error.

As noted earlier, models can only be as accurate as the data which go into their parameterization. However, the analyst is advised to consider the validity of the data with respect to the goals of his analysis. Specification sheet data represent the minimum guaranteed electrical specifications which the manufacturer will attribute to a given product line. A few manufacturers assign those data values based on 3σ points of measured parameter distributions. Unfortunately, most do not have a quantifiable procedure for setting specifications. In either event, the values may not be consistent when applied to any given device. The specification sheet data are important from the standpoint of representing the data which the design engineer utilized in designing the circuit. On the other hand, measured data reflect the actual characteristics of a device and all the data are consistent. However, they represent only a single device/characteristics set in a distribution of devices of that type. Depending on where that device lies in the distribution, analysis results based on its model parameters may be conservative or nonconservative. For analyses which are supposed to reflect the performance of a statistically significant set of circuits, the analyst should make some effort to establish the sensitivity of the results to variations in key model parameters. This should be done prior to the interpretation of the results.

Probably more time is wasted in attempting to debug models in the analysis circuit than in any other aspect of computer aided analysis. No model should ever be included in the circuit to be analyzed before its operation has been verified. In this handbook, several examples are given for curve tracer and simple pulse circuits which can be used to verify the anticipated operation of individual models. These simple

programs provide inexpensive vehicles for identifying model problems outside of the circuit to be analyzed. Time or expense spent in model verification is never wasted.

The final check on the results of all computer aided analysis should be, "Does the result make sense?" There is no foreseeable substitute for human understanding in the application of CAD results. The analyst's final responsibility is to exercise his own reasoning ability. Computer codes can produce errors as a result of numerical difficulties or they can simply "step over" an important part of the response (e.g., a photocurrent pulse) through an inappropriate selection of a time step. The analyst who understands the circuit is the last line of defense against such errors.

CHAPTER II
DIODES

CHAPTER II

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CHAPTER II
DIODES

A. INTRODUCTION

An understanding of diode modeling is fundamental to the task of modeling any semiconductor device. This is particularly true in the context of the modeling handbook since techniques for modeling radiation effects and other phenomenon are described in the greatest detail in chapter II.

An "expandable model" format is applied in this chapter. This format supports a basic rule in modeling which is, "use the simplest model possible." The expandable model format allows a range of complexity from the diode equation produced from a data sheet to diode models which simulate I-V behavior over many decades of current.

Techniques for obtaining model parameters from both terminal measurements and specification sheets are included. Terminal measurements will produce accurate parameter values for specific devices but indicate nothing about the distribution of device parameters unless numerous devices are tested. The manufacturer's specification sheets yield parameter values which are often very inaccurate, yet they place bounds on parameter variations which may be used for best or worst case analysis.

Some terminal measurements suggested by the modeling handbook must be regarded as useful only in the absence of better information. One example of this is the terminal estimation technique used to obtain background doping. The assumptions made were a planar, one-sided, abrupt junction. Because no junction is truly planar, the electric field at the curved portions of the junction will cause the junction to avalanche at a lower voltage than predicted. No diffused junction is truly abrupt, which implies that the term "background doping" loses some or all of its meaning in many devices. The point to be made is that the analyst should try to be aware of how the model attempts to simulate the physical processes of the device, the simplifications and assumptions made, and the

accuracy and limitations of the model chosen. It is for this reason that discussions of the physical processes are often included. An understanding of device physics is desirable but certainly not required for the modeling process.

When working with different computer codes, one often finds different sets of units being applied by the code. For example, resistance may normally be specified in ohms for one code and kilohms for another code. As a general rule, any self-consistent set of units may be used. A problem occurs with the default values and built-in models of circuit analysis codes. Therefore, it is safer to work in the units specified by each computer code.

Because of the overwhelming scope of semiconductor device modeling, many concepts, approaches, and models could not be addressed. It is for this reason that a bibliography is included at the end of this handbook. References which proved useful in the development of chapters are included at the end of each chapter.

B. DIODE MODELING

1. Diode Equation

a. Description

The foundation of all diode models is the diode equation which relates the diode current to diode voltage and may be written in its simplest form as:

$$I_D = I_S\left[\exp\left(\frac{qV_D}{KT}\right) - 1\right]$$

b. Advantages

The diode equation is implemented in almost all network simulation codes and is the simplest method for implementing a diode characteristic with a minimum number of elements. Specification sheet data may be used to parameterize the diode equation. The diode equation

requires only one measured parameter and an assumed temperature to define the parameters.

c. Cautions

The basic diode equation gives the gross, first order I/V characteristic. In circuits where the details of the diode response are important to proper operation, additional model elements must be included to simulate second order and radiation effects. The nature of these additional elements is discussed in the following sections.

d. Characteristics

The symbolic representation of the diode equation is shown in figure II-1.

The diode equation will produce the electrical characteristic shown in figure II-2.

e. Defining Equation

The diode equation is implemented as a voltage controlled current source defined by:

$$I_D = I_S \left[\exp\left(\frac{qV_D}{KT}\right) - 1 \right]$$

f. Parameter List

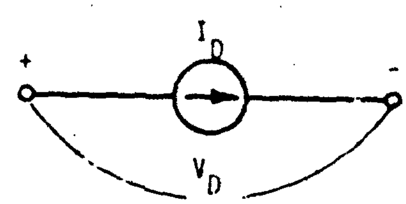
I_D = the diode current
I_S = the diode saturation current
q = the magnitude of electronic charge (1.6×10^{-19} coulomb)
V_D = the voltage across element I_D
K = Boltzmann's constant (8.62×10^{-5} eV/°K)
T = the junction temperature in °K

g. Parameterization

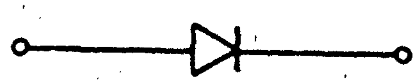
1) I_S

a) Definition

I_S is the reverse saturation current of the diode. In an ideal diode, the reverse current of a diode under several

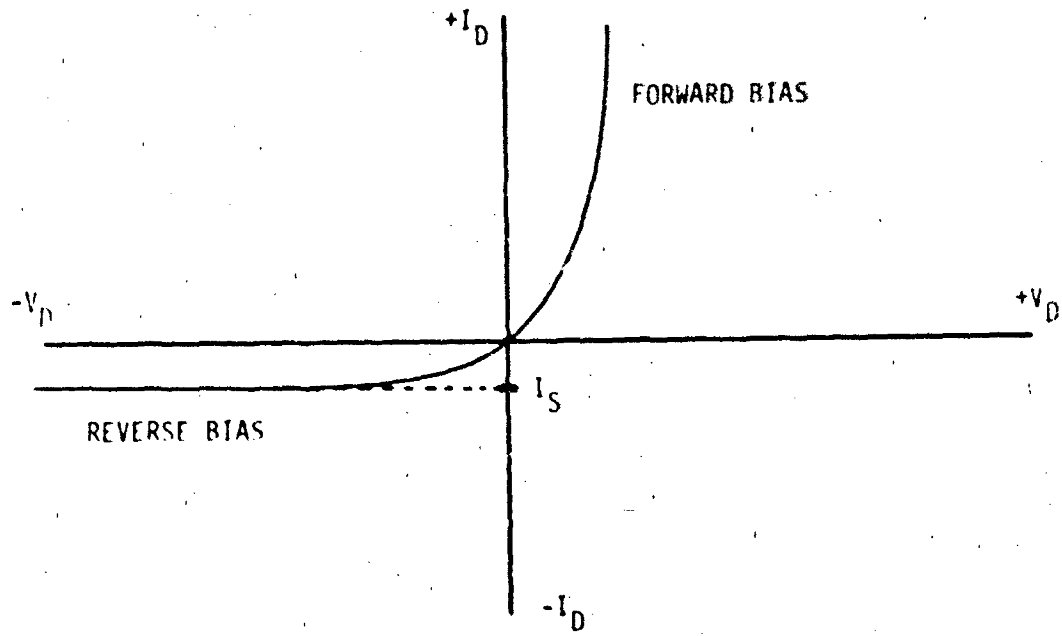


(a) Model Representation

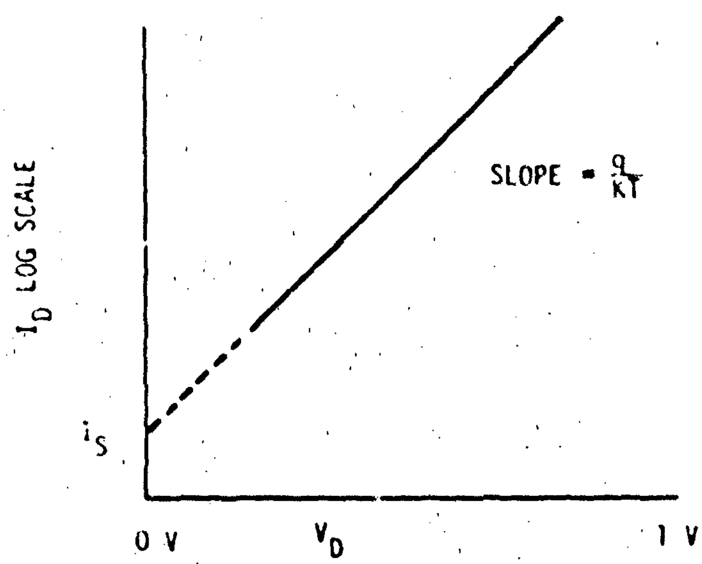


(b) Component Representation

Figure II-1. Symbolic Representation of the Diode Equation



(a) Linear Scale



(b) Semilogarathmic Plot

Figure II-2. Diode Characteristics

volts reverse bias would approach I_S. For real diodes, however, leakage and charge generation effects dominate the reverse current so I_S may not be obtained from reverse current measurements. I_S is obtained from the behavior of the diode in the forward operating region.

b) Typical Values

A value of 10^{-12} amperes is typical. I_S is directly proportional to the active junction area and may vary significantly between device types. A range of 10^{-5} to 10^{-17} amperes is common.

c) Measurement

I_S can be computed from the value of V_D and I_D at a forward biased operating point. It should be noted that only the I-V point will be accurately simulated, therefore, the I-V point chosen should be made near the operating point of the diode in the circuit. I_S can then be found from the relationship:

$$I_S = \frac{I_D}{\exp\left(\frac{qV_D}{KT}\right) - 1}$$

d) Example - 1N914

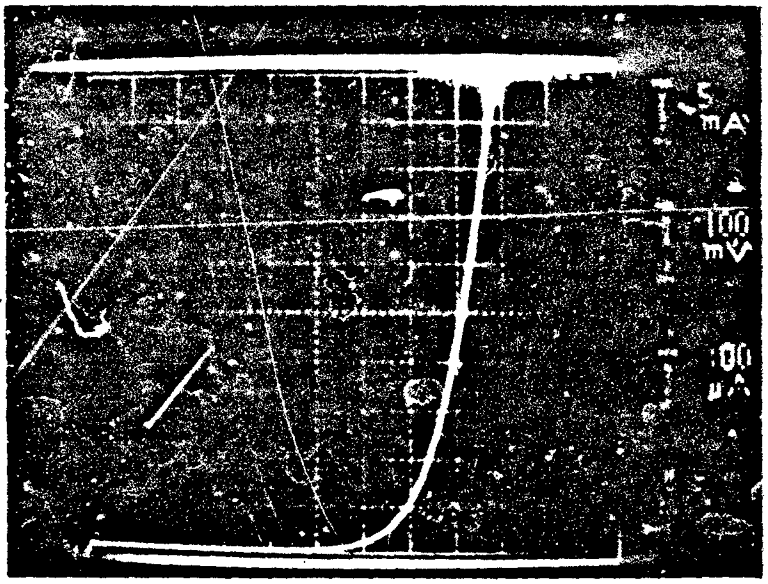
1 From Measurement

The point chosen in forward bias to be modeled was 5 mA. From the photographs shown in figure II-3, the diode voltage at 5 mA can be seen to be 690 mV. I_S was then computed at 300°K to be:

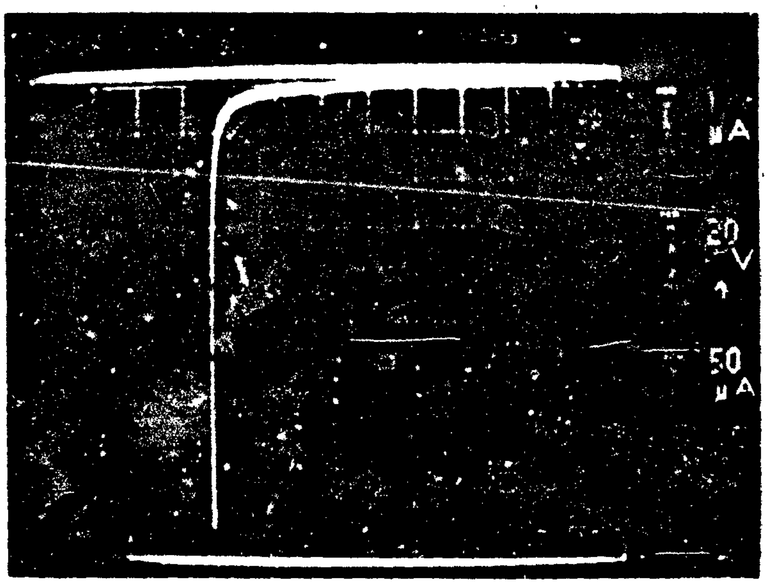
$$I_S = \frac{5\ \text{mA}}{\exp\left(\frac{0.69\ \text{V}}{0.0259\ \text{V}}\right) - 1} = 1.35 \times 10^{-14}\ \text{amperes}$$

2 From Data Sheets

An estimate of I_S can be made from specification sheet data. The specification sheet shown in figure II-4 lists a diode voltage of 0.72 V at a forward current of 5 mA.



(a) 1N914 Forward Characteristics



(b) IN914 Reverse Characteristics

Figure II-3. 1N914 Forward and Reverse Characteristics

TYPES 1N914, 1N914A, 1N914B, 1N915, 1N916, 1N916A, 1N916B and 1N917
DIFFUSED SILICON SWITCHING DIODES

maximum electrical characteristics at 25°C ambient temperature (unless otherwise noted)

		1N914	1N914A	1N914B	1N915	1N916	1N916A	1N916B	1N917	Unit
BV_R	Min Breakdown Voltage at 100 μa	100	100	100	65	100	100	100	40	v
I_R	Reverse Current at V_R	5	5	5	5	5	5	5		μa
I_R	Reverse Current at −20 v	0.025	0.025	0.025		0.025	0.025	0.025		μa
I_R	Reverse Current at −20 v at 100°C	3	3	3	5	3	3	3	25	μa
I_R	Reverse Current at −20 v at 150°C	50	50	50		50	50	50		μa
I_R	Reverse Current at −10 v				0.025				0.05	μa
I_R	Reverse Current at −10 v at 125°C									μa
I_F	Min Fwd Current at V_F = 1 v	10	20	100	50	10	20	30	10	ma
V_F	at 250 μa								0.64	v
V_F	at 1.5 ma								0.74	v
V_F	at 3.5 ma								0.83	v
V_F	at 5 ma			0.72	0.73			0.73		v
V_F	Min at 5 ma				0.60					v
C	Capacitance at V_R = 0	4	4	4	4	2	2	2	2.5	pf

maximum operating characteristics at 25°C ambient temperature (unless otherwise noted)

		1N914	1N914A	1N914B	1N915	1N916	1N916A	1N916B	1N917	Unit
t_{rr}	Reverse Recovery Time	**4 *8	**4 *8	**4 *8	*10	**4 *8	**4 *8	**4 *8	*3	nsec nsec
V_f	Fwd Recovery Voltage (50 ma Peak Sq. wave, 0.1 μsec pulse width, 10 nsec rise time, 5 kc to 100 kc rep. rate)	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	v

* Lumatron (10 ma I_F, 10 ma I_R, recover to 1 ma)
** EG&G (10 ma I_F, 6 v V_R, recover to 1 ma)

Figure II-4. 1N914 Manufacturer Specification Sheet (ref. II-1)

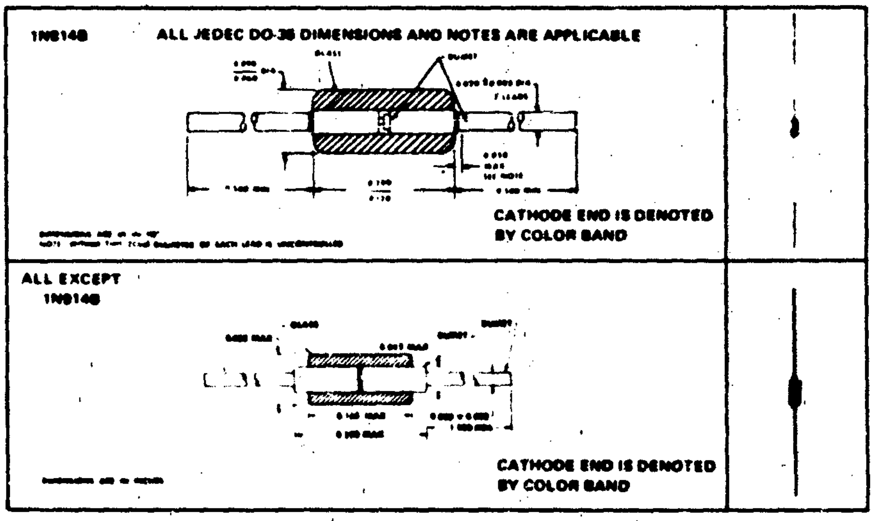
TYPES 1N914, 1N914A, 1N914B, 1N915, 1N916, 1N916A, 1N916B and 1N917 DIFFUSED SILICON SWITCHING DIODES

UNI/G·

TYPES 1N914, 1N914A, 1N914B, 1N915, 1N916, 1N916A, 1N916B, 1N917
BULLETIN NO. DL-S [illegible], JANUARY 1963
REVISED AUGUST 1966

- Extremely Stable and Reliable High-Speed Diodes

mechanical data



absolute maximum ratings at 25°C ambient temperature (unless otherwise noted)

		1N914	1N914A	1N914B	1N915	1N916	1N916A	1N916B	1N917	Unit
V_R	Reverse Voltage at — 65 to 150°C	75	75	75	50	75	75	75	30	v
I_o	Average Rectified Fwd. Current	75	75	75	75	75	75	75	50	ma
I_o	Average Rectified Fwd. Current at 150°C	10	10	10	10	10	10	10	10	ma
i_f	Recurrent Peak Fwd. Current	225	225	225	225	225	225	225	150	ma
$i_{f(surge)}$	Surge Current, 1 sec	500	500	500	500	500	500	500	300	ma
P	Power Dissipation	250	250	259	250	250	250	250	250	mw
T_A	Operating Temperature Range	-65 to 175								°C
T_{stg}	Storage Temperature Range	200								°C

Figure II-4. 1N914 Manufacturer Specification Sheet (Concluded)

$$I_S = \frac{5 \text{ mA}}{\exp\left(\frac{0.72 \text{ V}}{0.0259 \text{ V}}\right) - 1} = 4.23 \times 10^{-15} \text{ amperes}$$

2) T

a) Definition

T is the temperature of the junction in degrees Kelvin. Model paremeters should be obtained at the model simulation temperature.

b) Typical Value

T is often assumed to be room temperature, which is about 300°K. This assumption is valid for devices operated under low power conditions. If power conditions within the device make this assumption invalid, knowledge of the junction temperature or a higher order model may be desired to yield better results.

c) Measurement

When making low power measurements in climate-controlled areas, assume T to be 300°K.

h. Implementation Notes

Some difficulty may be encountered in the direct implementation of the diode equation in some circuit analysis codes. This problem is usually related to the topology requirements of the individual code. For SCEPTRE, a capacitor placed across the diode will eliminate topology problems The capacitor must be chosen small enough so as not to interfere with the diode action; 1 picofarad has been found to be adequate.

i. Computer Example

The diode equation was exercised by use of the network analysis code SCEPTRE. The forward characteristic was obtained by use of the simulation circuit of figure II-5.

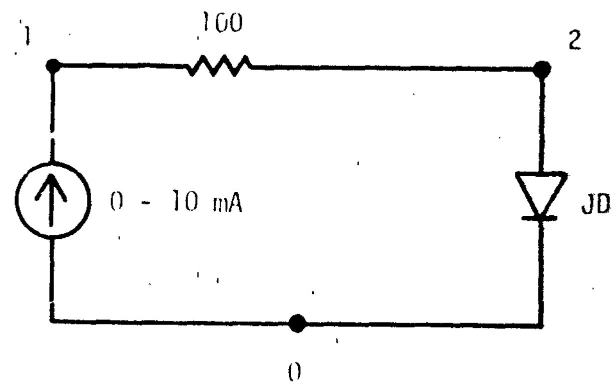


Figure II-5. Diode Test Circuit

The computer input listing for this run is given in figure II-6 and the simulated characteristic is shown in figure II-7.

As expected, the 5 mA, 690 mV point used to develop the model lies on the curve produced by the simulation.

2. <u>Reverse Bias Effects</u>

a. <u>Description</u>

The diode equation does not inherently contain provisions for reverse breakdown. However, the reverse breakdown effect may be important to the analyst who is modeling reference diodes or analyzing any circuit where transients due to radiation effects or other sources may drive the circuit into an operational mode outside the original design boundaries.

Electrical overstress produces device breakdown and possible catastrophic failure. Reverse breakdown may take place by two mechanisms, avalanche and tunneling. P-N junctions which break down at 8 volts or higher are considered to do so by avalanching mechanisms. Since the upper limit for tunneling is about 5 volts, both phenomena are considered to occur in devices with breakdown between 5 V and 8 V. There are three approaches to modeling reverse bias effects.

```
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AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2        5/76
 02/21/78     10.18.03.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD  "DOCUMENT"  AS THE FIRST CARD
OF THE INPUT TEXT



COMPUTER TIME ENTERING SETUP PHASE-
          CPA        .088 SEC.
          PP        0.000 SEC.
          IO        0.000 SEC.


CIRCUIT DESCRIPTION
ELEMENTS
JIN,0-1=TABLE 1(TIME)
RBIAS,1-2=100
JD,2-0=DIODE EQUATION(1.35E-14,38.51)
C,2-0=1.E-12
FUNCTIONS
TABLE 1
0,0,1.E-3,10.E-3
OUTPUTS
JD,PLOT(VJD)
RUN CONTROLS
STOP TIME=1.E-3
END

 SYSTEM NOW ENTERING SIMULATION



 COMPUTER TIME AT TERMINATION OF SETUP PHASE-
          CPA        .212 SEC.
          PP        0.000 SEC.
          IO        0.000 SEC.
```

Figure II-6. Diode Equation Test Circuit

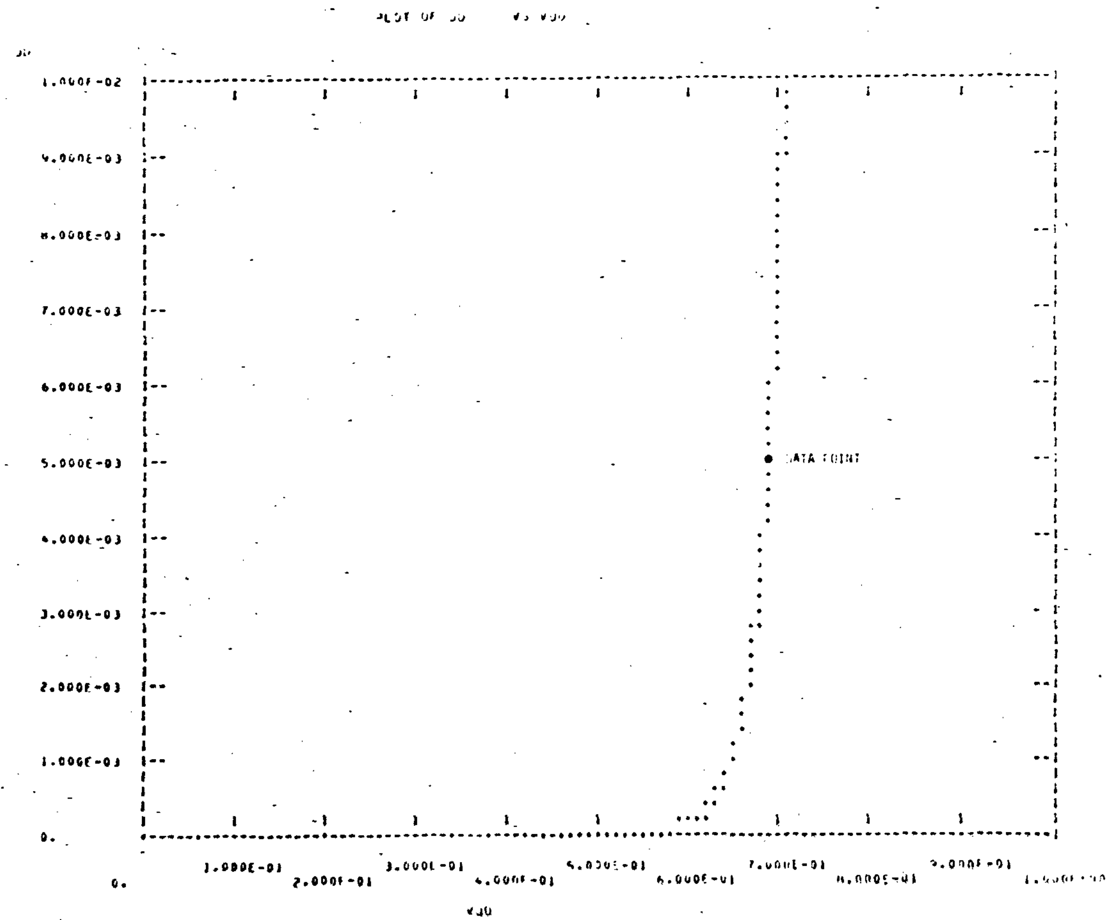

Figure II-7. Forward Region of Diode Characteristic

b. Multiplication Factor

1) Advantages

The advantage of the multiplication factor approach is that it relates better to the physical processes occurring in the diode.

2) Cautions

The multiplication factor is somewhat difficult to parameterize; therefore, care must be taken to insure the function is well behaved.

3) Characteristics

The topology required for the model is shown in figure II-8. The expected I-V characteristics are shown in figure II-9.

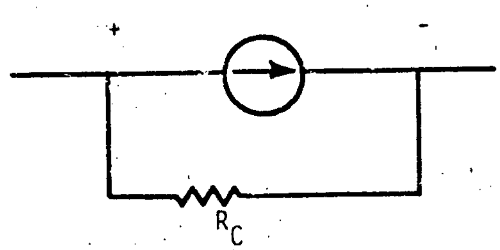

Figure II-8. Topology for Multiplication Factor Model

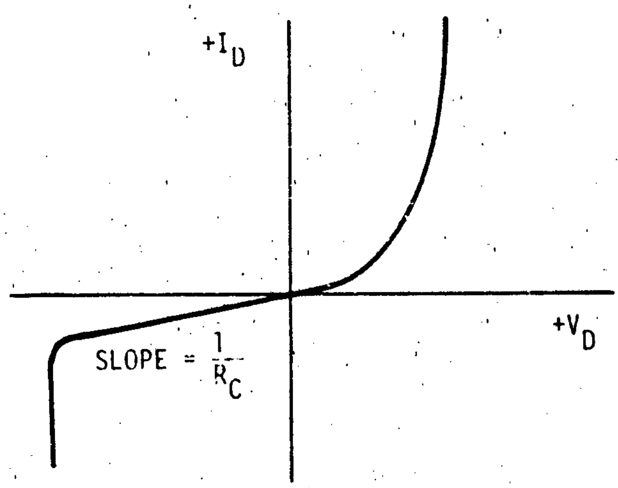

Figure II-9. I-V Characteristics of Multiplication Factor Model

4) Defining Equation

$$I_D = I_S \left[\exp\left(\frac{qV_D}{KT}\right) - 1\right] M(V)$$

$$M(V) = \frac{1}{1-\left(\frac{V_D}{V_{BD}}\right)^n}$$

5) Parameter List

V_{BD} = the breakdown voltage of the diode

$M(V)$ = the avalanche multiplication factor

n = empirical constant

6) Parameterization

a) V_{BD}

1 Definition

V_{BD} is defined as that voltage at which the reverse current increases at an almost infinite rate when voltage is increased.

2 Typical Value

V_{BD} ranges from about 5 volts for a reference diode to over 1000 volts for a high voltage rectifier.

3 Measurement

V_{BD} can be obtained from a photograph or plot of the reverse I-V characteristic. The value of V_{BD} can be determined by extrapolating the straight line portion of the breakdown curve to the voltage axis as illustrated in figure II-10.

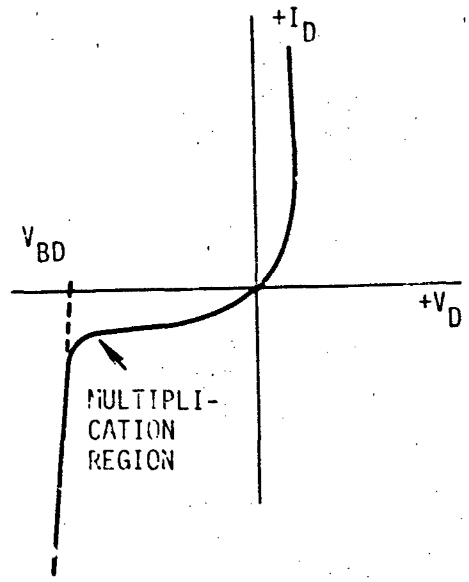

Figure II-10. Determining Breakdown Voltage

4 Example - 1N914

a From Measurements

V_{BD} may be determined from the photograph shown in figure II-3. By extrapolating along the straight line portion of the breakdown region to the voltage axis, V_{BD} was found to be 150 volts.

b From Data Sheets

The manufacturer specification sheets shown in figure II-4 lists a minimum breakdown voltage at 100 μA for the 1N914. The breakdown voltage listed is 100 volts.

b) R_C

1 Definition

R_C models the leakage current observed when a diode is reverse biased. R_C is actually voltage dependent, but assuming a constant value is a reasonable approximation.

2 Typical Value

Values of R_C vary from several kilohms to several hundred megohms.

3 Measurement

R_C may be determined by obtaining several I-V points on the diode's reverse biased characteristic. The points should be measured at least several volts away from reverse breakdown. R_C is calculated as:

$$R_C = \frac{\Delta V}{\Delta I}$$

4 Example - 1N914

a From Measurement

Reverse leakage current was measured by a sensitive current meter in series with the diode and then reverse biasing the diode with a power supply. Data obtained were:

V_D	I_D
-10 V	-5.4 nA
-50 V	-19.0 nA

$$R_C = \frac{-10\text{ V} - (-50\text{ V})}{-5.4\text{ nA} - (-19\text{ nA})}$$

$$R_C = 2.94 \times 10^9 \text{ ohms}$$

b From Data Sheets

The manufacturer specification sheet shown in figure II-4 lists maximum reverse current for the 1N914 at a reverse voltage of 20 volts. Since leakage current is usually much greater than saturation current, the following approximation will be applied:

$$R_C = \frac{V_D}{I_D}$$

$$R_C = \frac{-20\ V}{-0.025\ \mu A}$$

$$R_C = 8.0 \times 10^8 \text{ ohms}$$

c) <u>n</u>

<u>1</u> <u>Definition</u>

n is an experimental constant which models the multiplication region of the reverse diode characteristic.

<u>2</u> <u>Typical Value</u>

The value of n is typically between 2 and 4 for silicon diodes.

<u>3</u> <u>Measurement</u>

n can be determined from a point on the reverse characteristic in the multiplication region. n can be computed as:

$$n = \frac{\log\left[1 - \left(\frac{I_S + \frac{-V_D}{R_C}}{I_D}\right)\right]}{\log\left(\frac{-V_D}{V_{BD}}\right)}$$

<u>4</u> <u>Example - 1N914</u>

A point taken at the knee of the breakdown characteristic (figure II-3) yields:

$I_D = -0.5\ \mu A$
$V_D = -140\ V$

I_S and R_C are 1.35×10^{-14} amperes and 2.94×10^{9} ohms, respectively. n may now be computed as:

$$n = \frac{\log\left[1 - \dfrac{(1.35 \times 10^{-14}\ \mathrm{A} + 140/2.94 \times 10^{9})}{0.5\ \mu\mathrm{A}}\right]}{\log\ (140\ \mathrm{V}/150\ \mathrm{V})}$$

$$n = 1.45$$

c. <u>Direct Simulation Approach</u>

1) <u>Advantages</u>

The advantages of the direct simulation approach are that parameterization is straightforward and better simulation of resistance in breakdown is permitted.

2) <u>Cautions</u>

Photocurrent and leakage current will not undergo multiplication.

3) <u>Characteristics</u>

The topology required for the model is shown in figure II-11.

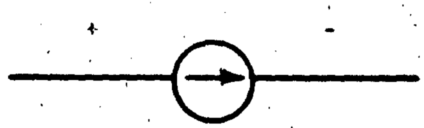

Figure II-11. Topology for Direct Simulation Model

The expected I-V characteristics are shown in figure II-12.

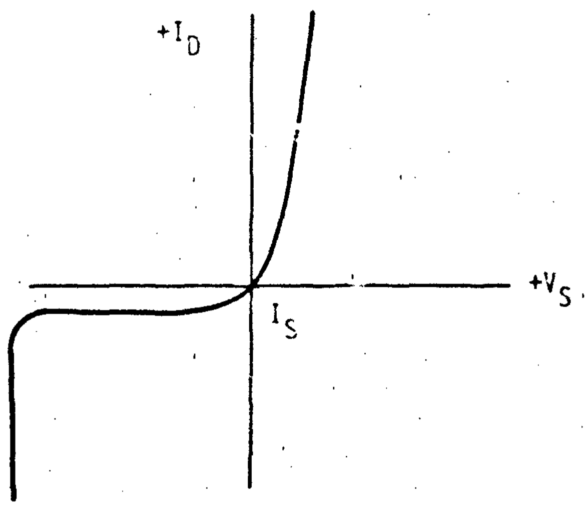

Figure II-12. I-V Characteristics for Direct Simulation Model

4) Defining Equations

$$I_D = I_S \left[\exp\left(\frac{qV_D}{KT}\right) - 1 \right] - f(V_D)$$

$f(V_D)$ = piecewise linear table or:

$$= I_S \, e^{A(V_D - V_{BD})}$$

5) Parameter List

V_{BD} = the breakdown voltage of the diode

A = empirical constant

I_S = diode leakaye current

6) Parameterization

a) Breakdown Table

The breakdown table was obtained from selected points on the reverse characteristic. The points chosen are shown in table II-1.

TABLE II-1. DIODE BREAKDOWN

V_{BD}	I_D
-152 V	-60 mA
-151	-30
-148	-200 μA
-147	-100
-144	-50
-140	-25
-120	-10
-100	-5

b) Electrical Analog Approach

1 Advantages

The advantage of the electrical analog approach is that no analytical functions or tables are required.

2 Cautions

The multiplication region of the characteristic is not accurately modeled. There is no correspondence to physical behavior.

3 Characteristics

The topology required for the model is shown in figure II-13.

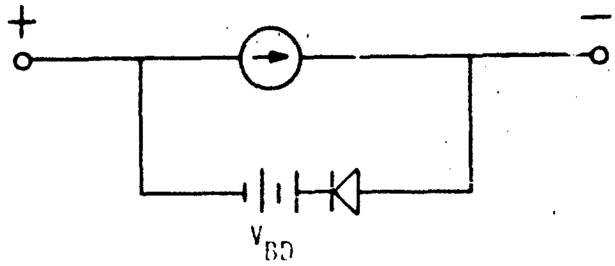

Figure II-13. Topology for Electrical Analog Model

The shunt diode is clamped "off" by the voltage source. When a reverse voltage is applied to the model which exceeds the voltage source, the shunt diode will conduct, simulating the breakdown characteristic. The multiplication region of the characteristic is simulated by the forward I-V behavior of the shunt diode. The characteristic produced will be similar, as shown in figure II-14.

d. Computer Examples

Two computer simulations of reverse breakdown were made, one by direct simulation and one by use of the multiplication factor. The test circuit applied for these simulations is shown in figure II-15.

The computer listing for the direct simulation test using a piecewise linear table is given in figure II-16. The breakdown characteristic produced is shown in figure II-17.

The input listing for the multiplication factor simulation is given in figure II-18. The output for this run is given in figure II-19.

Three features of figure II-19 are noteworthy. First, the curvature of the avalanche region is much more abrupt than indicated by the actual data. Second, the feature included in the multiplication

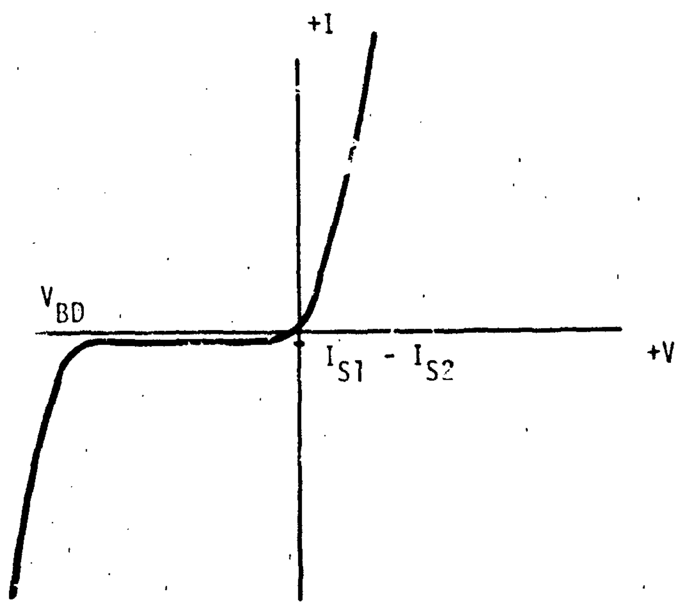

Figure II-14. I-V Characteristic of Electrical Analog Model

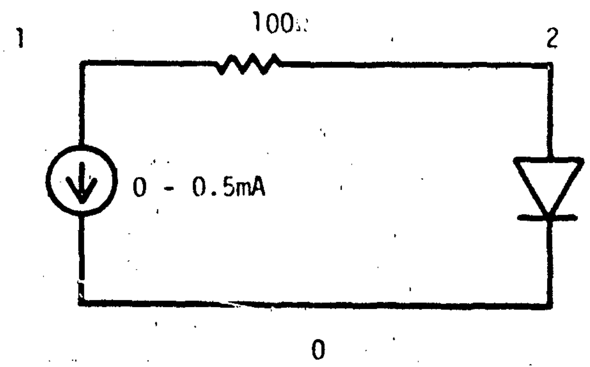

Figure II-15. Breakdown Test Circuit

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AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2        5/75.
 02/22/78     11.32.43.

FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD "DOCUMENT" AS THE FIRST CARD
OF THE INPUT TEXT

COMPUTER TIME ENTERING SETUP PHASE-
         CPA        .090 SEC.
         PP        0.000 SEC.
         IO        0.000 SEC.

CIRCUIT DESCRIPTION
ELEMENTS
JIN,0-1=TABLE 1(TIME)
RBIAS,1-2=100
JD,2-0=DIODE EQUATION(1.35E-14,38.51)
JB,2-0=TABLE 2(VJD)
C,2-0=1.E-12
FUNCTIONS
TABLE 1
0,0,1.E-3,-5.E-4
TABLE 2
-152,-60.E-3
-151,-30.E-3
-148,-200.E-6
-147,-100.E-6
-144,-50.E-6
-140,-25.E-6
-120,-10.E-6
-100,-5.E-6
OUTPUTS
JIN,PLOT(VJD)
RUN CONTROLS
STOP TIME=1.E-3
END

SYSTEM NOW ENTERING SIMULATION

COMPUTER TIME AT TERMINATION OF SETUP PHASE-
         CPA        .244 SEC.
         PP        0.000 SEC.
         IO        0.000 SEC.
```

Figure II-16. Listing for Breakdown Test Circuit

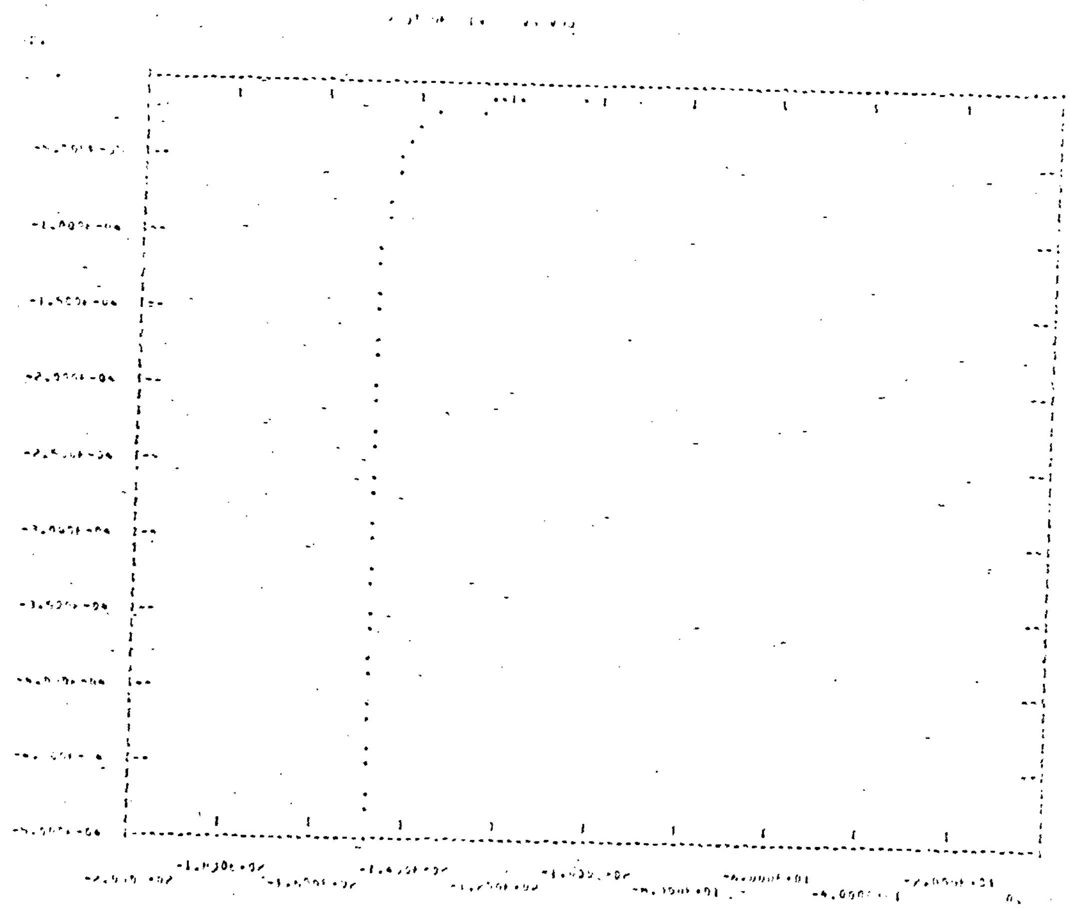

Figure II-17. Breakdown Characteristic as Predicted by Tabular Approach

```
S C E P T R E   NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2        5/75
 02/22/78     15.06.35.


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COMPUTER TIME ENTERING SETUP PHASE-
          CPA       .373 SEC.
          PP       0.000 SEC.
          IO       0.000 SEC.


CIRCUIT DESCRIPTION
ELEMENTS
JIN,0-1=TABLE 1(TIME)
RBIAS,1-2=100
JD,2-0=DIODE EQUATION(1.35E-14,38.51)
JR,2-0=X3(PMV*(IRC-1.35E-14))
C,2-0=1.E-12
RC,2-0=2.9E9
DEFINED PARAMETERS
PMV=XP(1./(1.-AMIN1(.99999999,(ABS(VJD/150.))**1.45)))
FUNCTIONS
TABLE 1
0,0,1.E-3,-5.E-4
OUTPUTS
JIN,PLOT(VJD)
RUN CONTROLS
STOP TIME=1.E-3
END

SYSTEM NOW ENTERING SIMULATION


COMPUTER TIME AT TERMINATION OF SETUP PHASE-
          CPA      1.203 SEC.
          PP       0.000 SEC.
          IO       0.000 SEC.
```

Figure II-18. Reverse Breakdown Simulation

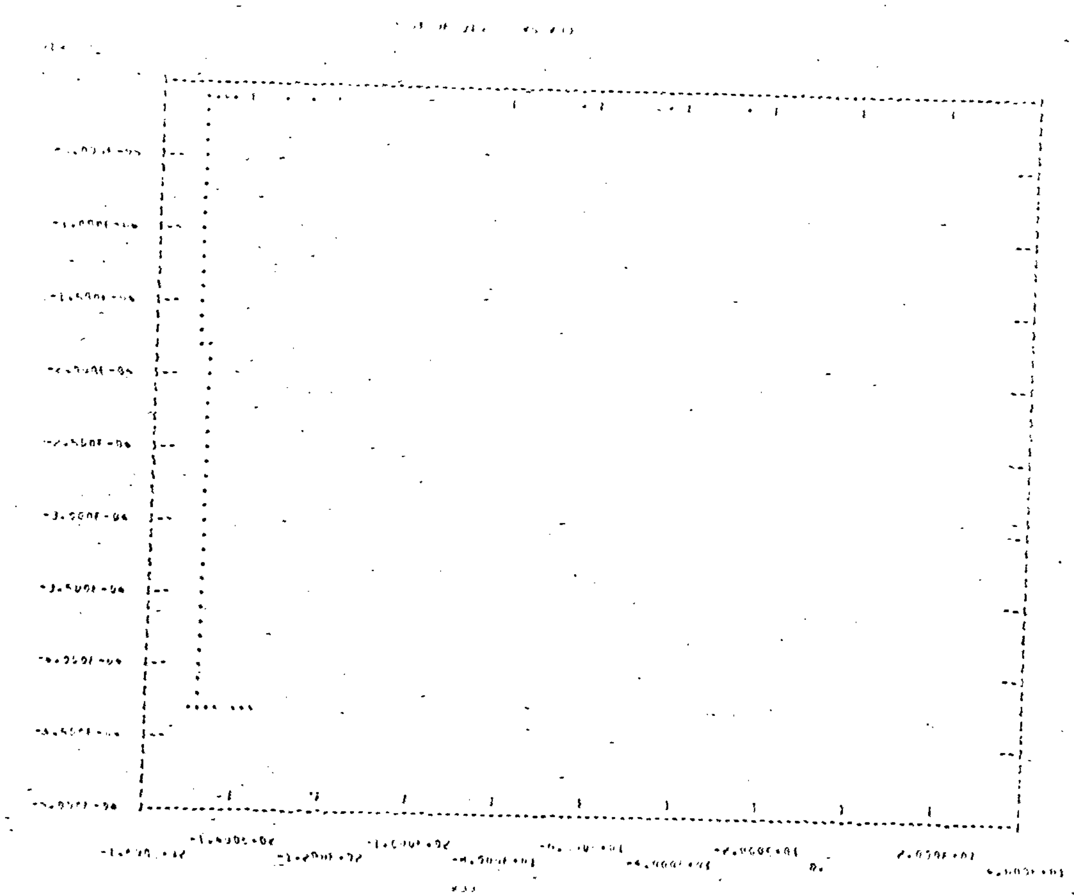


Figure II-19. Breakdown Simulation by use of Multiplication Factor

formula to prevent a singularity when $V_{BD} = V_D$ has also limited breakdown current to less than 0.5 mA. Such limiting can occur if the proper selection of limiting constants is not made. Finally, the slope of the breakdown characteristic is negative. This result may arise if a bulk resistance term is not included.

3. Nonideal Diode Equation

a. Description

The analyst who wishes to correctly simulate diode performance over several decades of current quickly notes that the ideal diode equation is not sufficient because most diodes do not have an ideal characteristic. The reason for this deviation from the ideal is a reflection of the efficiency of the diode as an emitter of minority carriers.

A semilog plot of V_D over a wide range of I_D will identify the region of nonideal behavior. Such a plot is demonstrated in figure II-20.

The nonideal region can be modeled as an emission constant in the diode equation.

b. Advantages

The inclusion of an emission constant permits accurate simulation of diode I-V characteristics over several decades of current.

c. Cautions

The inclusion of an emission constant generally requires some source of experimental data to determine the value of the emission constant. Distinctions must be made between variations in M and the change in I-V characteristics due to low and high injection effects.

d. Characteristics

The inclusion of an emission constant will produce an I-V characteristic which deviates from the ideal as illustrated in figure II-21.

e. Defining Equation

$$I_D = I_S \left[\exp\left(\frac{qV_D}{MKT}\right) - 1\right]$$

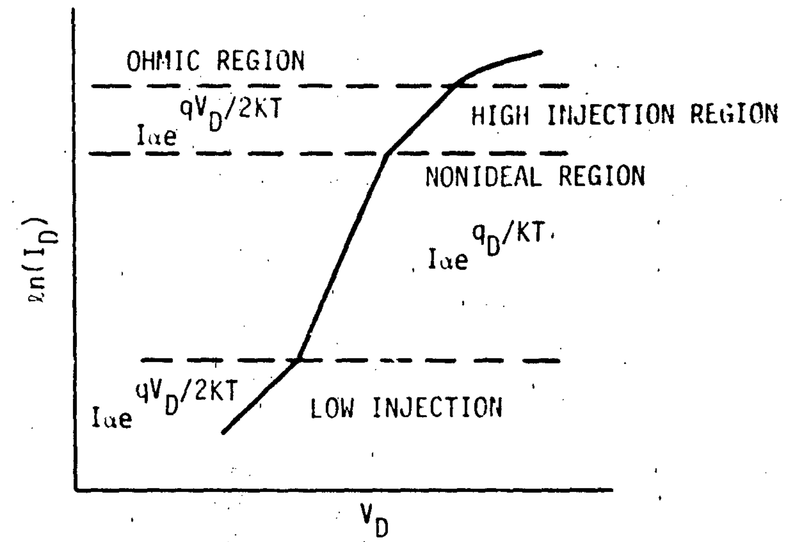


Figure II-20. Nonideal Diode Behavior

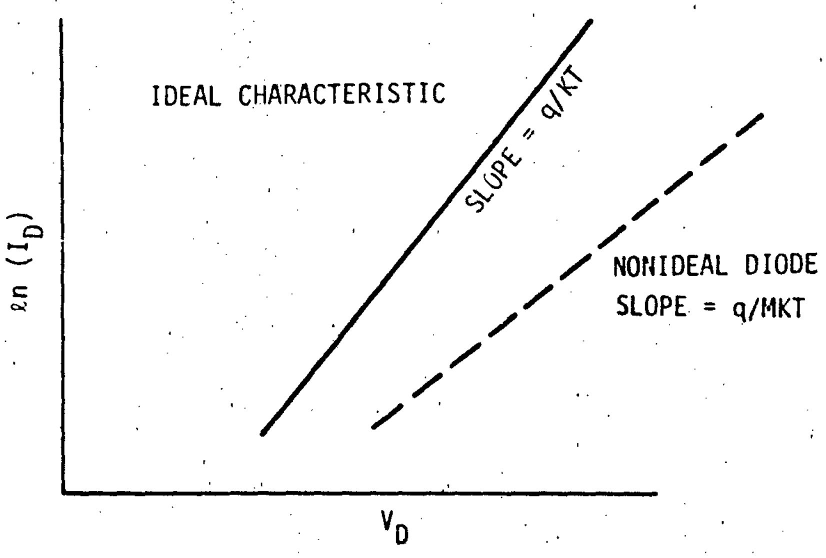


Figure II-21. I-V Characteristics Using an Emission Constant

f. Parameterization (M)

1) Definition

The constant M is the factor by which the junction voltage and dynamic resistance are larger than the ideal values given using qV_D/KT.

2) Typical Value

M equals 1 for the ideal case, but typically lies between 1 and 2.

3) Measurement

M can be found by identifying the nonideal line segment from a plot of $\ell n(I_D)$ as a function of V_D. A best fit to several points will yield the most acceptable value of M. Two points on the nonideal line segment will identify M as:

$$M = \frac{q(V_2 - V_1)}{KT\ \ell n(I_2/I_1)}$$

A new corresponding value for I_S must now be computed from one point on the line as:

$$I_S = \frac{I_D}{\exp\left(\frac{qV_D}{MKT}\right) - 1}$$

4) Example - 1N914

The I-V data assembled for determination of the dc parameters are listed in table II-2.

A plot of these data on a semilog plot produces figure II-22. Region 1 appears to be the nonideal region, region 2 is the high injection region, and region 3 is the ohmic region.

TABLE II-2. MEASURED I-V CHARACTERISTICS OF 1N914

I_D	V_D
1 µA	0.304 volts
4	0.373
10	0.416
40	0.481
100	0.521
400	0.585
1 mA	0.628
4	0.694
10	0.742
40	0.843
80	0.902
100	0.929
200	0.999
300	1.13
400	1.16
500	1.27
600	1.33
700	1.36

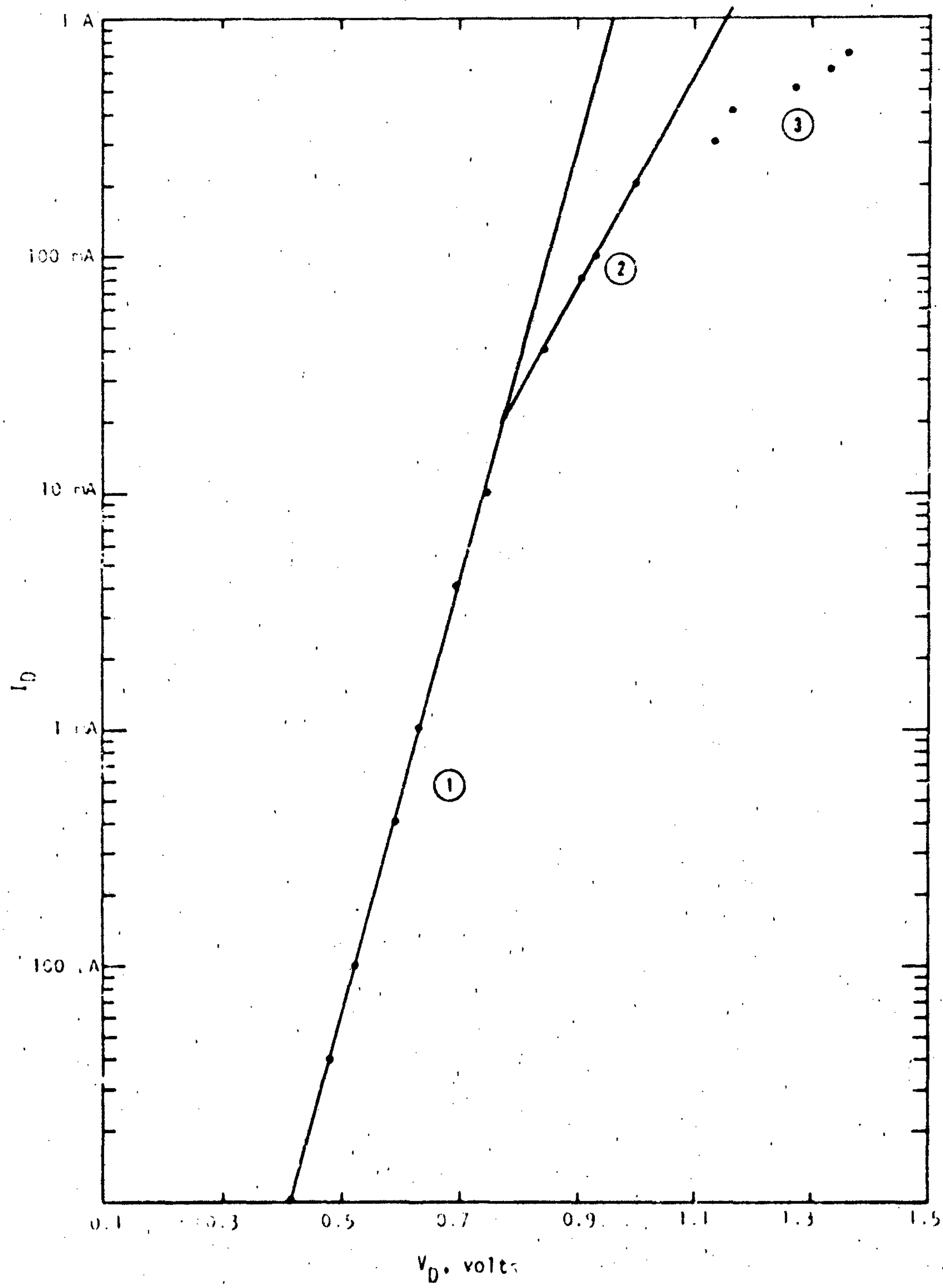


Figure II-22. 1N914 I-V Data

Choosing 10 μA and 1 mA as representative of the nonideal line segment yields:

$$M = \frac{(0.628\ V - 0.416\ V)}{0.0259\ V\ \ell n\ (1\ mA/10\ \mu A)} = 1.78$$

A new value of I_S must now be computed as:

$$I_S = \frac{10\ \mu A}{\exp\left[\frac{0.416}{(0.0259)(1.78)}\right] - 1} = 1.21 \times 10^{-9}\ \text{amperes}$$

4. High Injection Effects

a. Description

As the current through a diode increases, the injected carriers become approximately equal to the carrier concentration of the lightly doped side of the junction. This leads to the buildup of a retarding potential and is manifested as a change in the I-V characteristic. High injection may be modeled as a modification to the diode equation.

b. Advantages

Modeling of diode characteristics is permitted over an even larger number of current decades than is possible with the nonideal diode model.

c. Cautions

Additional reliance on experimental data is required. Additional parameterization effort is also needed.

d. Characteristics

Addition of the high injection modifications to the diode will produce the characteristic shown in figure II-23.

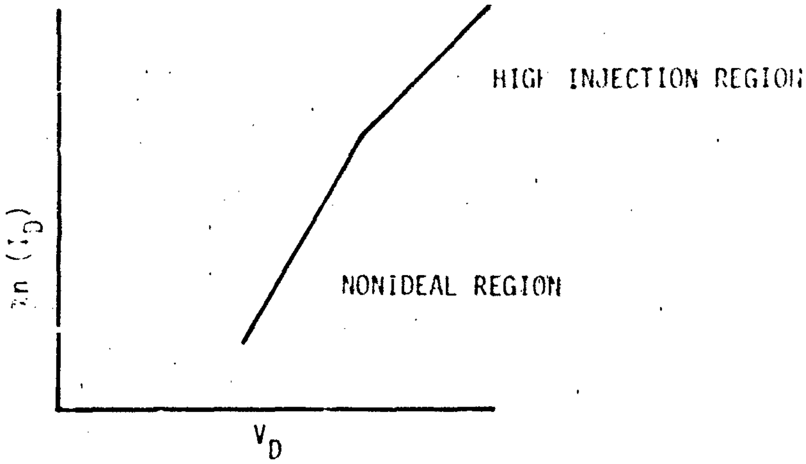


Figure II-23. Inclusion of High Injection

e. Defining Equation

$$I_D = \frac{I_S\left[\exp\left(qV_D/MKT\right) - 1\right]}{1 + \phi \exp\left(qV_D/2MKT\right)}$$

f. Parameterization

1) Definition

The parameter ϕ models the deviation from the ideal diode I-V characteristic due to high injection. High injection effects are sometimes difficult to observe and may be obscured by the effects of ohmic resistance.

2) Typical Value

A typical value of ϕ is 10^{-6}.

3) Measurement

Log(I_D) versus V_D is plotted over a wide range of diode current values. High injection occurs at the point where I_D changes from being proportional to exp (qV_D/MKT) to approximately proportional to exp ($qV_D/2MKT$). The parameter ϕ describes the high current asymptote of the log(I_D) versus V_D graph as:

$$I_D(\text{high level}) = \frac{I_S}{\phi} \exp\left[\frac{qV_D(\text{high level})}{2\ MKT}\right]$$

Choosing an operating point in high injection will yield an I_D(high level) and a V_D(high level).

4) Example - 1N914

To determine if high injection or bulk resistance effects account for the slope of line 2, the two constants will be determined. If slope 2 (figure II-22) is approximately $qV_D/2MKT$, then high injection effects probably account for line 2. Choosing two points from each line,

$$\text{slope 1} = \frac{\ln 1\ \text{mA} - \ln 1\ \mu\text{A}}{0.628\ \text{V} - 0.304\ \text{V}} = 21.3$$

$$\text{slope 2} = \frac{\ln 80\ \text{mA} - \ln 40\ \text{mA}}{0.902\ \text{V} - 0.843\ \text{V}} = 11.7$$

$$\frac{\text{slope 1}}{\text{slope 2}} = 1.82$$

which is close enough to 2 to justify the assumption that above 0.78 V, high injection effects occur. ϕ can now be calculated.

$$80\ \text{mA} = \frac{1.21 \times 10^{-9}\ \text{A}}{\phi} \exp\left[\frac{0.902\ \text{V}}{2(1.78)(0.0259\ \text{V})}\right]$$

$$\phi = 2.68 \times 10^{-4}$$

5. Ohmic Effects

a. Description

At the highest injection levels, the ohmic properties of the semiconductor material may contribute significantly to the I-V characteristics of the diode. This resistive term could theoretically be

calculated from knowledge of the material resistivity, the device area, and the width of the semiconductor material between the junction and the ohmic contact as:

$$R = \frac{\rho \ell}{A}$$

However, the resistive term may be more easily and reliably calculated from the I-V characteristic if appropriate care is taken in distinguishing ohmic and high injection effects.

b. Advantages

The addition of bulk resistance yields the most complete and accurate model over all regions of forward biased diode operation.

c. Cautions

Requires an additional electrical element and access to experimental data to determine value.

d. Characteristics

Bulk resistance is modeled by inclusion of a discrete series resistor as shown by figure II-24.

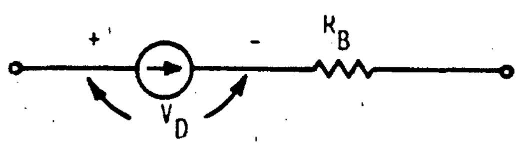


Figure II-24. Modeling Bulk Resistance

Inclusion of bulk resistance to the complete nonideal diode model will yield the characteristic of figure II-25.

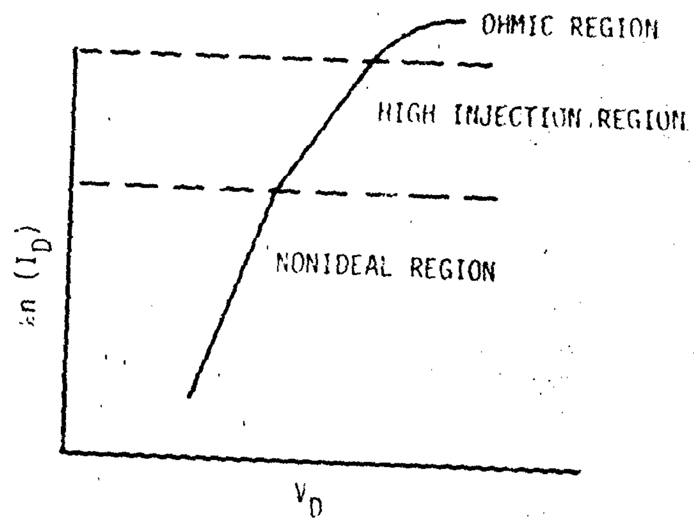


Figure II-25. Inclusion of Bulk Resistance

e. Parameterization (R_B)

1) Definition

R_B is the series ohmic resistance of the diode.

2) Typical Value

A typical value for R_B is 1 ohm.

3) Measurement

R_B may be determined from two points in the ohmic region of the diode as:

$$R_B = \frac{(V_2 - V_1) - (XMKT/q)\ \ell n(I_2/I_1)}{I_2 - I_1}$$

where:

$X = 1$, if the diode is not in high injection
$X = 2$, if the diode is in high injection

f. <u>Examples - 1N914</u>

The two points in the ohmic region chosen for analysis are:

V_D	I_D
1.13 V	300 mA
1.27	500

$$R_B = \frac{\left[(1.27\ V - 1.13\ V) - (2)(1.78)(0.0259)\ \ell n\,(500\ mA/300\ mA)\right]}{(500\ mA - 300\ mA)}$$

$$R_B = 0.464\ \text{ohms}$$

g. <u>Computer Example</u>

The simulated I-V characteristic of the 1N914 diode model was produced to allow comparison with experimental data. The simulated test circuit applied is illustrated in figure II-26. Nonideal, high injection, and ohmic effects were included in the model.

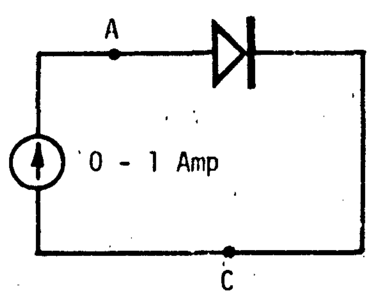


Figure II-26. Wide Current Range Model Test Circuit

The input listing for this run is shown in figure II-27. The results of this run were plotted in figure II-28. Satisfactory simulation results were obtained over 5 decades of current.

```
S C E P T R E    NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2        5/75
 02/23/78     17.07.21.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD  "DOCUMENT"  AS THE FIRST CARD
OF THE INPUT TEXT


COMPUTER TIME ENTERING SETUP PHASE-
          CPA         .351 SEC.
          PP         0.000 SEC.
          IO         0.000 SEC.


MODEL DESCRIPTION
MODEL IN914 (1-3)
ELEMENTS
RR.2-3=0.45
RC.1-2=2.94E4
JD.1-2=X1(1.21E-9*(EXP(21.69*VJD)-1)/(1.+2.66E-4*EXP(21.69/2*VJD)))
C.1-2=1.E-12
CIRCUIT DESCRIPTION
ELEMENTS
D1.A-C=MODEL IN914
JSIG.C-A=TABLE 1(TIME)
FUNCTIONS
TABLE 1
0.0.1.1
OUTPUTS
JSIG.PLOT(VJSIG)
RUN CONTROLS
STOP TIME=1
MAXIMUM PRINT POINTS=100
END


SYSTEM NOW ENTERING SIMULATION


COMPUTER TIME AT TERMINATION OF SETUP PHASE-
          CPA        1.205 SEC.
          PP         0.000 SEC.
          IO         0.000 SEC.
```

Figure II-27. Diode Forward Characteristic Test Circuit

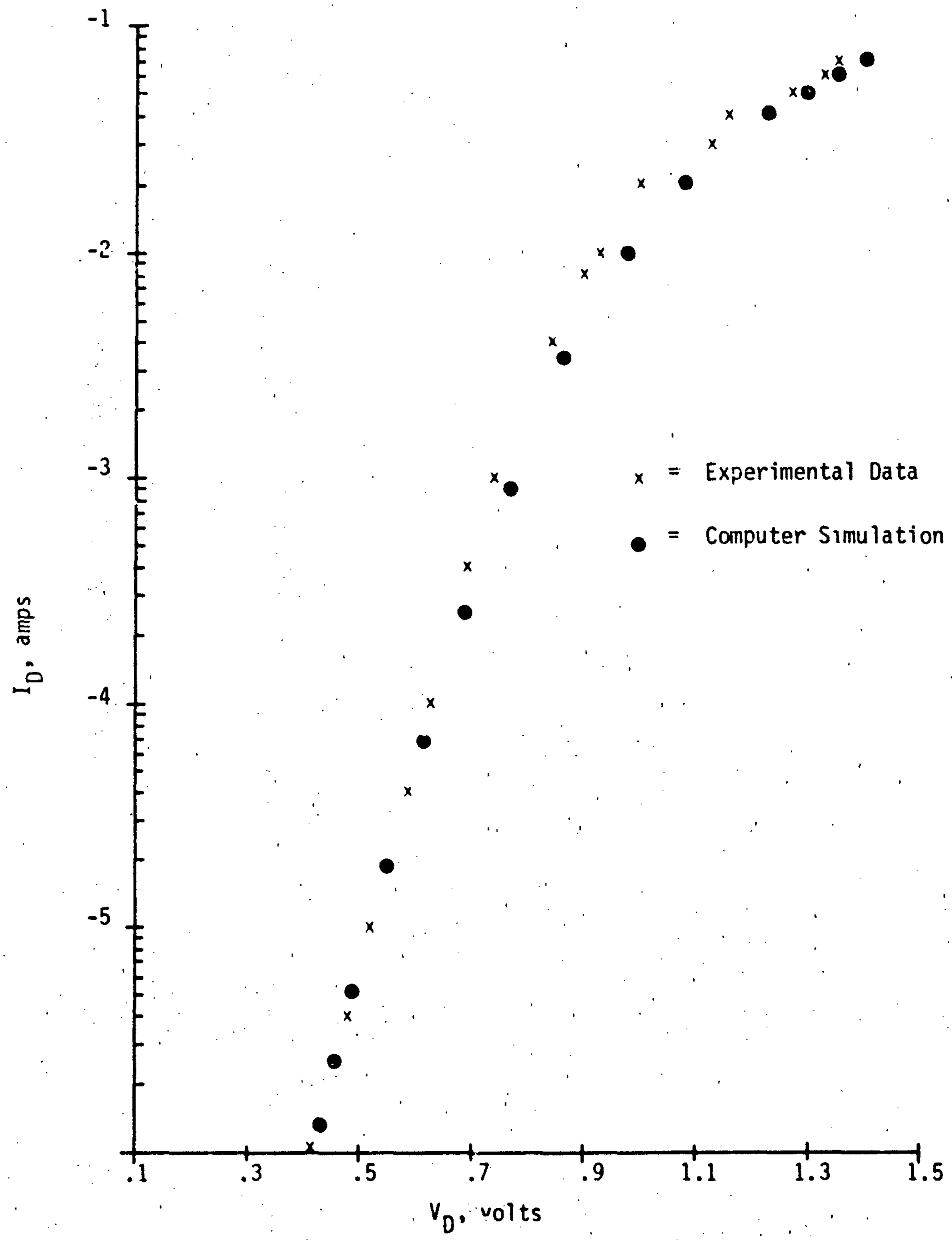


Figure II-28. Forward Characteristics

6. Depletion Region Capacitance

a. Description

The existence of a depletion region in the vicinity of the metalurgical junction of the diode gives rise to an effective parallel plate capacitance. This capacitance is usually referred to as the junction capacitance. Increasing the reverse bias across the junction has the effect of providing a greater separation between the "plates" of the capacitor and lowering the capacitance. This phenomena is modeled as a voltage variable capacitance in parallel with the diode current generator.

b. Advantages

The addition of the depletion (or transition) capacitor will improve the model accuracy in any analysis where the transient characteristics are important. As noted earlier, many codes require a capacitive element in parallel with the diode current generator in order to make the voltage across the diode a state variable. A small constant capacitance will satisfy this requirement, but a voltage variable capacitance requires no additional elements and very little additional mathematical complexity.

c. Cautions

Time-consuming capacitance measurements must be made with a capacitance bridge to develop the capacitance models.

d. Characteristics

The diode topology required for the addition of depletion capacitance is given in figure II-29.

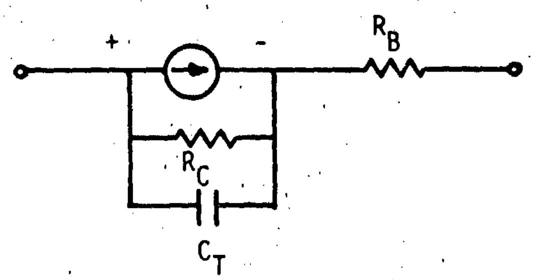


Figure II-29. Diode Topology for Inclusion of Depletion Capacitance

A typical plot of depletion capacitance as a function of diode bias is shown in figure II-30.

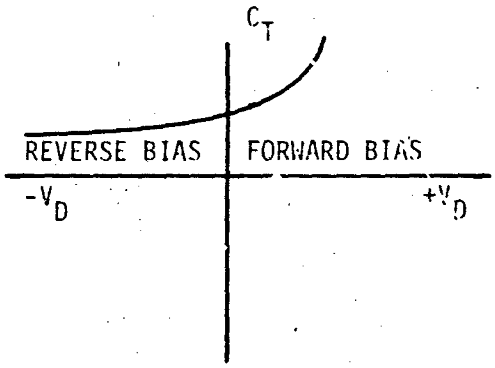


Figure II-30. Capacitance Versus Bias

e. Defining Equation

$$C_T = \frac{C_{TO}}{\left(1 - \frac{V_D}{\psi}\right)^m}$$

f. Parameter List

C_T = value of depletion capacitance

C_{TO} = the value of the diode junction capacitance at $V_D = 0$

ψ = the junction barrier potential

m = the junction capacitance gradient factor

g. Parameterization (C_{TO}, ψ, m)

1) Definition

C_{TO}, ψ, and m are the thr parameters that describe this junction capacitance due to the fixed charge in the junction depletion region. C_{TO} is the value of C_T at $V_D = 0$, ψ is the built-in barrier potential, and m is the capacitance gradient factor.

2) Typical Value

C_{T0} is typically on the order of 0.3 pF/mil^2 of junction area. The barrier potential ψ is usually about 0.6 V. The constant m will usually be between 0.333 (graded junction) and 0.5 (step junction) but may be much less for gold doped junctions.

3) Measurement

The junction capacitance can be obtained as a function of voltage by means of a bridge such as the Boonton model 75 or the Hewlett-Packard 4271.

A method of reducing the data by graphical techniques is to make an initial guess for ψ and then plot the resultant value of C_T as a function of $(\psi - V_D)$ on log-log graph paper. If a straight line results, the chosen values are assumed to be correct. If the line is not straight, a new guess is made for ψ and a new plot is made. If the curve is concave in a downward direction, decrease ψ.

Another technique is to plot $(C_T)^{-1/m}$ as a function of V_D. Plotting $1/C^3$ and $1/C^2$ are good starting points since a straight line result will establish the junction as linearly graded or abruptly discontinuous, respectively. When a straight line is obtained, ψ is determined by extrapolating the line to the V_D axis.

4) Example - 1N914

C-V data obtained in the reverse biased region are shown in table II-3.

TABLE II-3. JUNCTION CAPACITANCE VERSUS REVERSE BIAS

C_T	V_D
1.365 pF	0 volts
1.350	-0.5
1.354	-0.8
1.342	-1.0
1.336	-1.5
1.325	-2.5

Plotting $1/C^2$ and $1/C^3$ as a function of V_D yields the plots shown in figures II-31 and II-32, respectively. The similar curves indicate that the junction grading coefficient does not lie between 0.5 and 0.333 as predicted by simple theory. However, this result is not surprising since the 1N914 is gold doped. To find the grading coefficient, a different graphical technique will be applied for example purposes.

The first guess for the plot is $\psi = 0.6$ V. The resulting values for the plot are shown in table II-4. The resultant plot is illustrated in figure II-33. Since this plot forms a reasonably straight line, ψ is assumed to be 0.6 V and no other values of ψ need be tried. The value of -m is the inverse slope of the line plotted in figure II-33 and is:

$$-m = \frac{\log 1.365 \text{ pF} - \log 1.325 \text{ pF}}{\log 0.6 \text{ V} - \log 3.1 \text{ V}} = -0.0181$$

TABLE II-4. ALTERNATE CAPACITANCE DETERMINATION

C_T	$\psi - V_D$
1.365 pF	0.6 volts
1.350	1.1
1.345	1.4
1.342	1.6
1.336	2.1
1.325	3.1

C_{TO} can be calculated from the capacitance formula and a single raw data point as:

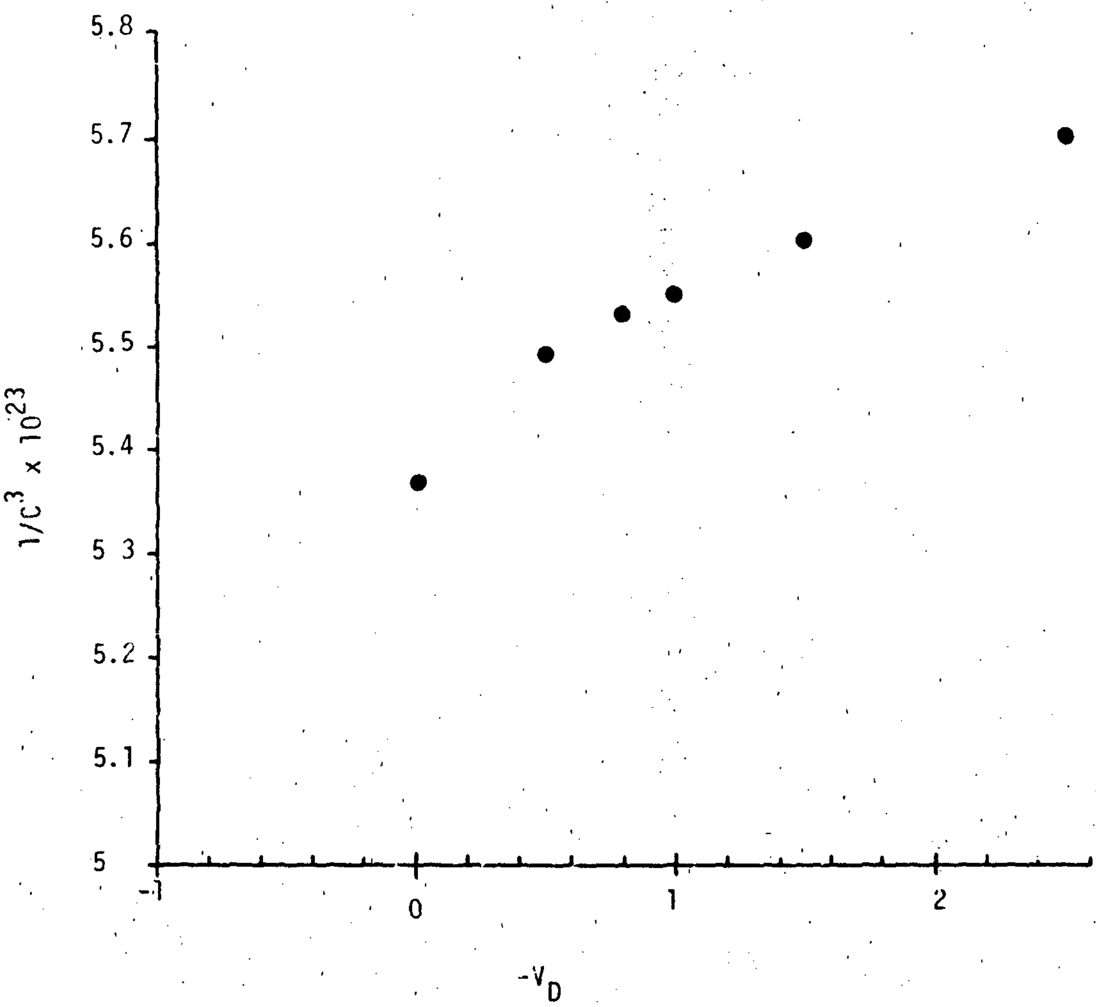


Figure II-31. $1/C^2$ Versus V_D

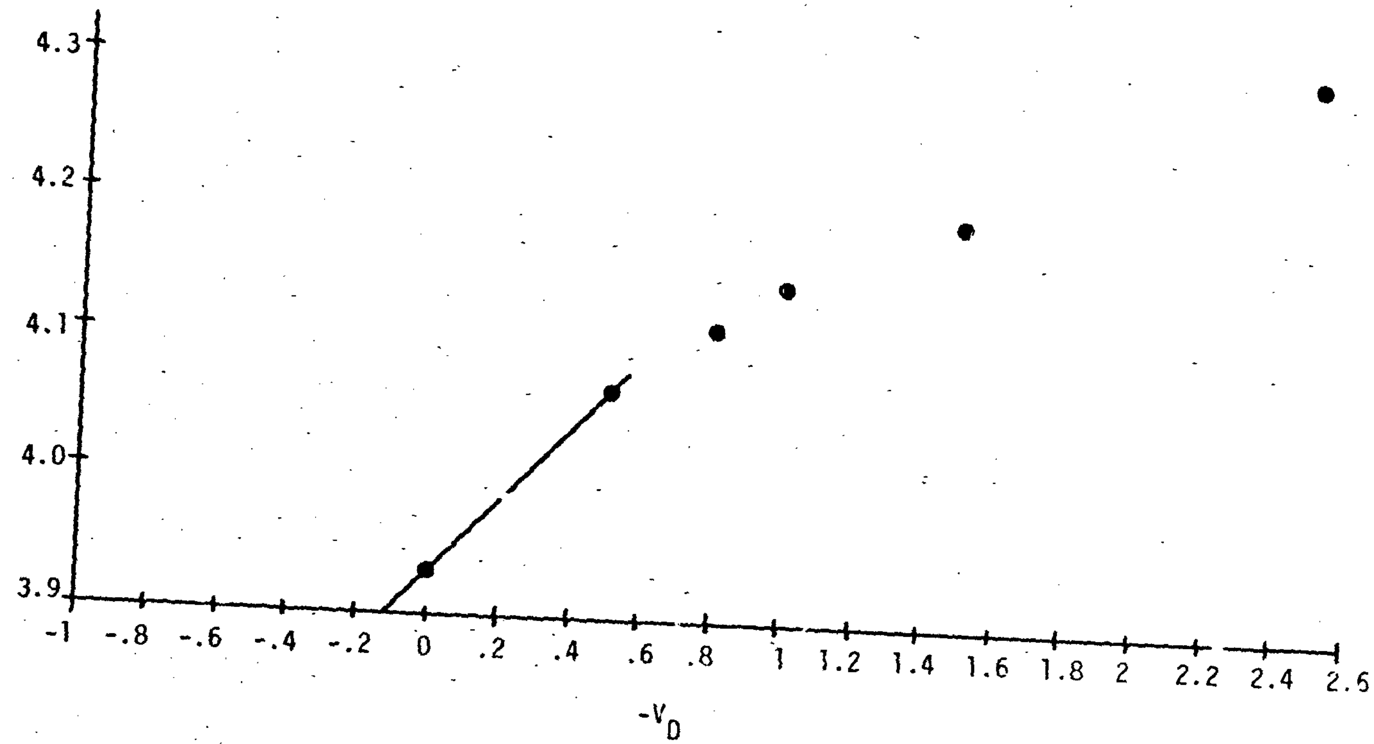


Figure II-32. $1/C^3$ Versus V_D

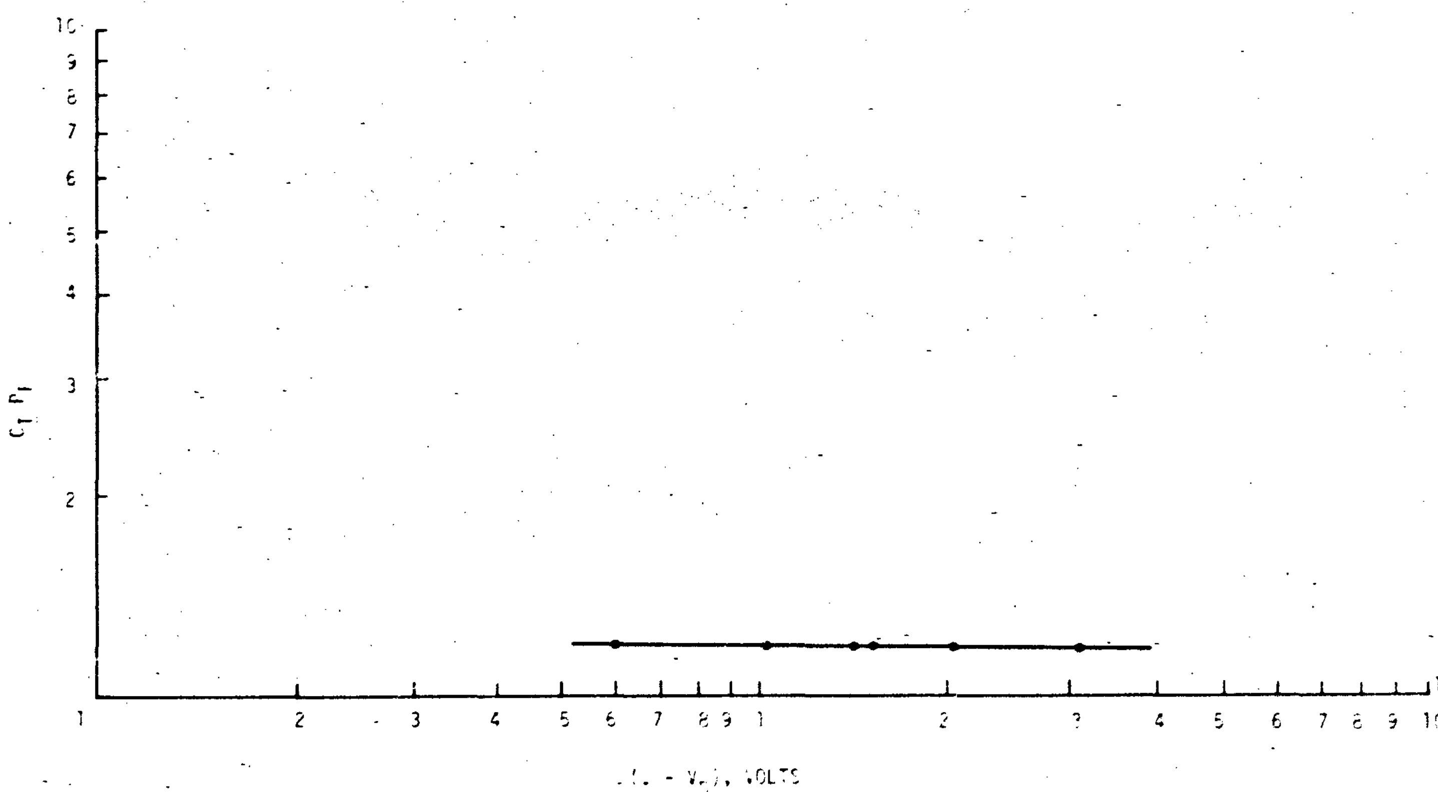


Figure II-33. Reduced C-V Plct

$$C_{TO} \text{ @ } -1\text{ V} = 1.342\text{ pF}\left[\frac{1-(-1\text{ V})}{0.6\text{ V}}\right]^{0.0181} = 1.37\text{ pF}$$

The experimental value of C_{TO} (V_D = 0 V) was 1.365 pF.

h. Implementation Notes

Direct implementation of the depletion capacitance equation will result in a singularity if $V_D = \psi$. To avoid this singularity, a typical capacitance equation will limit the term V_D/ψ to some value less than unity through application of the AMIN1 function. Limiting the capacitance by this means will have little affect on simulation results for the following reasons:

(1) Diffusion capacitance in the forward region will dominate over depletion capacitance.

(2) The depletion approximation used to develop the capacitance equation looses its validity as V_D approaches ψ.

7. Diffusion Capacitance Effects

a. Description

When the diode is forward biased, excess minority charge carriers are in transit throughout the semiconductor material. These carriers can be thought of as a charge stored in the volume of semiconductor material and modeled as a charge stored in a capacitive element. This capacitance is usually referred to as the diffusion capacitance and is proportional to the diode current.

b. Advantages

For transient analysis, the diffusion capacitance is essential in modeling diode storage time.

c. Cautions

Parameterization of the diffusion capacitance generally requires access to sophisticated pulsed measurement facilities or specification sheet data for storage time.

d. Characteristics

The topology required for the modeling of charge storage effects is given in figure II-34.

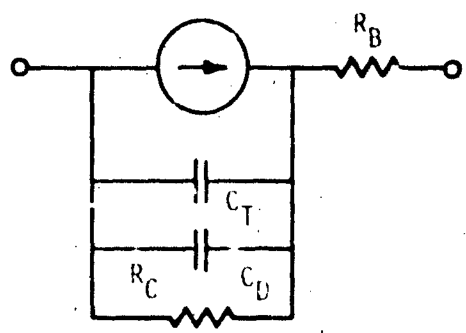


Figure II-34. Complete Charge Storage Diode Model

e. Defining Equation

$$C_D = \frac{q\ t_{cs}\ (I_D + I_S)}{MKT}$$

f. Parameterization (t_{cs})

1) Definition

t_{cs}, the charge storage factor, is related to the time required for all charges stored in the semiconductor volume to be dissipated. This constant will be a function of minority carrier life time, diffusion velocity, and other parameters which describe charge storage.

2) Typical Value

A typical value of the charge storage factor is 10 ns. Values from 0.1 ns to 1 μs are common.

3) Measurement

t_{cs} can be found by application of the expression

$$t_{cs} = \left(\frac{1}{2\pi F}\right) - C_T R_B$$

where F is the intrinsic diode cutoff frequency. Knowing the storage time, the frequency parameter F (required in the previous equation) is calculated from:

$$F = \frac{\ln (1 + I_F/I_R)}{2\pi\ t_s}$$

where:

I_F = the diode forward current
I_R = the diode reverse current
t_s = the diode storage time

Specification sheets often contain the necessary information to calculate F. A test configuration similar to the one shown in figure II-35 can be used to obtain diode storage time experimentally. The power supply is adjusted to obtain the desired forward test current. The pulse generator is then adjusted to obtain the desired reverse recovery current. The storage time is the time from the beginning of the reverse current transition to the time when the reverse current begins to decay toward its dc value. An example of a typical measurement waveform is shown in figure II-36.

4) Example - 1N914

The reverse recovery time information given by Lumatron (figure II-4) is in a form that can be applied directly. Assuming that the reverse recovery time is approximately equal to storage time,

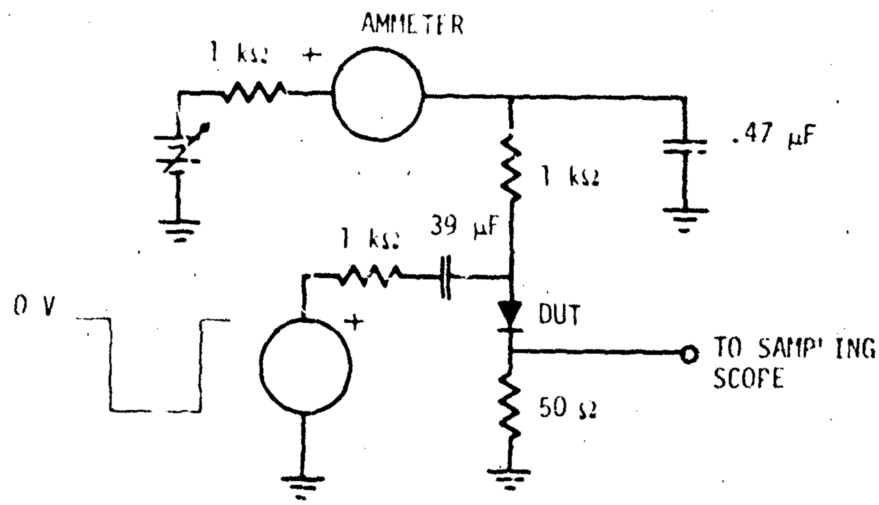


Figure II-35. Diode Storage Time Test Circuit

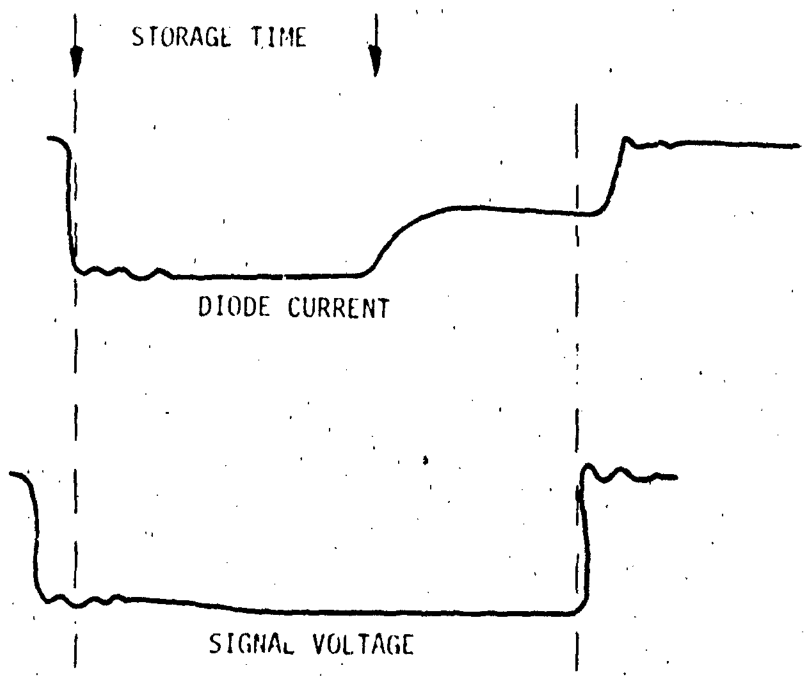


Figure II-36. Diode Storage Time Waveform

$$F = \frac{\ln\,(1 + 10\ \text{mA}/10\ \text{mA})}{2\pi\,(8\ \text{ns})} = 1.38 \times 10^{7}\ \text{hertz}$$

t_{cs} can now be found as·

$$t_{cs} = \frac{1}{2\pi\,(1.38 \times 10^{7}\ \text{Hz})} = 1.15 \times 10^{-8}\ \text{seconds}$$

g. Computer Examples

To verify the charge storage features of the diode model, a simulated storage time circuit was encoded The diode frequency parameter may be computed from the simulated storage time. This frequency parameter may be compared to the frequency parameter used to develop the model.

The storage time test circuit was simulated by use of the SPICE computer code. The storage time test circuit is illustrated in figure II-37. The input listing for this run is given in figure II-38. The test circuit output is listed in figure II-39. The output parameter is the voltage at node 6 which is designated by asterisks. This voltage is across 50 ohms; therefore, the diode current is known.

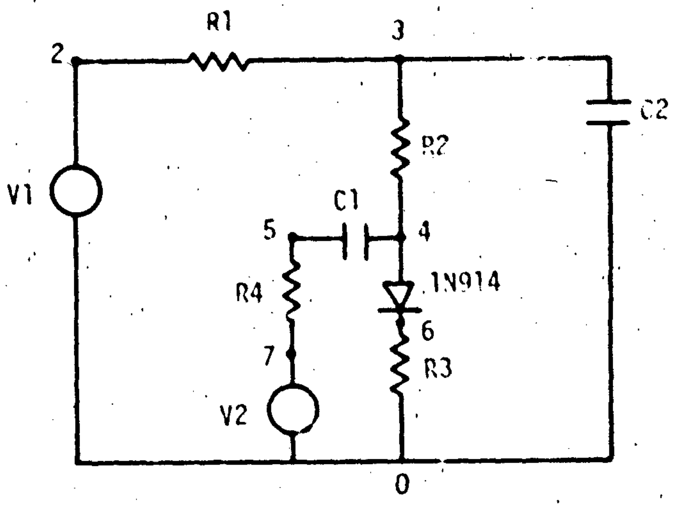


Figure II-37. Diode Storage Time Test Circuit

```
***** 02/24/78 ******** SPICE 2G.2 (26SEP76) ******** 13.06.24.*****

*LEVEL 2 DIODE TRANSIENT TEST

    INPUT LISTING                      TEMPERATURE =   27.000 DEG C

*******************************************************************


R1 2 3 1K
R2 3 4 1K
R3 6 0 50.
R4 7 5 1K
C1 5 4 .39E-6
C2 3 0 .47E-6
V1 2 0 20.5
V2 7 0 PWL(0 0 10.E-9 0 11.E-9 -22 20.E-9 -22)
DIODE 4 6 X
.MODEL X D(IS=1.21E-9 RS=0.464 N=1.76 TT=1.15E-8 CJO=1.37E-12 PB=0.6
*          M=0.0181)
.TRAN 1NS 50NS
.PLOT TRAN V(7) V(5)
.END
```

Figure II-38. Storage Time Test Listing

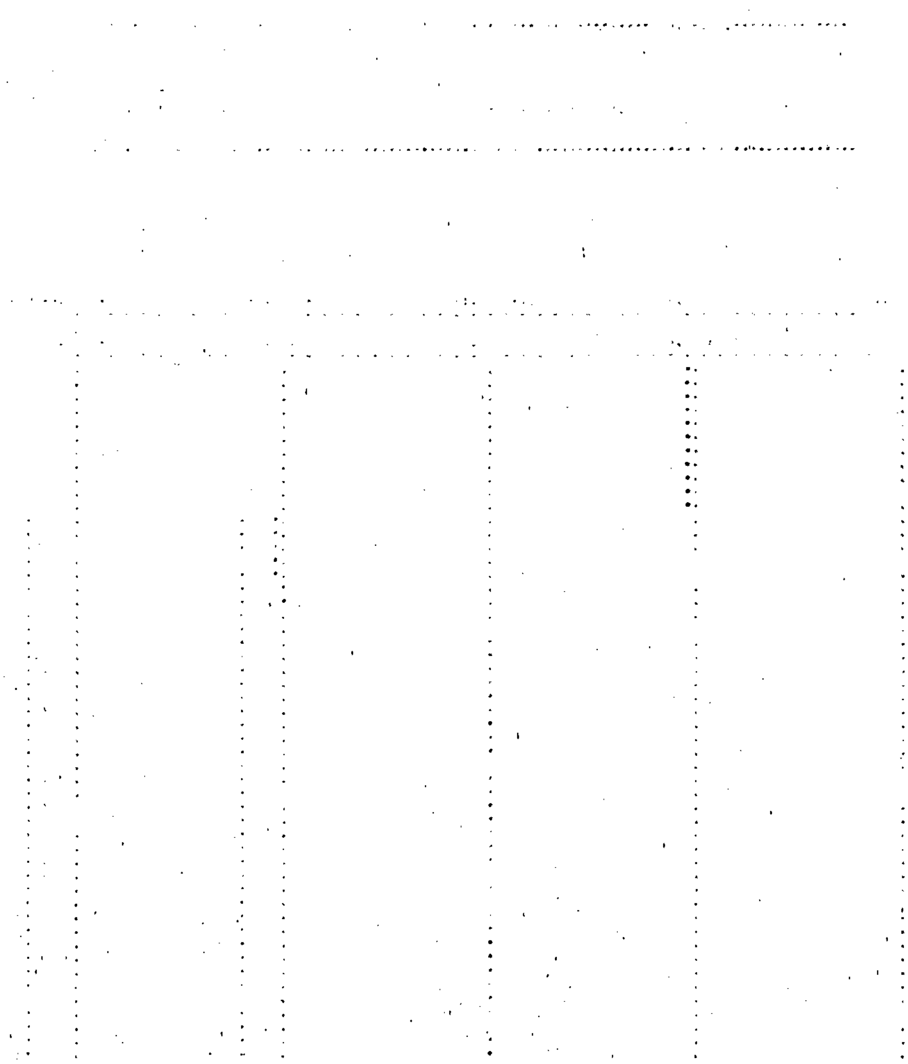


Figure II-39. Simulated Storage Time Waveform

The diode forward current, I_F, is about:

$$I_F = \frac{0.5\ V}{50\ \Omega} = 10\ mA$$

The diode transient reverse current, I_R , is about:

$$I_R = \frac{0.5\ V}{50\ \Omega} = 10\ mA$$

The storage time can be seen to be about 8 ns. The frequency parameter, F, can now be calculated as:

$$F = \frac{\ln\ (1 + 10\ mA/10\ mA)}{2\pi\ (8\ ns)}$$

$$F = 13.8\ MHz$$

The experimental frequency parameter used to develop the diode model is also 13.8 MHz.

8. Photocurrent Effects

a. Description

A P-N diode junction exposed to a pulse of ionizing radiation will produce a photocurrent due to the interaction between the junction and the hole-electron pairs produced by the radiation. The amplitude of the photocurrent is proportional to the dose rate of the radiation exposure and to the volume of the semiconductor contributing hole-electron pairs to the conduction process.

A convenient unit of ionizing radiation is the rad. One rad deposits 100 ergs of energy in 1 gram of the irradiated material. In silicon, 1 rad produces 4×10^{13} hole-electron pairs/cm^3. This constant is the generation rate for silicon.

The diode photocurrent consists of two components. The prompt component consists of electron-hole pairs generated within the depletion volume at the metallurgical junction. Carriers produced in

this volume are immediately swept out by the high electric field which exists in this region. Nonequilibrium minority carriers produced in the quasineutral region bordering the depletion region may be swept across the junction if the carriers can reach the depletion region edge before recombining. The average distance minority carriers travel before recombination is called the diffusion length. The delayed photocurrent component will consist of generated minority carriers produced within one diffusion length of the depletion region edge. A time delay occurs due to the finite time required for the minority carriers to reach the depletion region.

A complication arises in that the behavior of minority carrier electrons differs from minority carrier holes. The photocurrent expressions presented make the simplifying assumption that only one type of minority carrier dominates the photoresponse.

The physical parameters required to predict photocurrent are best determined from knowledge of the device material and geometry. Since such information is not normally available, methods for estimating physical parameters from terminal measurements are given. Such techniques must be regarded as only "best guesses" to be made in the absence of other sources of information.

b. Advantages

Evaluation of the photocurrent expressions allows the detailed prediction of photoresponse for complex electronic circuits. Experimental photocurrent inclusion allows a quick and simple method of transient response analysis.

c. Cautions

For dose rates greater than 1×10^9 rad (Si)/sec, photocurrent amplitudes do not necessarily scale linearly with increasing dose rate. Therefore, experimental data are usually necessary to accurately model photoresponse in this region. Also, the diffusion component of photocurrent is highly dependent on minority carrier lifetime. Since lifetime is difficult to determine, purely theoretical predictions of photocurrent amplitude and decay times are not reliable at any dose rate.

d. Characteristics

The placement of the photocurrent generator in the diode model is illustrated in figure II-40.

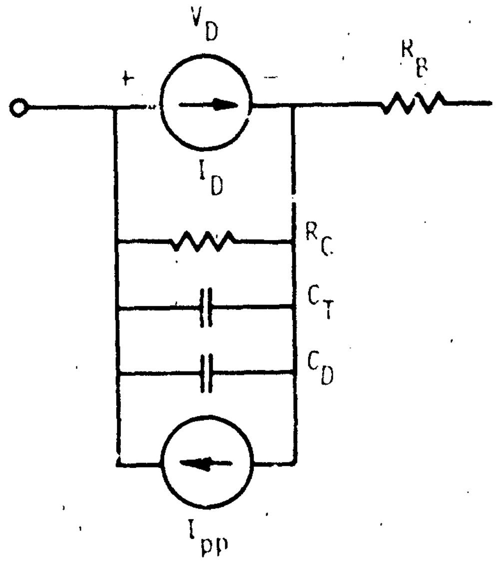


Figure II-40. Photocurrent Inclusive Diode

e. Defining Equations

Four descriptions of the photocurrent generator are considered:

(1) Piecewise linear table describing photocurrent from experimental data. This method has the advantage of accuracy and ease of implementation. The main disadvantage is the lack of flexibility.

(2) Wirth and Rogers (ref. II-2) have performed an evaluation of photocurrent for a rectangular pulse width with the following result.

$$I_{pp}(t) = \dot{\gamma} q\, gA \left\{ \left[W + L \operatorname{erf} (t/\tau)^{\frac{1}{2}} \right] U(t) - \left[W + L \operatorname{erf} \left(\frac{t - t_p}{\tau} \right)^{\frac{1}{2}} \right] U(t - t_p) \right\}$$

(3) For nonrectangular radiation pulses, the photocurrent can be predicted more accurately if a convolution integral is used to relate the time dependent rate of radiation exposure to the photocurrent production.

$$I_{pp} = C\dot{\gamma}p \left[W \left(\frac{\dot{\gamma}(t)}{\dot{\gamma}p}\right) + \frac{L}{\dot{\gamma}p\sqrt{\pi\tau}} \int_0^t \exp\left(\frac{-\lambda}{\tau}\right) \lambda^{-1/2} \dot{\gamma}(t-\lambda)d\lambda \right]$$

(4) Examination of the plots of the Wirth and Rogers equation reveals that the photocurrent waveshapes can often be estimated as a double exponential. This expression is:

$$JP = I_{pp} \left(\exp \left\{ \frac{-A_{MAX1}\left[(t-t_{D2}),0\right]}{\tau_F} \right\} - \exp \left\{ \frac{-A_{MAX1}\left[(t-t_{D1}),0\right]}{\tau_R} \right\} \right)$$

f. Parameter List

I_{pp}	=	the diode photocurrent
W	=	effective depletion region width
L	=	diffusion length
τ	=	minority carrier lifetime
$\dot{\gamma}(t)$	=	time dependent radiation pulse
$\dot{\gamma}p$	=	peak value of radiation pulse
C	=	an empirically determined scaling factor reflecting material and geometric constants
g	=	generation rate in silicon
t_p	=	radiation pulse width
$U(t)$	=	unit step
t_{D2}	=	radiation pulse termination time
τ_F	=	time constant for waveform falling edge
t_{D1}	=	radiation pulse initiation time
τ_R	=	time constant for waveform rising edge
λ	=	dummy variable for integration
t	=	time

g. Parameterization

1) W

a) Definition

W is the width of the depletion region at the metallurgical junction. The value of W is voltage dependent, but a constant approximation may be used.

b) Typical Value

A typical value for W is 1×10^{-4} cm.

c) Measurement

W can be estimated from the values of the breakdown of the junction. By making the assumption that the junction is abrupt and planar, W at the breakdown voltage may be estimated as:

$$W = \left[\frac{2 \varepsilon_s V_{BD}}{q \left(\frac{V_{BD}}{2.72 \times 10^{12}} \right)^{-3/2}} \right]^{1/2}$$

ε = The permittivity of the material (1.04×10^{-12} F/cm for silicon)

The depletion width at zero bias can now be calculated as:

$$W_0 = \frac{W_{VBD}}{\left(1 - \frac{V_{BD}}{\psi} \right)^m}$$

The depletion width at any bias can now be estimated as:

$$W = W_0 \left(1 - \frac{V_D}{\psi} \right)^m$$

d) Example - 1N914

The breakdown voltage of the 1N914 being modeled is 150 volts. The width of the depletion region at this bias is:

$$W = \left[\frac{2\ (1.04 \times 10^{-12}\ F/cm)\ (150\ V)}{\left(1.6 \times 10^{-19}\ C\right)\left(150/2.72\ .\ 10^{12}\right)^{-3/2}} \right]^{1/2}$$

$$\therefore W = 8.94 \times 10^{-4}\ cm \text{ at } V_{BD}$$

$$W_0 = \frac{8.94 \times 10^{-4}\ cm}{\left[1 - \frac{(-150)}{0.6}\right]^{0.0181}} = 8.09 \times 10^{-4}\ cm$$

2) τ

a) Definition

τ is the lifetime of the predominant minority carrier produced by ionizing radiation.

b) Typical Value

A typical value of τ is 10 nanoseconds. A range of 0.1 ns to 1 μs is common.

c) Measurement

An approximation for τ is the charge storage factor, t_{cs}, discussed earlier.

d) Example - 1N914

The value of t_{cs} obtained for the 1N914 from data sheets was 1.15×10^{-8} seconds. Therefore, the estimate of τ is 1.15×10^{-8} seconds.

3) L

a) Definition

L is the diffusion length of the predominant minority carrier. It is the average distance a carrier will diffuse before recombining.

b) Typical Value

A typical value for L is 10 μm. The maximum value of L is of the order of 1 cm in undoped silicon. Minimum values are less than 1 μm.

c) Measurement

L can be determined from the expression

$$L = \sqrt{D\tau}$$

where D is the carrier diffusion constant. At room temperature, the electron diffusion constant varies from approximately 30 cm^2/sec to 35 cm^2/sec, depending on the doping level. The corresponding hole diffusion constants are 12 and 11. Because the variations of D_n and D_p are small in the range of interest, they may be chosen as constants. If it is not known whether electrons or holes are the predominant minority carrier, several facts may help:

(1) The substrate material into which the diffusion was made generally determines the predominant minority carrier. The dominant carriers will be electrons if the substrate is P-type, or holes if N-type.

(2) Planar process diodes are generally produced using N-type substrates.

d) Example - 1N914

Since no details about the 1N914 substrate are readily available, an N-type substrate will be assumed. A diffusion constant of 12 cm^2/sec will be chosen. L can now be solved for as:

$$L = \sqrt{(12\ cm^2/sec)(1.15 \times 10^{-8})\ sec}$$

$$L = 3.71 \times 10^{-4}\ cm$$

4) C

a) Definition

C is an empirically determined constant which scales the value of predicted photocurrent to correspond to actual observed levels.

b) Typical Value

The theoretical value of C is 6.46×10^{-6} times the area (cm^2) of the diode.

c) Measurement

If radiation data are not available,

$$C = A\ q\ g_o$$

If radiation data are available,

$$C = \frac{I_{pp}\ (\text{steady state})}{(W + L)\ \dot{\gamma}\ (\text{steady state})}$$

d) Example - 1N914

Experimental photocurrent data from measurements for a 1N914 are shown in table II-5.

TABLE II-5   MEASURED PHOTOCURRENTS FOR 1N914

$V_D = -60$ V

$\dot{\gamma}$	I_{pp}
1.16 x 10"	100 mA
1.59 x 10"	100 mA
1.67 x 10"	80 mA
2.03 x 10"	120 mA
2.53 x 10"	100 mA
2.50 x 10"	100 mA

W at -60 V is:

$$W = 8.09 \times 10^{-4}\left[1 - \frac{(-60\ \mathrm{V})}{0.6\ \mathrm{V}}\right]^{0.0181}$$

$$W = 8.79 \times 10^{-4}\ \mathrm{cm}$$

Applying the approximation

$$C = \frac{I_{pp}}{\dot{\gamma}\,(W + L)}$$

yields the results shown in table II-6.

TABLE II-6. DETERMINATION OF C

$\dot{\gamma}$	C
1.16 x 10"	6.90×10^{-10}
1.59 x 10"	5.03×10^{-10}
1.67 x 10"	3.83×10^{-10}
2.03 x 10"	4.73×10^{-10}
2.53 x 10"	3.16×10^{-10}
2.50 x 10"	3.20×10^{-10}

$\bar{C} = 4.48 \times 10^{-10}$

The theoretical value for C is:

$$C = (1.6 \times 10^{-19}\ C)(4 \times 10^{13}/rad)(1.29 \times 10^{-4}\ cm)$$

$$C = 8.26 \times 10^{-10}$$

5) t_{D2}, τ_F, t_{D1}, τ_R

a) Definition

t_{D1} and τ_R are, respectively, the radiation pulse initiation time and the time constant for the rising edge of the photocurrent. Similarly, t_{D2} and τ_F are the pulse termination time and the time constant for the falling edge.

b) Measurement

t_{D2}, τ_F, t_{D1}, and τ_R can be found by examination of the photocurrent waveform as illustrated by figure II-41.

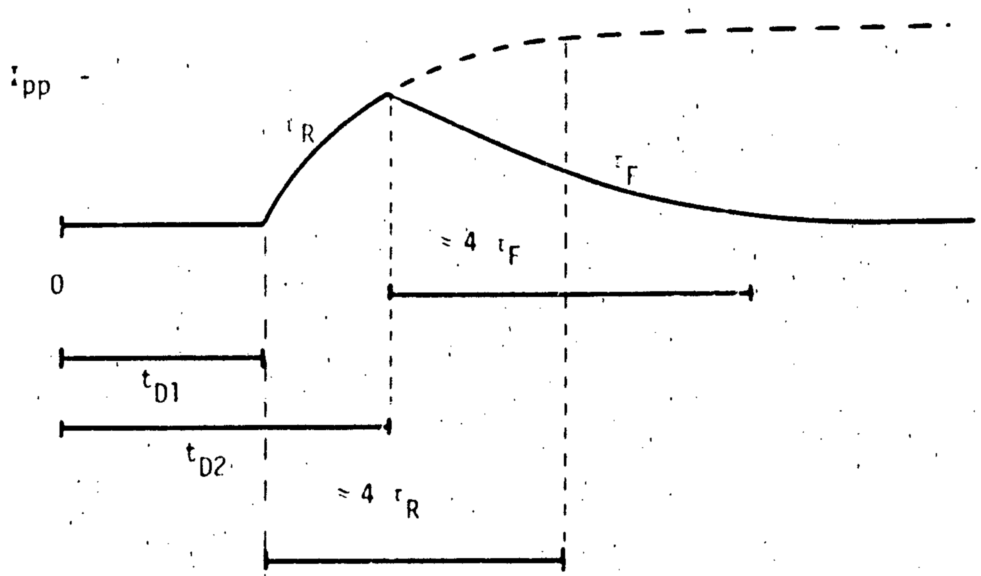


Figure II-41. Photocurrent Waveform

The rise- and falltime constants may be estimated by recalling that an exponential reaches 98 percent of the steady state value in four time constants.

h. Implementation Notes

The error function may be approximated by using the following expansion of erf.

$$\operatorname{erf} X = 1 - \left(1 + B_1X + B_2X^2 + B_3X^3 + B_4X^4\right)^{-4}$$

where:

$B_1 = 0.278394$
$B_2 = 0.230388$
$B_3 = 0.000973$
$B_4 = 0.078108$

error $< 2.5 \times 10^{-4}$

A subroutine which implements the convolution integral photocurrent solution is very useful for photocurrent predictions. Subroutine PPC (ref. II-3), shown in figure II-42, may be used to compute a photocurrent waveform for input into a circuit analysis code as a table.

i. Computer Example

The PPC subroutine was applied to predict the photoresponse of a diode exposed to a peak dose rate of 1.16×10^{10} rad (Si)/sec (estimated by dosimetry). The test was made at zero volts bias and the ionizing waveform was estimated to be as in figure II-43.

```
SUBROUTINE [illegible]
COMMON [illegible]
COMPUTES THE PRIMARY PHOTOCURRENT THAT FLOWS
IN A DIODE [illegible] TO EXPOSURE TO GAMMA RADIATION

INPUTS THAT [illegible] THE JUNCTION MATERIAL ARE
[illegible].....MINORITY CARRIER DIFFUSION CONSTANT
       [illegible]
TA.....MINORITY CARRIER LIFETIME (NANOSECONDS)
W......JUNCTION DEPLETION WIDTH (CM)
       TYPICAL [illegible] (4)
ST.....TRANSIENT ANALYSIS STOP TIME (NSEC)

TWO [illegible] ROUTINES ARE REQUIRED
GAMDOT.....USER SUPPLIED ROUTINE THAT DEFINES
THE INPUT GAMMA PULSE AS A FUNCTION OF TIME.
THE PULSE SHOULD HAVE A PEAK VALUE OF 1.0.
ERF.......THIS ROUTINE PROVIDES THE VALUE OF
THE STANDARD ERROR FUNCTION.

OUTPUT IS THE PRIMARY PHOTOCURRENT STORED IN
THE ARRAY PPC(I) FOR N TIME POINTS WHOSE VALUES
ARE STORED IN THE ARRAY T(I) EVENLY SPACED FROM
0.0 TO ST. TIME [illegible] IS IN UNITS OF NSEC.
PHOTOCURRENT [illegible] IS IN UNITS OF AMPERES AFTER
[illegible] BY [illegible] PEAK GAMDOT WHERE
Q..............ELECTRONIC CHARGE (PICOCOULOMBS)
GO.............CARRIER GENERATION CONSTANT
                (HOLE-ELECTRON PAIRS/(RAD(SI)*CM**3))
A.............. JUNCTION AREA (CM**2)
PEAK GAMDOT....CONSTANT (RADS/SEC)

DIMENSION [illegible](2000),[illegible](2000),FF(2000)
DIMENSION T(2000),[illegible](2000)
[illegible]
DATA N/[illegible]/
[illegible]
[illegible]
[illegible]
[illegible]
DO 10 I=1,N
TIME=[illegible]
T(I)=TIME
[illegible]
[illegible]
[illegible]
FF(I)=ERF([illegible]/TA))
10 CONTINUE
DO 40 I=1,N
[illegible]
DO 20 J=1,I
K=I-J
[illegible]
20 CONTINUE
PPC(I)=[illegible]*TA))/1000.0
40 CONTINUE
RETURN
END
```

Figure II-42. Subroutine PPC

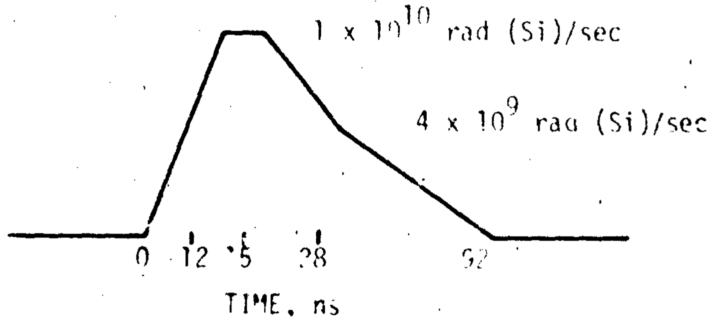


Figure II-43. Ionizing Waveform

The computer listing for the prediction is given in figure II-44. The results of this program are plotted in figure II-45. A comparison with the actual test, figure II-46, shows agreement within 50 percent. The predicted peak photocurrent was about 8 mA· the experimental peak photocurrent (at a current probe response of 5 mV/mA) was 14.4 mA.

9. Neutron Effects

a. Description

Displacement damage produced by neutron irradiation destroys the crystalline structure of the semiconductor altering the electrical behavior of the material. There is a tendency for the crystalline structure to reorder itself under the influence of time, temperature, and bias. Hence, the fluence dependent electrical characteristics tend to recover (anneal) toward their preirradiation level under the influence of time and temperature. This process tends to occur more rapidly at short times after exposure (rapid annealing) if current densities are high. The analyst should determine if short term, post exposure predictions or longer term problems are to be considered.

The neutron flux is the number of particles per second passing through a sphere of unit cross-sectional area. For a normal beam, the sphere would reduce to planar area of unity. Fluence is the

```
      COMMON PPI(300),T(300)
      [illegible]
      TA=[illegible]
      W=4.0E-4
      STPTM=100.0
      CALL PPC(D,TA,W,STPTM)
      PRINT 3
    3 FORMAT (1H1[illegible]TIME-NS[illegible]PP-AMPS)
      DO 1 I=1,100
      PPI(I)=PPI(I)*[illegible]E-7*[illegible]E13*1.29E-4*1.15E1
      PRINT 2,T(I),PPI(I)
    2 FORMAT ([illegible]E10.3)
    1 CONTINUE
      STOP
      END
      SUBROUTINE PPC(D,TA,W,STPTM)
      COMMON PPI(300),T(300)
C     COMPUTES THE PRIMARY PHOTOCURRENT THAT FLOWS
C     IN A DIODE DUE TO [illegible] GAMMA RADIATION
C
C     INPUTS THAT DEFINE THE JUNCTION MATERIAL ARE
C     D.....MINORITY CARRIER DIFFUSION CONSTANT
C           [illegible] FOR N-TYPE, [illegible] FOR P-TYPE)
C     TA....MINORITY CARRIER LIFETIME (NANOSECONDS)
C     W.....JUNCTION DEPLETION WIDTH (CM)
C           [illegible] TO [illegible] (CM)
C     STPTM...TRANSIENT ANALYSIS STOP TIME (NSEC)
C
C     TWO FUNCTION ROUTINES ARE REQUIRED
C     GAMP.......[illegible] ROUTINE THAT DEFINES
C     THE INPUT GAMMA PULSE AS A FUNCTION OF TIME.
C     THE PULSE SHOULD HAVE A PEAK VALUE OF 1.0.
C     ERF.......THIS ROUTINE PROVIDES THE VALUE OF
C     THE STANDARD ERROR FUNCTION.
C
C     OUTPUT IS THE PRIMARY PHOTOCURRENT STORED IN
C     THE ARRAY [illegible] N TIME POINTS WHOSE VALUES
C     ARE STORED IN THE ARRAY T(I) EVENLY SPACED FROM
C     [illegible] TIME T0 IS IN UNITS OF NSEC.
C     PHOTOCURRENT WILL BE IN UNITS OF AMPERES AFTER
C     MULTIPLICATION BY [illegible] WHERE
C     Q............ELECTRONIC CHARGE (MICROCOULOMBS)
C     G............CARRIER GENERATION CONSTANT
C                  [illegible] PAIRS/(RAD-CM**3))
C     A............JUNCTION AREA (CM**2)
C     PEAK GAMDOT...[illegible] (RADS/NSEC)
C
      DIMENSION [illegible]
      [illegible]
      [illegible]
      DATA [illegible]
      [illegible]
      [illegible]
      [illegible]
      [illegible]
   10 CONTINUE
      [illegible]
      RETURN
      END
      FUNCTION ERF(X)
      [illegible](1.0+0.[illegible]*X+0.2303[illegible]*X+0.000[illegible]+0.078[illegible]
     [illegible]
      RETURN
      END
      FUNCTION GAMP(TIME)
      [illegible]
      IF [illegible]
      IF [illegible]
      IF [illegible]
      IF [illegible]
      IF [illegible]
      RETURN
      END
```

Figure II-44. Photocurrent Prediction Listing

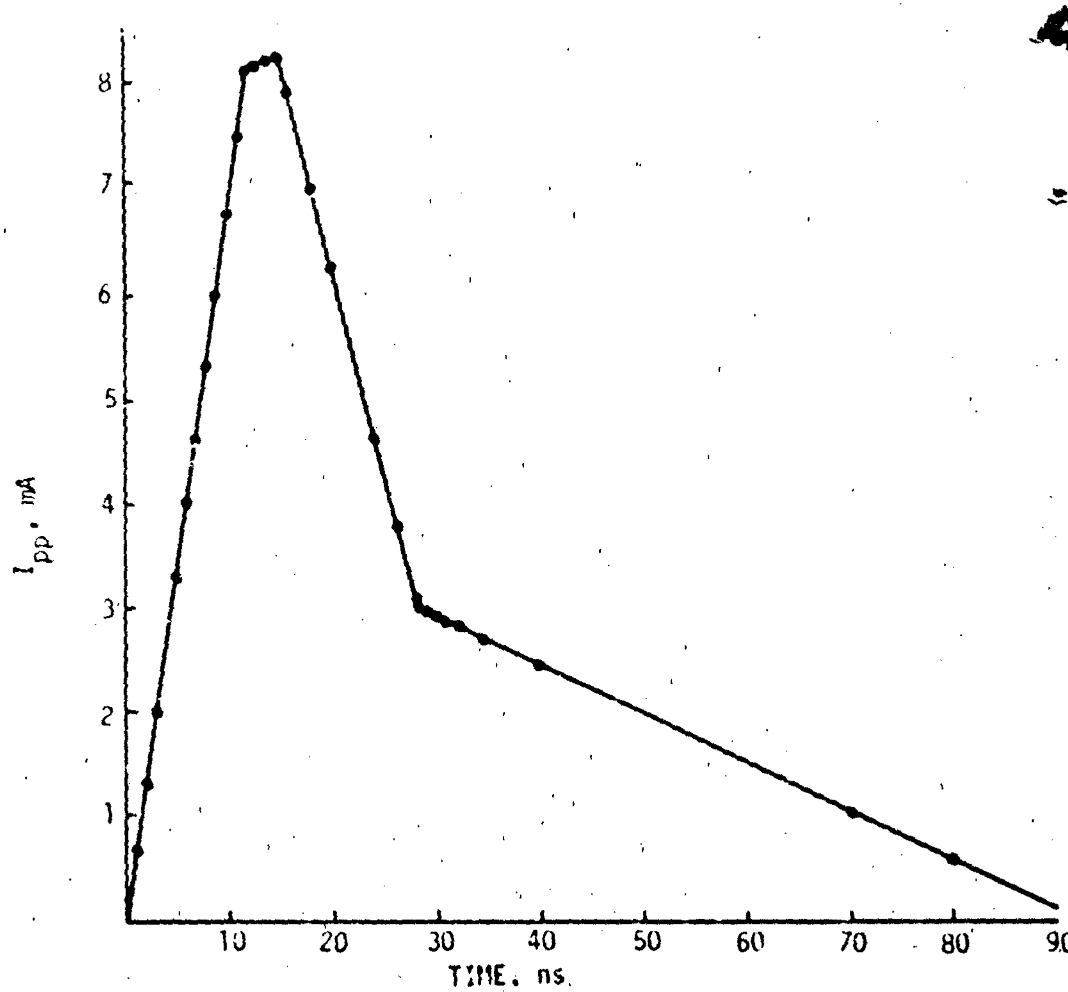


Figure II-45. Predicted Photocurrent

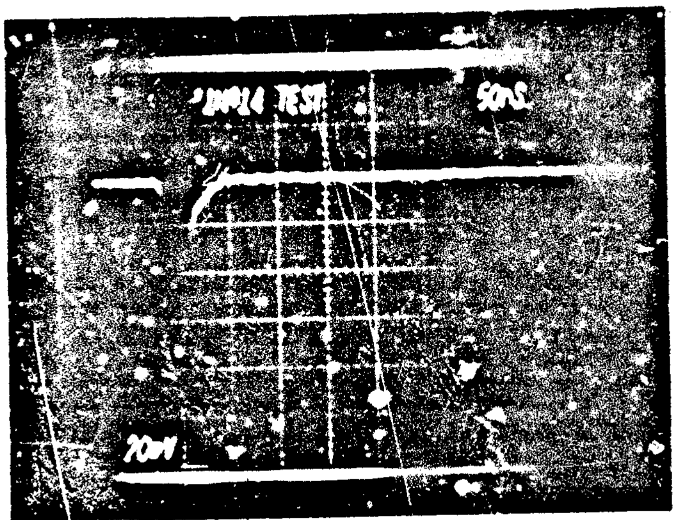


Figure II-46. Experimental Photocurrent

time integral of flux and has units of neutrons/cm^2. The amount of damage produced by a neutron exposure is also a function of the energy spectrum of the neutrons. The modeling procedures discussed here assume that the analyst has been provided with the equivalent neutron fluence in terms of neutrons with energies of 1 MeV.

The three major effects of neutron damage on semiconductor devices are:

(1) Increased density of recombination centers resulting in a decrease in minority carrier lifetime and increased generation currents.

(2) A carrier removal effect which effectively "counter-dopes" the semiconductor, resulting in more lightly doped regions. This in turn causes the equilibrium majority carrier concentration to decrease and the equilibrium minority carrier concentration to increase.

(3) Mobility decreases due to the increased damage.

The effect of this damage will be to increase the diode leakage, emission constant, and bulk resistivity. For those diodes having extremely low breakdown voltages, where the breakdown is the result of band-to-band tunneling, the introduction of additional generation-recombination centers can lower the breakdown voltage. Diodes with high breakdown voltages may exhibit carrier removal effects which result in resistivity increases. Minority carrier lifetime degradation may result in a decrease in the diffusion capacitance of diodes which originally had long storage times. To model these effects, variations may be required in values for I_S, R_C, C_D, and M.

b. Advantages

Inclusion of neutron damage effects on model parameters permits the analyst to predict circuit degradation as a result of neutron exposure

c. Cautions

Experimental data are the most reliable source of neutron degradation information. However, neutron irradiation facilities are not

available to most analysts. The CRIC data base (ref. II-4) provides post exposure characteristics of some device types. It should be used as the second most desirable source of data. Neutron degradation theory is generally quite sophisticated. However, some knowledge of preirradiation minority carrier lifetime (τ) is generally required in order to apply the theory. Since τ is difficult to determine, the results of theoretical predictions should only be considered approximations.

d. Characteristics

The topology required for the neutron susceptible diode is illustrated in figure II-47.

A typical pre- and postirradiation diode characteristic is illustrated in figure II-48.

e. Defining Equations

For recombination rate per carrier:

$$R = R_o + k\phi$$

There are no exact values of k. However, typical values are 4×10^{-6} to 6×10^{-6} $cm^2/n\text{-}s$ for P-type silicon and 6×10^{-6} to 9×10^{-6} $cm^2/n\text{-}s$ for N-type silicon.

For impurity concentration:

$$N = N_o - \phi \frac{dN}{d\phi}$$

$dN/d\phi$ is the carrier removal rate and usually lies between 1.5 and 3.0 carriers/n-cm for P-type silicon and 1.0 and 4 carriers/n-cm for N-type silicon.

Other relevant expressions are:

$$\frac{1}{\tau} = \frac{1}{\tau_o} + \frac{\phi}{k_\tau}$$

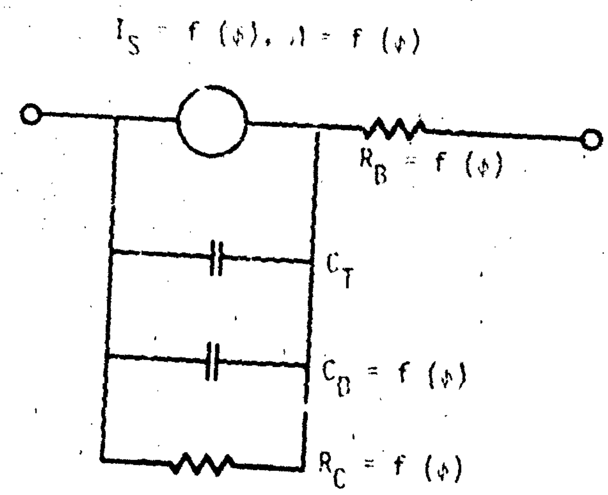


Figure II-47. Topology for Neutron Susceptible Diode

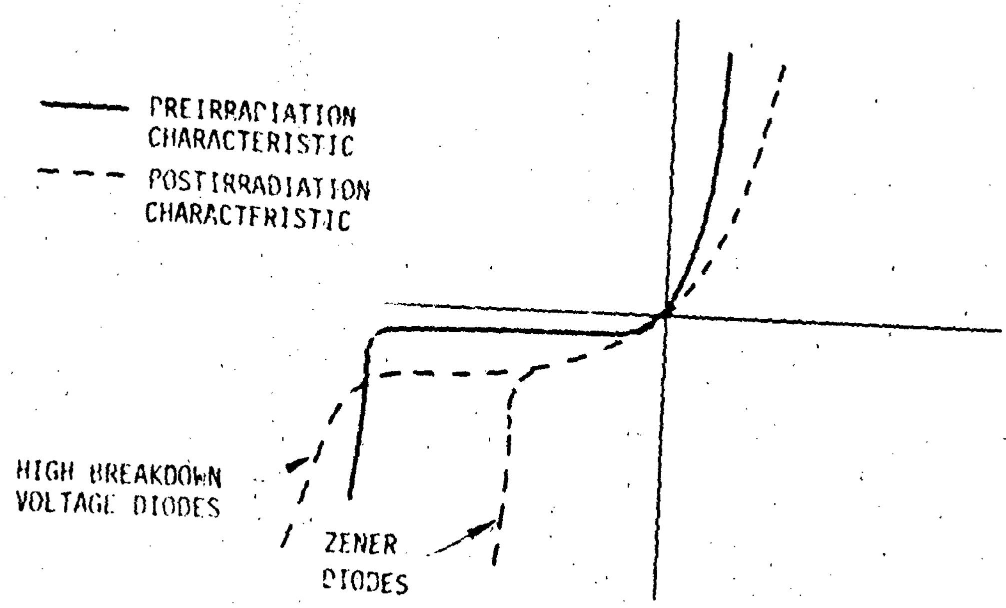


Figure II-48. Pre- and Postirradiation Diode Characteristics

which is obviously related to the recombination rate, and

$$\mu = \mu_0 - \phi \frac{d\mu}{d\phi}$$

Mobility changes are usually insignificant relative to other effects.

10. Burnout

a. Description

A nuclear event produces large amounts of electromagnetic energy which may be coupled to an electronic circuit. The large transient voltages and currents produced by the EMP (electromagnetic pulse) may produce catastrophic failure of semiconductor devices by destructive heating of the above device. Junctions usually fail while being pulsed in the reverse biased mode due to the higher power dissipations possible. This implies that reverse breakdown must be included in the model if an EMP assessment of the circuit is to be made.

Electrical overstress may produce a failure of a forward biased junction. Because of the lower voltage drops associated with a forward biased junction, much higher current levels are required to fail a forward biased junction as opposed to a reverse biased junction. Because of the high current levels, voltage drops along the bulk regions of the diode become important. Forward bias failures can be predicted in a similar manner as reverse biased failures if the general form of the Wunsch expression is applied. It has been observed that the Wunsch constant for the forward region is roughly 10 times the Wunsch constant for the reverse region.

Metallization failures may become important for MOS integrated circuits and other circuits which utilize narrow metallization due to low power requirements. The failure is due to the destructive ohmic heating of the metallization interconnects. Often, the failure will occur at an oxide step on the circuit because of thin films which form at the step. Metallization failure has been observed after device destruction when the junction shorts due to heating. If overstress test data

are not available to indicate the nature of the failure mode of a device, metallization failure should not be considered a likely occurrence unless MOS or low power integrated circuits are being considered.

Two procedures are established for modeling junction burnout. One is based on the average power delivered to a junction and is suitable for rectangular overstress pulses. The other procedure is based on a thermal analogy model and is suitable for any waveshape.

The most straightforward procedure for modeling the failure characteristics is to:

(1) Monitor the current and voltage for the device of interest.

(2) Compute an average power.

(3) Compare the calculated power to the calculated failure threshold given by $P = K_w t^{-1/2}$

where:

P = failure power

K_w = device damage constant (Wunsch constant)

t = overstress pulse width

The thermal analog circuit allows the prediction of burnout from codes which have no subroutine capability. The one dimensional lumped element for heat flow is shown in figure II-49. Since junction power is the known thermal quantity, the electrical analogy of the heat source should be a current source. When the temperature (voltage) of the analog circuit rises above some failure temperature, a simulated device failure occurs.

The literature suggests several possible failure temperature criteria, one of which, the intrinsic temperature, is that temperature at which the intrinsic carrier concentration becomes equal to the semiconductor doping density.

b. Advantages

A power monitoring subroutine or thermal analog allows the analyst to examine the possibility of device failure.

THERMAL	ELECTRICAL
Power (energy flow) (watts)	Current (amps)
Temperature (°C referenced to room temperature)	Voltage (volts)
Energy (joules)	Charge (coulomb)
Resistance (watts/°C)	Resistance (volts/amp or ohm)
Heat Capacity (joules/°C)	Capacitance (coulomb/volt)

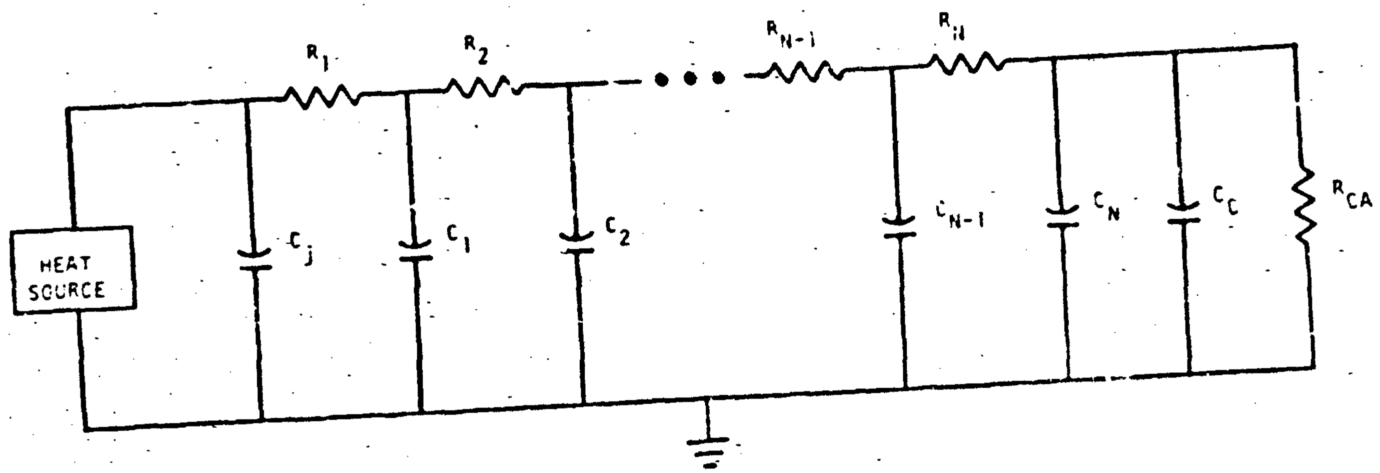


Figure II-49. One Dimensional Lumped Element Model of Heat Flow

c. Cautions

Knowledge of the damage constant, K, is required for the device to be analyzed. For the thermal analog circuit, knowledge of the device failure temperature is needed. Inclusion of a power monitoring subroutine or thermal analog will increase the complexity of an analysis.

d. Characteristics

A typical waveform of a device subjected to a destructive step voltage is illustrated in figure II-50.

e. Defining Equations

$$P_{FAIL} = K_w \, t^{-1/2}$$

f. Parameterization (K_w)

1) Definition

K_w is the constant which relates the power required to fail a diode to the time the power is applied.

2) Typical Value

A typical value of K is 0.1 watt-sec$^{1/2}$. The value of K_w depends on device area and fabrication details.

3) Measurement

K can be determined by applying rectangular voltage pulses to reverse biased diodes. The pulse length should be varied between 100 ns and 100 μs. The pulse amplitude is gradually increased until the device does not meet its specifications. K is then calculated as:

$$K = IV\sqrt{t}$$

where:

I = the failure current level

V = the failure voltage level

t = the failure time

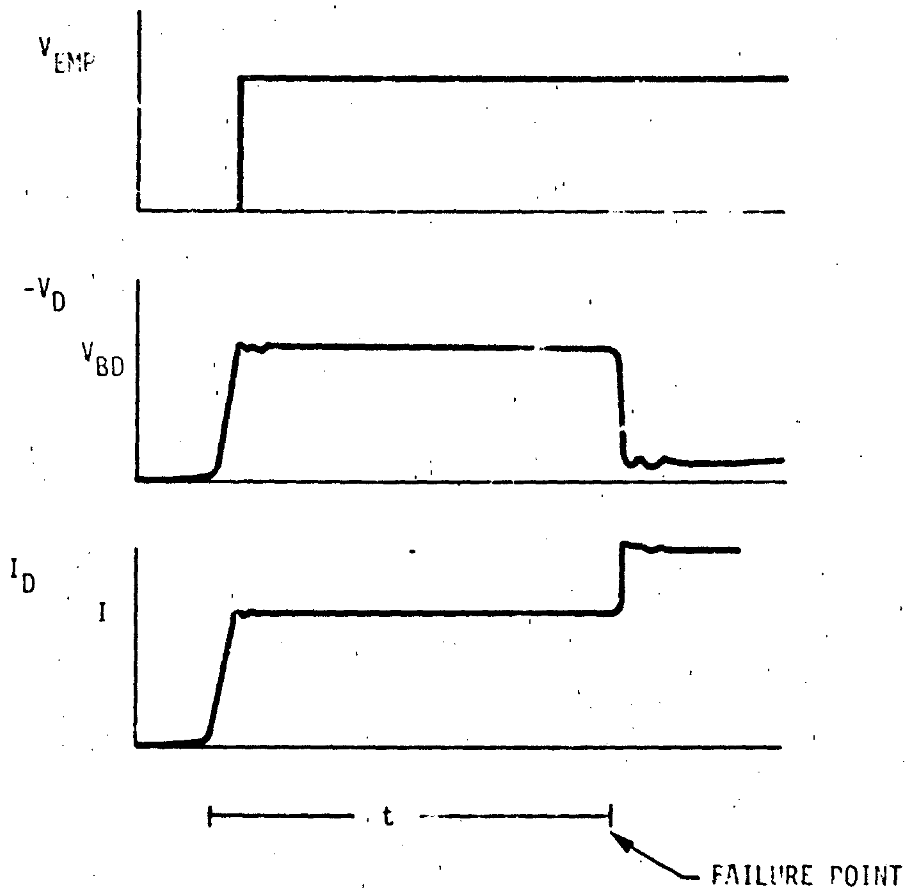


Figure II-50. Device Failure Waveforms

At least six devices should be tested at 3 pulse widths to obtain an average value of K_w.

4) Example - 1N914

The Wunsch constant for the 1N914 was obtained through published experimental results. The experimental values of K_w obtained were:

7.2×10^{-2} watt-sec$^{1/2}$

2.1×10^{-1} watt-sec$^{1/2}$

9.6×10^{-2} watt-sec$^{1/2}$

$\bar{K}_w = 0.126$ watt-sec$^{1/2}$

g. Implementation Notes

The average power model for detecting semiconductor damage is contained in the FORTRAN subroutine FBURN. FBURN is included in the computer example of the following section.

h. Computer Example

As an example of the implementation of a power monitoring subroutine, FBURN, the 1N914 diode model was subjected to 0.3 amps reverse bias as shown in figure II-51. Since the breakdown voltage was 150 volts and the K for this test was 0.126 watt-sec$^{1/2}$, the failure time should be:

$$t = \left[(0.3\ \text{A})(150\ \text{V})/0.126\ \text{watt-sec}^{1/2}\right]^{-2}$$

$$t = 7.84\ \mu\text{s}$$

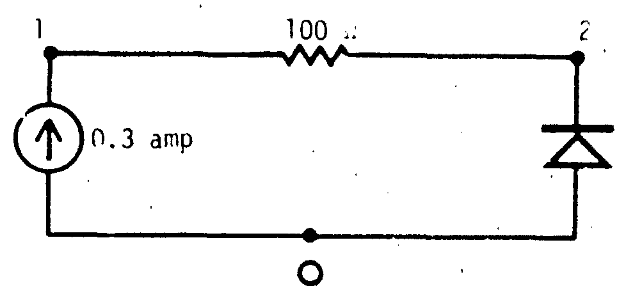


Figure II-51. Burnout Simulation Circuit

The listing for this test, including FBURN, is given in figure II-52. The failure flag produced by FBURN is shown in figure II-53. The failure time indicated by FBURN is 7 μs.

11. Total Dose Effects

The accumulated ionizing dose damages semiconductor surfaces. The ionizing radiation produces positive charge within the oxide at the semiconductor surface. The number of surface energy states is increased. The total dose effect on planar diodes is to produce a junction leakage term which may be large relative to the initial leakage but usually less than 100 nA.

12. Code Implementation

Circuit analysis computer codes differ in nomenclature and details of model formulation. The purpose of this section is to present a table which will allow the analyst to convert the modeling handbook parameters to a form acceptable to several network analysis codes.

The computer programs chosen are codes which have found much utility as tools to study the radiation response of electronic circuits and systems. These codes are CIRCUS 2, TRAC, SCEPTRE, NET-2, and SPICE.

Column one of the conversion table, table II-7, contains the symbols of model parameters as developed by the modeling handbook and the units used to form a consistent set. The following columns list the equivalent parameter for a computer code. The symbology and preferred units of the code are given. The last column is a list of typical, conservative parameter values which may be applied in the event of an

```
S C E P T R E   NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2        5/76
 02/27/78     16.50.4?.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD  "DOCUMENT"  AS THE FIRST CARD
OF THE INPUT TEXT



COMPUTER TIME ENTERING SETUP PHASE-
          CPA        .388 SEC.
          PP        0.000 SEC.
          IO        0.000 SEC.


SUBPROGRAM
      FUNCTION FBURN(AD,TIME,PAVE,PFAIL,I,V,TE,A,B)
C     THIS SUBROUTINE MONITORS POWER IN A JUNCTION AND FLAGS FAILURE.
C     FAILURE IS DEFINED BY P=AT**(-B) USING AVERAGE POWER.
C     PAVE = AVERAGE POWER. PFAIL = FAILURE POWER. FBURN = PAVE/PFAIL
C     I,V,A,B SHOULD ALL REFER TO JUNCTION VALUES OR OVERALL VALUES.
C     I,V,A,B MAY REFER TO EITHER FORWARD OR REVERSE POLARITIES.
C      V= VOLTAGE, I= CURRENT
C     A,B ARE CONSTANTS IN THE FAILURE POWER VERSES TIME RELATIONSHIP.
      REAL I
C     AD IS INTEGER IDENTIFYING JUNCTION AND POLARITY TO BE EVALUATED.
      DIMENSION OLDP(20),OLDT(20),OLDE(20),OLDF(20)
      MAXMOD = 20
C     TO INCREASE NUMBER OF BURNOUT MODELS AVAILABLE,
C     INCREASE ALL DIMENSIONS AND MAXMOD EQUALLY.
C     THIS MODEL ASSUMES P=AT**(-B) FOR 0..LT.T-TE.LE.TMAX
      TMAX = 500.E-6
      P = I*V
C     FR IS THE RATIO OF AVERAGE POWER/FAILUER POWER DEFINED AS FAILURE
      FR = 1.
      ID = INT(AD)
      IF((ID.GT.MAXMOD).OR.(ID.LT.1)) GO TO 10
      IF(TIME.LE.TE) GO TO 20
      IF(TIME.LT.OLDT(ID)) GO TO 20
      IF(TIME.GT.TMAX) GO TO 20
C     TRANSIENT HAS STARTED AND
C     POINT AT TIME = OLDT WAS ACCEPTED BY ERROR CRITERIA.
      OLDE(ID) = OLDE(ID) + (P+OLDP(ID))*(TIME-OLDT(ID))/2.
      PAVE = OLDE(ID)/(TIME-TE)
      PFAIL = A*(AMAX1(TIME-TE,0.)**(-B))
      FBURN = PAVE/PFAIL
      IF(OLDF(ID).GT.FR) GO TO 5
      IF(FBURN.GT.FR) PRINT 100,ID,TIME,PAVE,PFAIL
      OLDF(ID) = FBURN
    5 CONTINUE
      OLDP(ID) = I*V
      OLDT(ID) = TIME
      RETURN
C     BURNOUT MODEL IDENTIFIER OUT OF RANGE
   10 PAVE = 0.
      PFAIL = 0.
      FBURN = 0.
      PRINT 200,ID
      RETURN
```

Figure II-52. Burnout Test Listing

```
C       TRANSIENT HAS NOT STARTED.
C       OR TIME EXCEEDS VALID INTERVAL FOR P=K/SQRT(T).
   20   OLDP(ID) = 0.
        OLDT(ID) = TE
        OLDE(ID) = 0.
        PFAIL = 0.
        PAVE = 0.
        OLDF(ID) = 0.
        FBURN = 0.
        RETURN
   30   PRINT 300
        STOP
  100 FORMAT(6(/),10X,*ID =*,I5,5X,*FAILURE TIME =*,E17.7,5X,
     1 *AVERAGE POWER =*,E13.3,5X,*THRESHOLD FAILURE POWER =*,E13.3)
  200 FORMAT(10X,*BURNOUT MODEL IDENTIFIER OUT OF RANGE.  ID =*,I5)
  300 FORMAT(10X,*INVALID RESUTLS FROM DAMAGE MODEL*,/,10X,
     1 *RUN TERMINATED.*,/,10X,*RESULTS OF DAMAGE MODEL MAYBE USED *,
     2 *ONLY IN THE OUTPUTS SECTION.*)
CIRCUIT DESCRIPTION
ELEMENTS
JIN,0-1=0.3
RBIAS,1-2=100
JPN,0-2=X9(1.35E-14*(EXP(38.6*VJPN)-1.)+PBD-PI)
C,2-0=1.E-12
DEFINED PARAMETERS
PBD=TABLE 3(VJPN)
PI=TABLE 2(TIME)
PA=0.0
PF=0.0
PIR=X1(AMIN1(JPN,0.))
PVR=X2(AMIN1(VJPN,0.))
PTE=0.0
PK=0.126
PB=0.5
PFR=FBURN(1.,TIME,PA,PF,PIR,PVR,PTE,PK,PB)
FUNCTIONS
TABLE 2
0,0,1.E-3,0
TABLE 3
-152,-60.E-3
-151,-30.E-3
-148,-200.E-6
-147,-100.E-6
-144,-50.E-6
-140,-25.E-6
-120,-10.E-6
-100,-5.E-6
0,0
OUTPUTS
PFR,PLOT
JPN,PLOT(VJPN)
RUN CONTROLS
STOP TIME=10.E-6
MINIMUM STEP SIZE=1.E-39
END

SYSTEM NOW ENTERING SIMULATION
```

Figure II-52. Burnout Test Listing (Concluded)

```
COMPUTER TIME ENTERING SIMULATION-
        CPA      3.582 SEC.
        PP       0.300 SEC.
        IO       0.300 SEC.


        ID =    1    FAILURE TIME =    .69052565-05    AVERAGE POWER =    .480E+02    THRESHOLD FAILURE POWER =    .479E+02
```

Figure II-53. FBURN Flag

TABLE II-7. CODE IMPLEMENTATION

MODELING HANDBOOK	CIRCUS 2	TRAC	SCEPTRE*	NET-2	SPICE	"SAFE" DEFAULT VALUES
R_B (Ω)	RB (Ω)	-	RB (kΩ)	RB (kΩ)	RS (Ω)	1×10^{-4}
R_C (Ω)	RS (Ω)	ROL (Ω)	RS (kΩ)	-	-	1×10^{1} [illegible] Ω
C_{jo} (farads)	A (farads)	CDO·VDBI$^{1/2}$ (F)	CO (pF)	C (pF)	CJO (F)	[illegible] pF
φ (volts)	PHI (volts)	VDBI (V)	φ (V)	VZ (V)	PB (V)	0.6 V
m	N	0.5	n	N	M	0.5
I_s (A)	IS (A)	IS (A)	IS (mA)	IS (mA)	IS (A)	1×10^{-14} A
N	38.61/THETA	MD	38.61/θ	38.61/TH	N	1
q/NKT (1/V)	THETA (1/V)	38.61/MD(1/V)	θ (1/V)	TH (1/V)	-	38.61
t_{cs} (S)	KD/THETA(S)	TD (S)	KD 1/θ(ns)	1/W(ns)	TT (S)	10 ns
**q/KT (1/V)	38.61 (1/V)	38.61 (1/V)	38.61 (1/V)	38.61 (1/V)	38.61 (1/V)	38.61 (1/V)

*Not representative of SCEPTRE examples in the handbook

**At room temperature

incomplete data set. When utilizing a default value, a "units" conversion may be required to maintain a consistent set of parameters within a given code.

13. Linvill Lumped Model of The Diode

a. Introduction

The Linvill lumped model is presented in this section to introduce the analyst to an alternate approach to the modeling process. The Linvill lumped model uses elements that represent actual physical processes to describe the diode. The previous diode models treat only the terminal behavior of the device.

The Linvill model allows greater insight into the physical processes occurring in the diode. A disadvantage of the Linvill lumped model is the inability to directly obtain the values of the Linvill elements. For this reason, Linvill model is a more appropriate tool for analyses considering the effect of material or fabrication variations on device and circuit performance. The interaction between radiation effects at the basic material level and their manifestation in the electrical behavior of the diode is easily simulated by the model. The following presentation contains both electrical effects and radiation effects in the Linvill terminology.

The Linvill model provides great flexibility in modeling material variations in the diode structure and demonstrating the result of these variations on terminal performance. For example, diodes constructed with an epitaxial layer can have both the characteristics of the epitaxial layer and the substrate included individually by the incorporation of appropriate elements in the model.

Only the NET-2 circuit analysis code has Linvill elements which may be utilized directly in the construction of a Linvill lumped model. The model cannot be used directly in any other code addressed in the handbook.

b. Basic Concepts

Consider the diode shown in the schematic of figure II-54

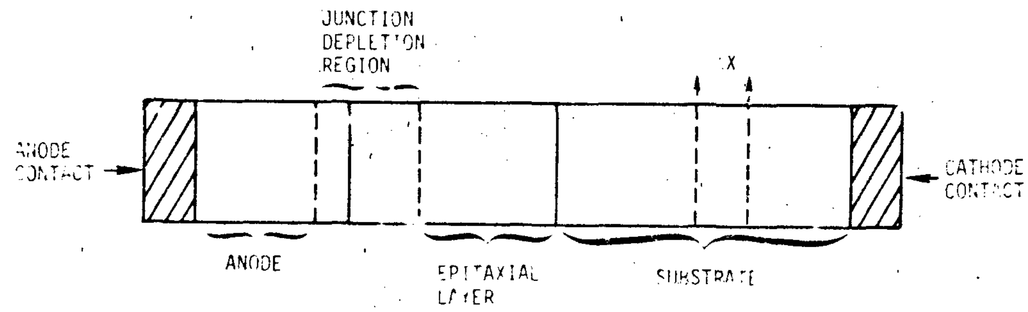


Figure II-54. Diode Structure

A slice of material ΔX is shown in the substrate material. This slice forms a volume $\Delta X \cdot A$ where A is the area of the diode. A fundamental equation of semiconductor physics, the continuity equation describes the processes occurring within a semiconductor volume as:

(1) The flow of minority carriers into the volume.

(2) The flow of minority carriers out of the volume.

(3) The recombination of carriers within the volume.

(4) The generation of carriers in the volume.

(5) The storage of minority carriers in the volume.

The usual procedure is to make the volumes approach zero and then contend with the resulting partial differential equations.

The Linvill model leaves the volumes finite. The volumes are usually formed by slicing the device parallel to the junction region so that the problem is one dimensional. The accuracy versus simplicity trade-off is made in determining the thickness and number of slices.

The Linvill elements are functions of the minority carrier concentrations in the region (holes if N-type, electrons if P-type). Each element represents a portion of the continuity equation. Diffusance represents the movement of carriers when a carrier gradient is formed. Storance represents charge flowing into a volume but not leaving the volume. Combinance represents the loss of minority carriers through

recombination. Driftance represents carrier motion produced by an electric field. The defining equations of the Linvill elements are given in figure II-55. The element symbols are used without the p-n subscripts when the material type is undefined.

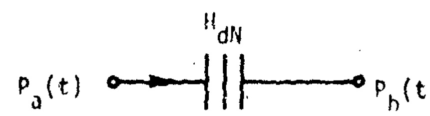
The "slices" of a semiconductor are represented by Linvill lumps. These lumps are valid only in quasineutral regions; that is, where no depletion exists. The Linvill elements represent the physical processes occurring in the lumps. A Linvill lump is shown in figure II-56. The current flow through the Linvill elements depends only on the value of minority carrier concentration at the minority carrier node as defined in figure II-55.

The junction region model is illustrated by figure II-57. The minority carrier concentrations at the depletion boundaries are defined as a function of the voltage across the junction and the equilibrium minority carrier concentrations n_{po} and p_{no}. The P-N junction model defines the boundary conditions for minority carrier concentrations and all diode current is a consequence of the charge at the junction.

c. Diode Modeling

The choice of the number and placement of the lumps for a diode is a matter of judgment. Only as few lumps as are required for correct results to a problem should be used. Some general rules are available.

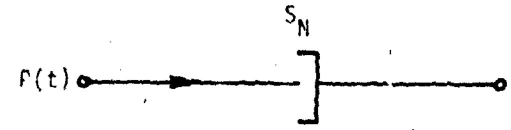
Diodes in which one side is heavily doped compared to the other side may be modeled by including lumps on only the lightly doped side. This simplification requires the assumption that minority carrier injection into the heavily doped side is insignificant. In the simplest form only one lump may be used. This model will be adequate for only the dc or slow behavior of the diode. Two lumps would produce a better simulation of the transient behavior. Often the "slices" of the two lump model are given different widths. Typical values are L/2 and 3L/2 where L is the diffusion length. The two lump model will predict a more accurate storage time but will yield significant errors in predicting the ratio of reverse to forward current. For better results, more lumps are needed.



$$i_{HdN} = H_{dn}\,(P_a(t) - P_b(t))$$

where

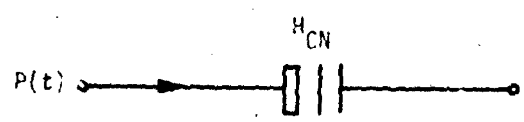
H_{dN} = the diffusance element
P = minority carrier hole concentration
i = current



$$i_{SN} = S_N \frac{dP}{dt}$$

where

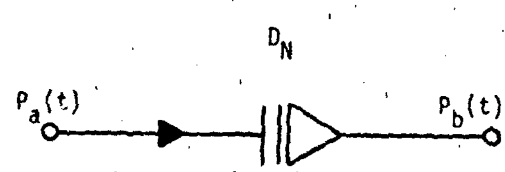
S_N = the storance element



$$i_{HCN} = H_{CN}\,P(t)$$

where

H_{CN} = the combinance element

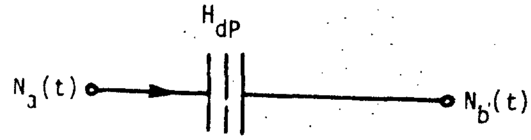


$$i_{DN} = D_N\,(P_a(t) - P_b(t))$$

where

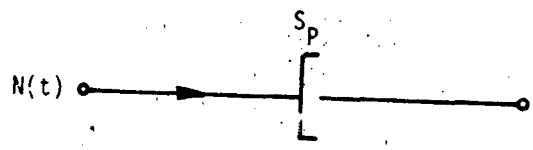
D_N = the driftance element

Figure II-55. Linvill Lumped Elements for N and P Material



$$i_{HdP} = H_{dP}\,(N_a(t) - N_b(t))$$

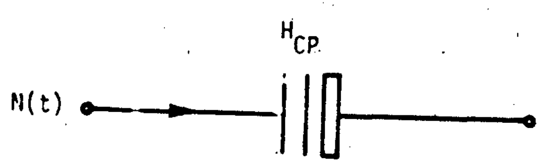
where H_{dP} = the diffusance element
N = minority carrier electron concentration



$$i_{SP} = S_P \frac{dN}{dt}$$

where

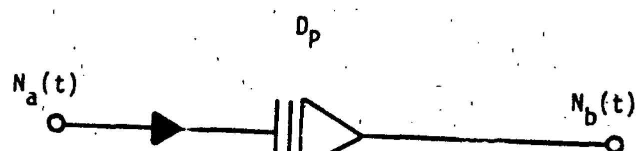
S_P = the storance element



$$i_{HCP} = H_{CP}\,N(t)$$

where

H_{CP} = the combinance element



$$i_{DP} = D_P(N_a(t) + N_b(t))$$

where D_P = the driftance element

Figure II-55. Linvill Lumped Elements for N and P Material (Concluded)

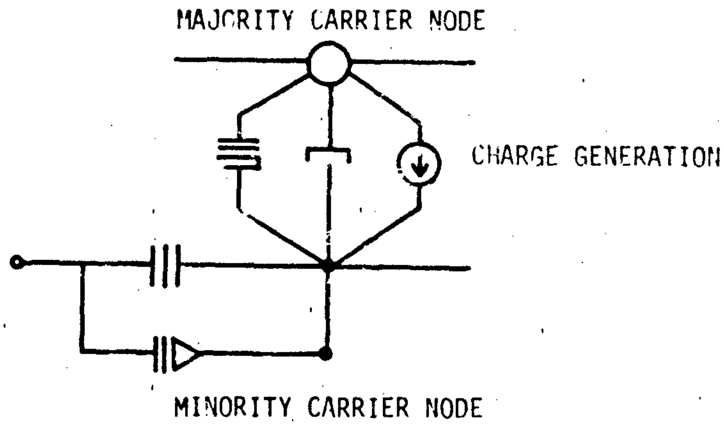


Figure II-56. Linvill Lump

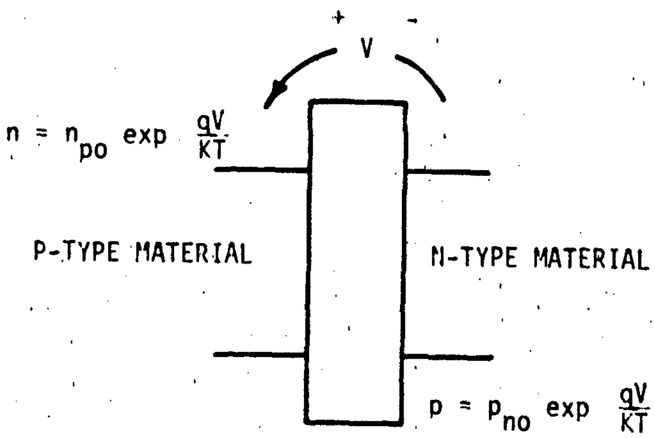


Figure II-57. Representation of Junction Region

For the case where neither side of the junction is heavily doped, lumps are required on each side of the junction.

d. Inclusion of Radiation Effects

The Linvill lumps will represent the physical changes induced by radiation. Ionizing radiation will produce an additional term for the charge generation current element which will be:

$$I_g = m_o H_c + \dot{\gamma} q g_o \Delta X A$$

where:

m_o = the equilibrium minority carrier concentration

g_o = the generation rate

ΔX = the width of the "slice"

A = the area of the "slice"

$\dot{H}_c$ = the value of the combinance element

A current generator across the Linvill junction is required to model the prompt component. This current generator will have the value:

$$I_p = \gamma q g_o WA$$

where W is the depletion region width.

Neutron damage will alter the values of the Linvill elements. Carrier removal effects will alter the equilibrium values of minority concentrations. The increased number of recombination sites produced by radiation-induced displacement may drastically alter the value of the combinance element. And finally, mobility changes will affect the values of the diffusance and driftance elements. The radiation sections of this chapter indicate some of the quantative changes which occur to the physical behavior of semiconductor material. The Linvill alterations of the Linvill element values must reflect these changes.

To illustrate the implementation of a Linvill diode by a circuit analysis code, a Linvill model of the 1N914 was developed by use of estimation techniques. This example is illustrated in the next section.

e. Example Linvill Diode Model

1) Description

The Linvill lumped model uses elements that represent actual physical processes to describe the diode. Neutron, photocurrent, and failure effects may be simulated.

2) Advantages

The Linvill model gives greater insight into the nature of semiconductor devices.

3) Cautions

The one lump model presented does not model second order effects. Transient behavior is not adequately modeled. The Linvill elements cannot be determined directly from terminal measurements.

4) Characteristics

The radiation inclusive one lump model for the 1N914 is illustrated in figure II-58.

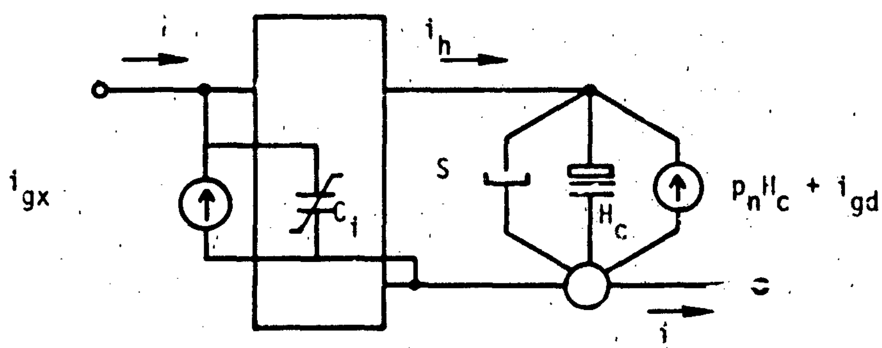


Figure II-58. One Lump Model

5) <u>Defining Equations</u>

$$m = m_o \left[\exp\left(\frac{qV}{KT}\right) - 1\right]$$

$$i_{gx} = \gamma q\, g\, AW$$

$$i_{gd} = \gamma q\, g\, AL$$

6) <u>Parameter List</u>

m = the minority carrier concentration within the lightly doped region at the boundary of the junction region

m_o = the equilibrium minority carrier concentration within the lightly doped side of the junction

q = the magnitude of the electronic charge

V = the voltage applied to the junction region

k = Boltzmann's constant

T = temperature in °K

S = the storance element

H_C = the combinance element

C_j = the junction capacitance

i_{gx} = photocurrent produced by generated carriers in depletion region

i_{gd} = photocurrent produced by carriers generated within one diffusion length of the depletion region edge

g = carrier generation rate

A = junction area

W = depletion width

L = diffusion length

7) Parameterization

a) m_o

m_o is the minority carrier concentration within the lightly doped region of a one-sided diode. If the N side is lightly doped, m_o equals p_{no}. If the P side of a diode is lightly doped, m_o is equal to n_{po}. m_o can be determined as:

$$m_o = \frac{n_i^2}{N_L}$$

where N_L is the doping concentration on the lightly doped side. Corresponding equations are:

$$p_{no} = \frac{n_i^2}{N_D}$$

$$n_{po} = \frac{n_i^2}{N_A}$$

where N_D and N_A are the doping concentrations in the N and P regions, respectively, and n_i is the intrinsic carrier concentration.

If the doping profiles are known, p_{no} and n_{po} can be estimated directly. If no doping information is available, then m_o can be estimated from measurements and used to calculate S and H_C, but information about which minority carrier is being dealt with will be unknown. N_L, the doping on the light side of a diode, can be estimated as (one-sided abrupt junction):

$$N_L = \left(\frac{V_{BD}}{2.72 \times 10^{12}}\right)^{-3/2}$$

m_o is now calculated for silicon at room temperature to be:

$$m_o = \frac{2.1 \times 10^{20}}{N_L}$$

b) $\underline{C_j}$

1 <u>Definition</u>

C_j is a nonlinear, voltage-dependent capacitor which is associated with the depletion region of a diode.

2 <u>Typical Value</u>

C_j varies with bias voltage and is typically on the order of 0.3 pF/mil^2 of junction area.

3 <u>Measurement</u>

C_j can be determined and characterized by the methods developed in chapter II.B.6.

c) $\underline{H_C}$

1 <u>Definitic</u>

H_C is the value of the combinance element in the one-lump model presented. The combinance element represents the recombination on nonequilibrium minority charge carriers.

2 <u>Typical Value</u>

Values of H_C vary widely. A typical value of H_C is 1×10^{-16} cm$^3 \cdot$A.

3 <u>Measurement</u>

H_C can be determined from the reverse saturation current of the diode, I_S. I_S is first determined using the measurement scheme developed in chapter II.B.3. H_C can now be calculated as:

$$H_C = \frac{I_S}{m_o}$$

d) S

1 Definition

S is the value of the storance element in the one lump model presented. The storance element represents minority charge storage in the neutral, lightly doped side of the diode.

2 Typical Value

Values of the storance element may vary widely. A typical value for S is 1×10^{-24} $cm^3 \cdot C$.

3 Measurement

S can be calculated from t_{cs} values. t_{cs} values can be determined by the method explained in chapter II.B.7. S can then be calculated from:

$$S = t_{cs} H_C$$

8) Example - 1N914

a) m_o

Since doping profiles of the 1N914 are not readily available, m_o was estimated using the measured breakdown voltage and assuming the 1N914 is a well-behaved, one-sided junction. The reverse breakdown voltage was then measured at a reverse current of 10 μA as 150 volts. m_o was then calculated as:

$$m_o = \frac{2.1 \times 10^{20}}{\left(\dfrac{150\ V}{2.72 \times 10^{12}}\right)^{-3/2}} = 8.6 \times 10^4/cm^3$$

b) H_C

H_C for the 1N914 diode can now be determined from a calculated value of I_S and m_o. For the value of I_S used in the 1N914 model, H_C is:

$$H_C = \frac{1.21 \times 10^{-9}\ A}{8.6 \times 10^{4}/cm^{3}} = 1.41 \times 10^{-14}$$

c) S

S is determined from H_C and t_{cs} as:

$$S = (1.15 \times 10^{-8}\ sec)\ (1.41 \times 10^{-14}) = 1.62 \times 10^{-22}\ cm^{3} \cdot C$$

f. Example Computer Simulations

1) Forward Characteristic of Linvill Diode

The Linvill 1N914 diode was exercised through its forward characteristic to allow comparison with other theoretical and actual data. The network used to test the Linvill diode is illustrated in figure II-59. The NET-2 input listing is given in figure II-60. The simulated characteristic is plotted along with the actual characteristic in figure II-61. Excellent agreement is obtained.

2) Transient Response of 1N914 Model

The Linvill diode model was put through the same storage time test as was the standard diode model. As expected, the waveform produced was nearly identical. The NET-2 listing for this run is given in figure II-62. The output plot is given in figure II-63. All storage time parameters (forward current, reverse current, storage time) compare very closely to those of the standard diode model (figure II-39).

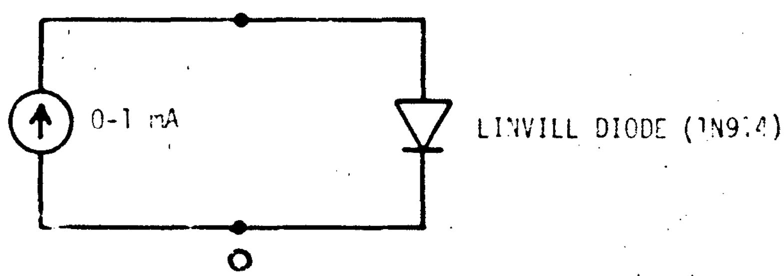
C. REFERENCES

II-1. Preferred Semiconductors and Components From Texas Instruments, Texas Instruments, 1970 Catalog.

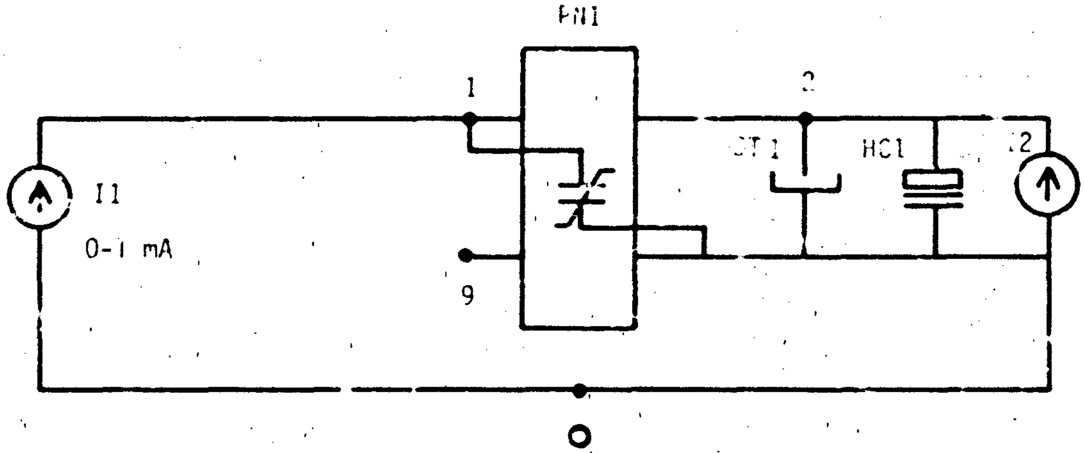
II-2. Wirth, J. L. and S. C. Rogers. "The Transient Response of Transistors," IEEE Transactions on Nuclear Science, NS-11, November 1964.

II-3. Pocock, D. N., et al. "Simplified Microcircuit Modeling," AFWL-TR-73-272, March 1974.

II-4. Radiation Effects on Semiconductor Services, Harry Diamond Laboratories, HDL-DS-77-1, May 1977.



(a) Forward Characteristic



(b) Expanded View of Test Circuit

Figure II-59. Linvill Diode Test Circuit

```
NET-2 NETWORK ANALYSIS PROGRAM    RELEASE 9
 03/24/78     15.12.03.

          00000000011111111112222222222333333333344444444445555555555666666666677777777778
          12345678901234567890123456789012345678901234567890123456789012345678901234567890
        *CHARACTERISTIC OF LINVILL LUMPED DIODE MODEL
          PN1 1 0 9 2 DIODE
          ST1 0 2 1.52E-22
          MC1 0 2 1.41E-14
          I2 2 0 9.8E-10
          I1 1 0 P1
          P1 0
          LIBRARY
                PN DIODE 9
                      C 1.37E-12
                      N 0.0181
                      VPO 0
                      PNO 9.6E4
                      TH 21.69
                      VZ 0.5
          STATE1
          STATE1
                P1 0 (50) 1.E-3
                PLOT I1 VS N(1)
          END
```

Figure II-60. NET-2 Listing for Linvill Diode Test

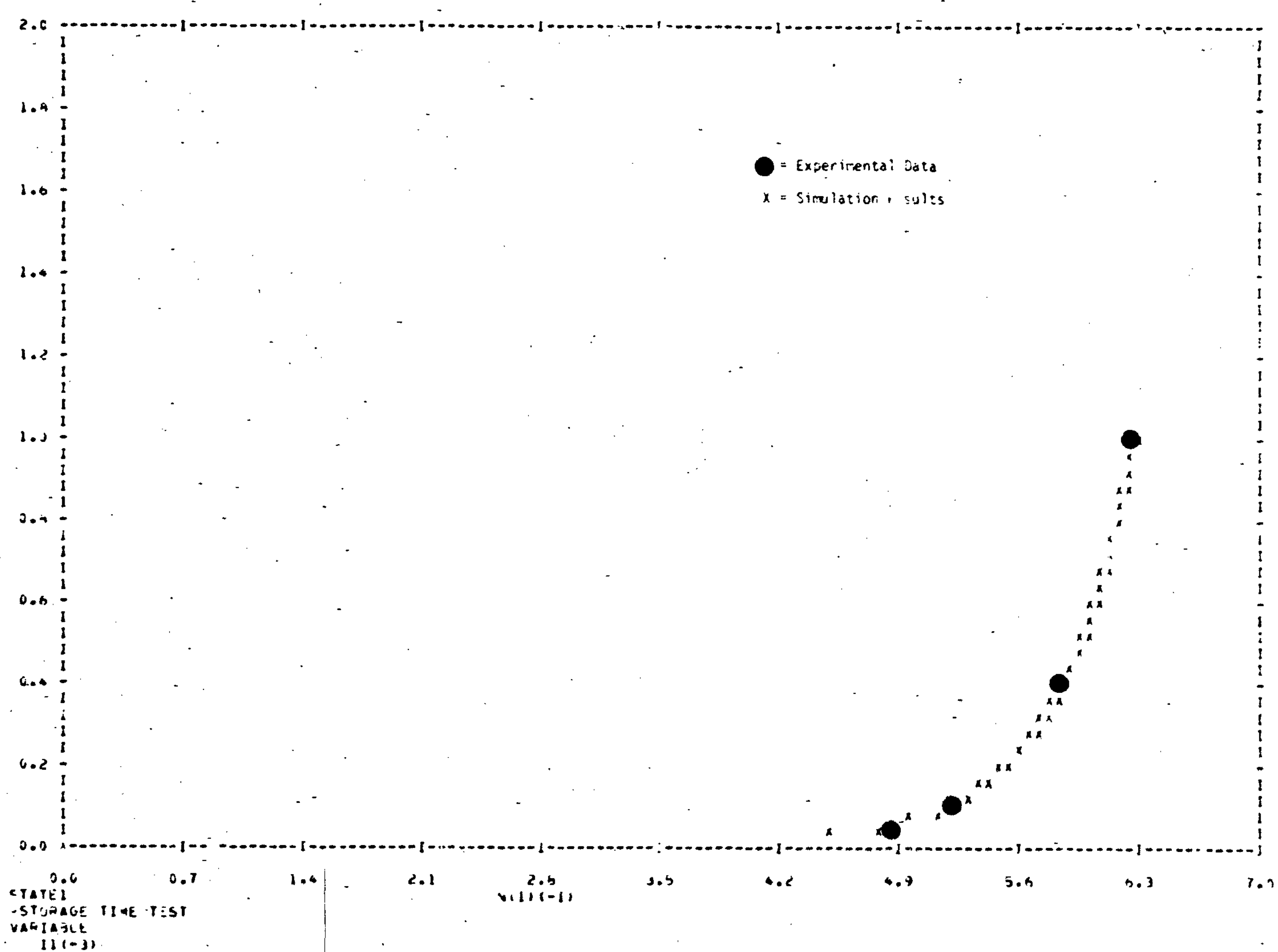


Figure II-61. Linvill Model Results and Experimental Data

```
NET-2 NETWORK ANALYSIS PROGRAM    RELEASE 9
 03/24/78     14.33.33.

     00000000011111111112222222222333333333344444444445555555555666666666677777777778
     12345678901234567890123456789012345678901234567890123456789012345678901234567890
     *LINVILL TRANSIENT TEST
     PN1 4 5 9 8 DIODE
     ST1 6 8 1.52E-22
     HC1 6 8 1.41E-14
     I2 8 6 9.8E-10
     R1 2 3 1000.
     R2 3 4 1000.
     R3 6 0 50.
     R4 7 5 1000.
     C1 5 4 .39E-6
     C2 3 0 .47E-7
     V1 2 0 20.5
     V2 7 0 TABLE1(TIME)
     TABLE1
          0 0
          10.E-9 0
          11.E-9 -22
          20.E-9 -22
     LIBRARY
          PN DIODE 8
               C 1.37E-12
               N 0.0181
               VPO 0
               PNO 8.6E4
               TH 21.69
               VZ 0.5
     STATE1
          TIME 0 (50) 50.E-9
          PLOT I(R3)
     END
```

Figure II-62. NET-2 Listing for Storage Time Test

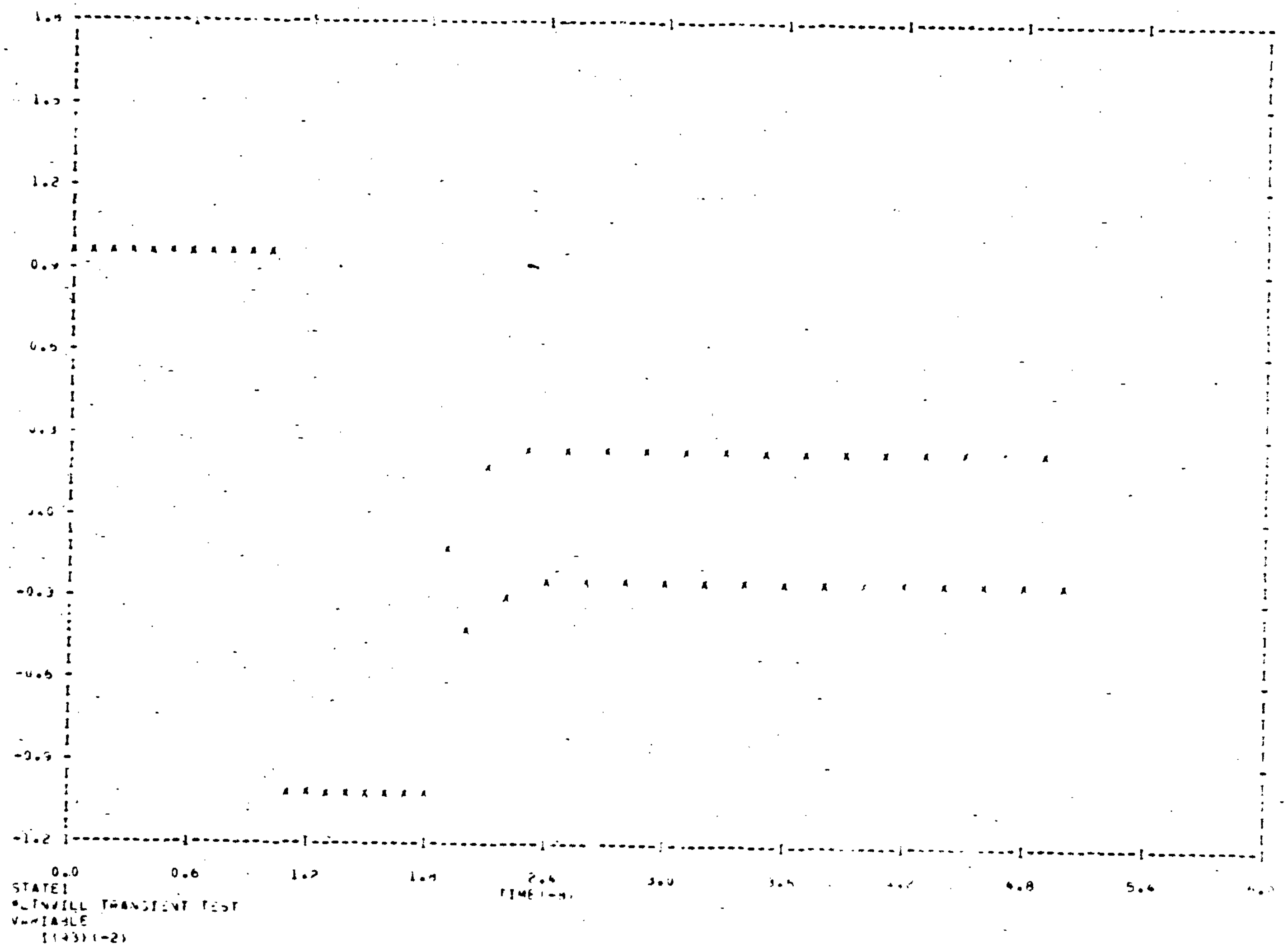


Figure II-63. Storage Time Waveform Produced by One Lump Diode Model

CHAPTER III

BIPOLAR TRANSISTORS

CHAPTER III

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CHAPTER III

BIPOLAR TRANSISTORS

A. INTRODUCTION

Bipolar junction transistor models are the best represented category of models and also the most diverse. The three basic transistor modeling approaches considered in this chapter are the Ebers-Moll model, Gummel-Poon model, and Linvill lumped model.

An "expandable model" format is applied in this chapter to allow the analyst to develop the simplest model required for the problem under consideration. The expansions occur in four steps:

(1) Basic Transistor Modeling

(2) The Addition of Ohmic and Charge Storage Elements

(3) Modeling of Beta Variations

(4) Modeling Higher Order Effects

The transistor models presented in this chapter represent a summary of the essential features of Modeling The Bipolar Transistor by Ian Getreu (reference 1). Users interested in more than a superficial treatment of transistor models are referred to this book.

The user should always be aware of the limitations of the model being used. Transistor models are usually based on describing equations which require numerous simplifications and assumptions for their development. If possible, attempts should be made to develop a basic understanding of the physical processes which occur in a transistor. Such an understanding will vastly simplify the modeling process. Discussions of physical phenomenon in this handbook need not be understood to develop a model, but are merely intended to clarify the reasons for model development.

A transistor model will only be as accurate as the parameters which describe it. Judgment must be exercised concerning which source of parameter information to use. Data sheet information is generally very conservative yet it places bounds on the parameters of a device type. Minimum beta information from data sheets will yield a worst case value for neutron hardness assessments but will represent a lower bound for

secondary photocurrent production. Measurements will yield accurate values for the device being measured, but will not indicate the distribution of parameters over the whole device type. The problem of choosing parameter values now becomes statistical in nature and may be treated as such if sufficient information can be obtained. Radiation effects simulation often requires knowledge of material physical properties. This chapter includes techniques for estimating these properties from terminal measurements on transistors. These techniques are often based on far reaching assumptions and should be applied only in the absence of better data. Again, a physical understanding of the problem will give the analyst insight into the usefulness of a given estimation technique.

B. TRANSISTOR MODELING

1. Basic Transistor Model

a. Description

The most widely used basic transistor model was originally proposed by Ebers and Moll. It is a nonlinear, large signal dc model which models the fundamental current gain properties of transistors.

b. Advantages

The basic transistor model may be quickly and easily parameterized. Manufacturer specification sheets are often all that is required to develop useful models. It will perform first order dc analyses with minimum computer time.

c. Cautions

The basic transistor model simulates only first order dc effects. Therefore, it cannot simulate frequency effects or any of the second order transistor characteristics covered by latter sections.

d. Characteristics

Two versions of the basic transistor model are the transport version and the injection version. The two are mathematically identical, differing only in the choice of reference currents. The injection version is shown in figure III-1.

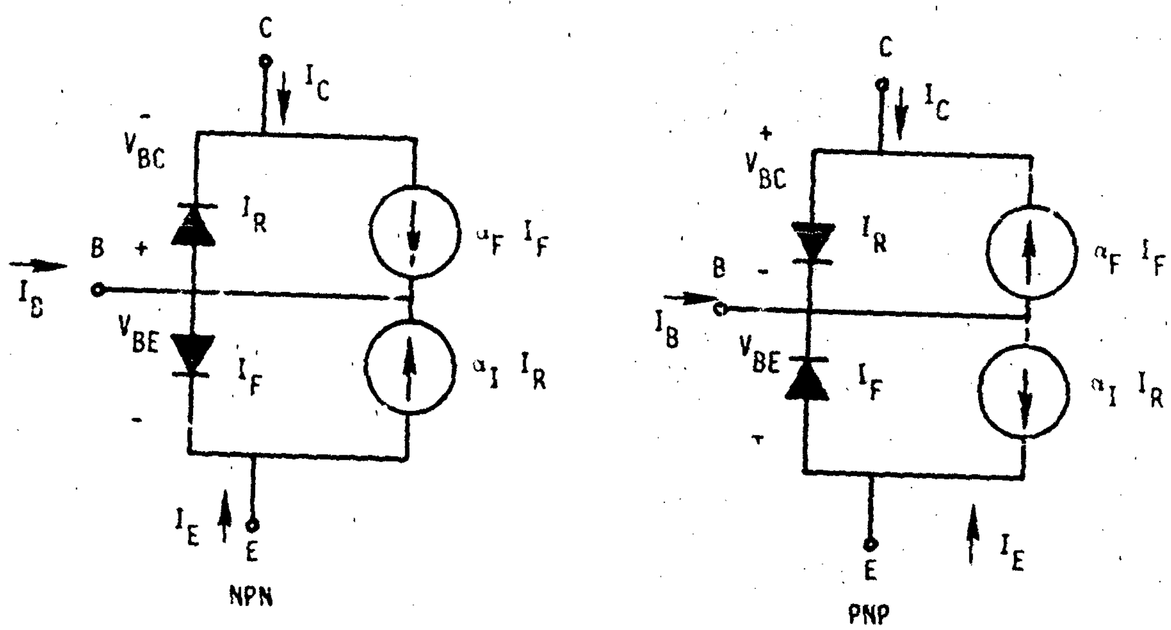


Figure III-1. Injection Version

The transport version of the basic transistor model is shown in figure III-2.

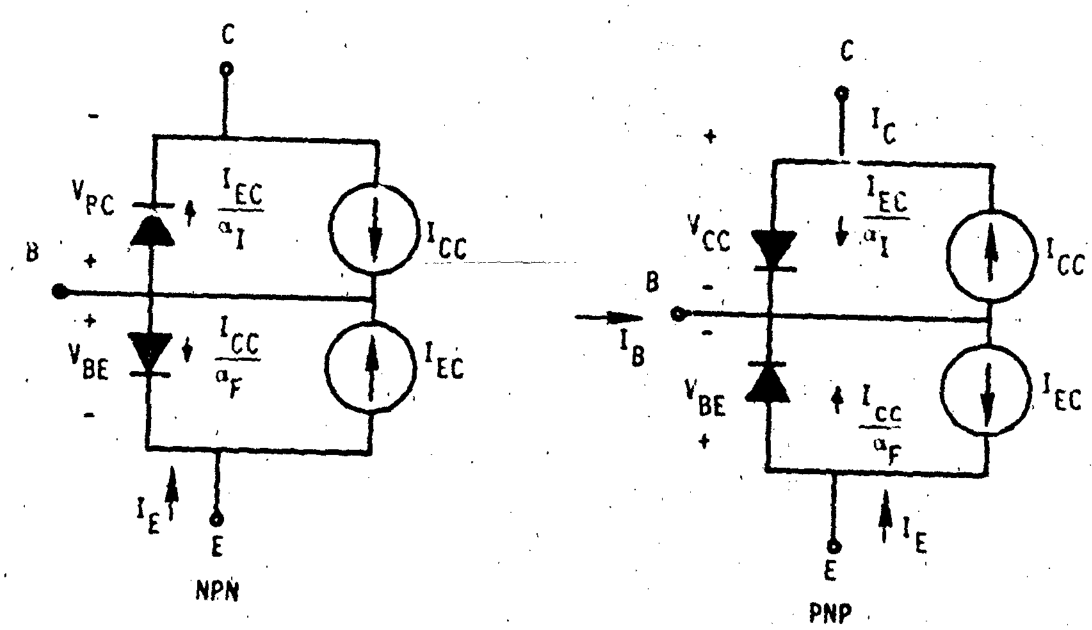


Figure III-2. Transport Version

The transport version is preferable for the following reasons:

(1) Both reference currents can be completely determined if a single quantity, I_S, is known.

(2) In practice, transport reference currents are linear over many decades on a semilog plot.

(3) For more complex models, diffusion capacitance is more easily specified.

An example of the transport version will be given in this chapter. Both versions of the basic transistor model produce an ideal characteristic illustrated in figure III-3.

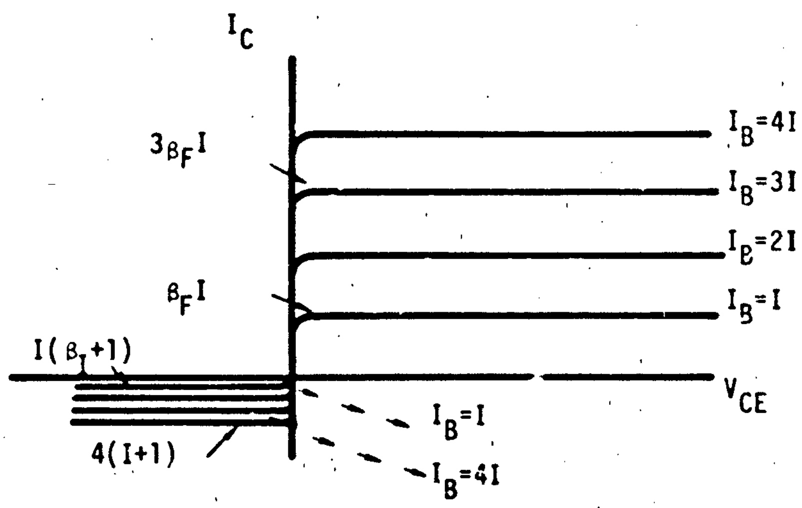


Figure III-3. Model Characteristic

e. <u>Defining Equations</u>

For the injection version:

$$I_F = I_{ES}\left[\exp\left(\frac{qV_{BE}}{KT}\right) -1\right]$$

$$I_R = I_{CS}\left[\exp\left(\frac{qV_{BC}}{KT}\right) -1\right]$$

For the transport version:

$$I_{CC} = I_S \left[\exp \left(\frac{qV_{BE}}{KT} \right) -1 \right]$$

$$I_{EC} = I_S \left[\exp \left(\frac{qV_{BC}}{KT} \right) -1 \right]$$

f. <u>Parameter List</u>

I_{CC} = reference collector source current
I_{EC} = reference emitter source current
I_S = transistor saturation current
q = magnitude of electronic charge (1.60×10^{-19} coulombs)
K = Boltzmann's constant (8.62×10^{-5} eV/°K)
T = temperature of device in °K
V_{BE} = base to emitter voltage
V_{BC} = base to collector voltage
α_F = forward large current common base gain
α_I = inverse large current common base gain

g. <u>Parameters to be Found</u>

I_S, α_F, α_I, T

h. <u>Parameterization</u>

1) <u>α_F</u>

a) <u>Definition</u>

α_F is the ratio of the dc collector current to the dc emitter current when the transistor is in the normal active region (collector-base reverse biased, base-emitter forward biased) and the base is grounded. Although α_F typically varies with collector current, for most applications a constant value may be assumed.

b) <u>Typical Value</u>

A typical value for α_F is 0.99.

c) Measurement

α_F can be determined from the relationship:

$$\alpha_F = \frac{\beta_F}{1 + \beta_F}$$

where β_F is the ratio of the dc collector current to the dc base current when the transistor is in the normal active region and the emitter is grounded.

The appropriate constant value of β_F can be determined by biasing the transistor to a desired operating point and then dividing the collector current by the base current. Current gain information may also be obtained from manufacturer specification sheet data.

d) Example - 2N2222A

1 From Measurement

α_F was determined from the curve tracer photograph shown in figure III-4. The point to be modeled was chosen as V_{CE} = 10 V and I_C = 5 mA. The trace most closely corresponding to the chosen point is I_B = 4(5 μA) = 20 μA. At V_{CE} = 10 V, this base drive produces a collector current of 5.6 mA.

$$\beta_F = 4.6 \text{ mA}/20\ \mu\text{A} = 230$$

$$\alpha_F = 230/(1 + 230) = 0.99567$$

Other operating points which could have been chosen are shown in table III-1.

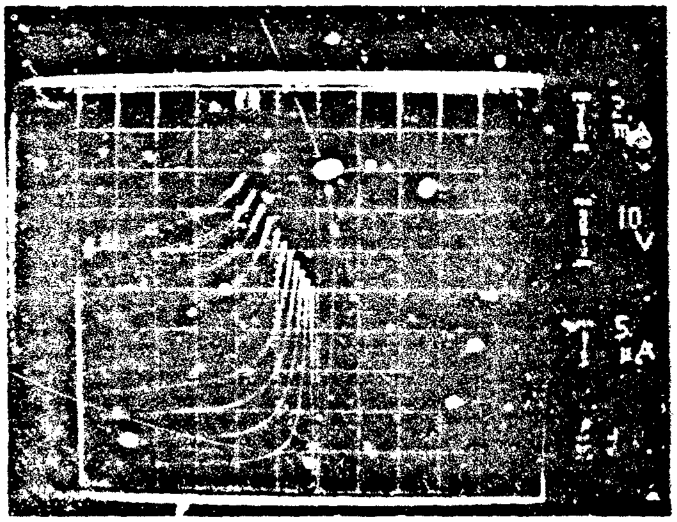


Figure III-4. 2N2222A Forward Characteristics

TABLE III-1. ALTERNATE OPERATING POINTS

I_B	β
5 μA	240
10	240
15	240
20	240
25	240
30	240
35	251
40	250
45	249
50	256

2 From Data Sheets

The manufacturer specification sheet parameters are listed in figure III-5. From the "On Characteristics" section dc current gain (β) for the 2N2222A is specified as a minimum of 50 at I_C = 1 mA and a minimum of 75 at I_C = 10 mA The "Selection Guide" puts dc current gain between 100 and 300 at I_C = 150 mA. The data sheets therefore provide useful information for worst case simulations, but fail to provide an accurate estimation of current gain for a given device.

2) α_I

a) Definition

α_I, the inverse α, is the ratio of the dc emitter current to dc collector current when the transistor is in the inverse operating region (collector-base forward biased, base-emitter reverse biased), and the base is grounded.

b) Typical Value

A typical value of α_I is 0.5.

c) Measurement

α_I can be measured with the same technique as α_F, but with the emitter and collector leads interchanged.

2N2218S, AS, 2N2219S, AS, 2N2221, A (SILICON)
2N2222, A, 2N5581, 2N5582

NPN SILICON ANNULAR HERMETIC TRANSISTORS

[illegible] widely used Industry Standard transistors for applications as medium speed switches and as amplifiers from audio to VHF frequencies.

- DC Current Gain Specified [illegible] to 500 mAdc
- Low Collector Emitter Saturation Voltage
  $V_{CE(sat)}$ [illegible]
  [illegible] Max — Non A Suffix
  [illegible] Max — A Suffix
- High Current Gain Bandwidth Product
  f_T [illegible] — All Types Except
  [illegible] — 2N2219A, 2N2222A, 2N5582
- Complements to PNP 2N2904 A thru 2N2907 A
- JAN, JTX [illegible] devices
- JTX [illegible] Available in 2N2222 A Series
- [illegible] Package [illegible]

NPN SILICON SWITCHING AND AMPLIFIER TRANSISTORS

CASE 79-02
TO-39
[illegible]

CASE 22-03
[illegible]
2N2221 A
2N2222 A

CASE 26-03
[illegible]
2N5581
2N5582

SELECTION GUIDE

Device Type	BVCEO I_C = 10 mAdc Volts	hFE I_C = 150 mAdc Min Max	I_C = 500 mAdc	Package
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	40	[illegible]	[illegible]	[illegible]
[illegible]	40	[illegible]	[illegible]	[illegible]

***MAXIMUM RATINGS**

Rating	Symbol	2N2218 2N2219 2N2221 2N2222	2N2218A 2N2219A 2N2221A 2N2222A	2N5581 2N5582	Unit
[illegible] Voltage	[illegible]	[illegible]	40	[illegible]	[illegible]
[illegible] Voltage	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible] Voltage	[illegible]	[illegible]	[illegible]	6.0	[illegible]
[illegible] Current [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		2N2218 A 2N2219 A	2N2221 A 2N2222 A	2N5581 2N5582	
[illegible] Dissipation [illegible] T_A [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Watt
Derate above [illegible]		[illegible]	[illegible]	[illegible]	[illegible]
[illegible] Dissipation [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Watts
Derate above [illegible]		[illegible]	[illegible]	11.43	[illegible]
Operating and Storage Junction Temperature Range	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

[illegible]

Figure III-5 2N2222A Manufacturer Specification Sheets (ref. III-1)

2N2218S,AS, 2N2219S,AS, 2N2221,A, 2N2222,A, 2N5581, 2N5582 (continued)

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector Emitter Breakdown Voltage		BV_{CEO}			Vdc
(I_C = 10 mAdc, I_B = 0)	Non A Suffix		30	-	
	A Suffix, 2N5581,2N5582		40	-	
Collector Base Breakdown Voltage		BV_{CBO}			Vdc
(I_C = 10 μAdc, I_E = 0)	Non A Suffix		60	-	
	A Suffix, 2N5581,2N5582		75	-	
Emitter Base Breakdown Voltage		BV_{EBO}			Vdc
(I_E = 10 μAdc, I_C = 0)	Non A Suffix		5.0	-	
	A Suffix, 2N5581,2N5582		6.0	-	
Collector Cutoff Current		I_{CEX}			nAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	A Suffix, 2N5581,2N5582		-	10	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = 50 Vdc, I_E = 0)	Non A Suffix			0.01	
(V_{CB} = 60 Vdc, I_E = 0)	A Suffix, 2N5581,2N5582		-	0.01	
(V_{CB} = 50 Vdc, I_E = 0, T_A = 150°C)	Non A Suffix			10	
(V_{CB} = 60 Vdc, I_E = 0, T_A = 150°C)	A Suffix, 2N5581,2N5582			10	
Emitter Cutoff Current		I_{EBO}			nAdc
(V_{EB} = 3.0 Vdc, I_C = 0)	A Suffix, 2N5581,2N5582			10	
Base Cutoff Current		I_{BL}			nAdc
(V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	A Suffix			20	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			
(I_C = 0.1 mAdc, V_{CE} = 10 Vdc)	2N2218,A,2N2221,A,2N5581(1)		20		
	2N2219,A,2N2222,A,2N5582(1)		35	-	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	2N2218,A,2N2221,A,2N5581		25		
	2N2219,A,2N2222,A,2N5582		50		
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	2N2218,A,2N2221,A,2N5581(1)		35		
	2N2219,A,2N2222,A,2N5582(1)		75		
(I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = -55°C)	2N2218A,2N2221A,2N5581		15		
	2N2219A,2N2222A,2N5582		35		
(I_C = 150 mAdc, V_{CE} = 10 Vdc)(1)	2N2218,A,2N2221,A,2N5581		40	120	
	2N2219,A,2N2222,A,2N5582		100	300	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc)(1)	2N2218A,2N2221A,2N5581		20		
	2N2219A,2N2222A,2N5582		50		
(I_C = 500 mAdc, V_{CE} = 10 Vdc)(1)	2N2218,2N2221		20		
	2N2219,2N2222		30		
	2N2218A,2N2221A,2N5581		25		
	2N2219A,2N2222A,2N5582		40		
Collector Emitter Saturation Voltage(1)		$V_{CE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)	Non A Suffix			0.4	
	A Suffix, 2N5581,2N5582			0.3	
(I_C = 500 mAdc, I_B = 50 mAdc)	Non A Suffix			1.6	
	A Suffix, 2N5581,2N5582			1.0	
Base Emitter Saturation Voltage(1)		$V_{BE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)	Non A Suffix		0.6	2.0	
	A Suffix, 2N5581,2N5582		0.6	1.2	
(I_C = 500 mAdc, I_B = 50 mAdc)	Non A Suffix			2.6	
	A Suffix, 2N5581,2N5582			2.0	

* Indicates JEDEC Registered Data

Figure III-5. 2N2222A Manufacturer Specification Sheets (Continued)

2N2218S,AS, 2N2219S,AS, 2N2221,A, 2N2222,A, 2N5581, 2N5582 (continued)

*ELECTRICAL CHARACTERISTICS (Continued)

Characteristic		Symbol	Min	Max	Unit
SMALL SIGNAL CHARACTERISTICS					
Current Gain – Bandwidth Product(2)		f_T			MHz
(I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	All Types Except		250		
	2N2219A, 2N2222A, 2N5582		300		
Output Capacitance(3)		C_{ob}		8.0	pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)					
Input Capacitance(3)		C_{ib}			pF
(V_{EB} = 0.5 Vdc, I_C = 0, f = 100 kHz)	Non A Suffix			30	
	A Suffix, 2N5581, 2N5582			25	
Input Impedance		h_{ie}			k ohms
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A, 2N2221A, 2N5581		1.0	3.5	
	2N2219A, 2N2222A, 2N5582		2.0	8.0	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A, 2N2221A, 2N5581		0.2	1.0	
	2N2219A, 2N2222A, 2N5582		0.25	1.25	
Voltage Feedback Ratio		h_{re}			X 10^{-4}
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A, 2N2221A, 2N5581			5.0	
	2N2219A, 2N2222A, 2N5582			8.0	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A, 2N2221A, 2N5581			2.5	
	2N2219A, 2N2222A, 2N5582			4.0	
Small Signal Current Gain		h_{fe}			
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A, 2N2221A, 2N5581		30	150	
	2N2219A, 2N2222A, 2N5582		50	300	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A, 2N2221A, 2N5581		50	300	
	2N2219A, 2N2222A, 2N5582		75	375	
Output Admittance		h_{oe}			μmhos
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A, 2N2221A, 2N5581		3.0	15	
	2N2219A, 2N2222A, 2N5582		5.0	35	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N2218A, 2N2221A, 2N5581		10	100	
	2N2219A, 2N2222A, 2N5582		25	200	
Collector Base Time Constant		$r_b'C_c$			ps
(I_E = 20 mAdc, V_{CB} = 20 Vdc, f = 31.8 MHz)	A Suffix, 2N5581, 2N5582			150	
Noise Figure		NF			dB
(I_C = 100 μAdc, V_{CE} = 10 Vdc, R_S = 1.0 k ohm, f = 1.0 kHz)	2N2219A, 2N2222A			4.0	
SWITCHING CHARACTERISTICS (A Suffix, 2N5581 and 2N5582)					
Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = 0.5 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc) (Figure 14)	t_d		10	ns
Rise Time		t_r		25	ns
Storage Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc) (Figure 15)	t_s		225	ns
Fall Time		t_f		60	ns
Active Region Time Constant** (I_C = 150 mAdc, V_{CE} = 30 Vdc)		τ_A		2.5	ns

*Indicates JEDEC Registered Data

**Motorola Guarantees this Data in Addition to JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

(2) f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity

(3) 2N5581 and 2N5582 are Listed C_{cb} and C_{eb} for these conditions and values

Figure III-5. 2N2222A Manufacturer Specification Sheets (Continued)

FIGURE 1 – NORMALIZED DC CURRENT GAIN

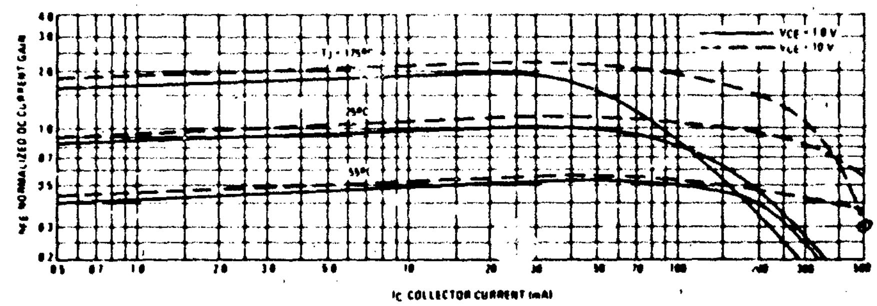
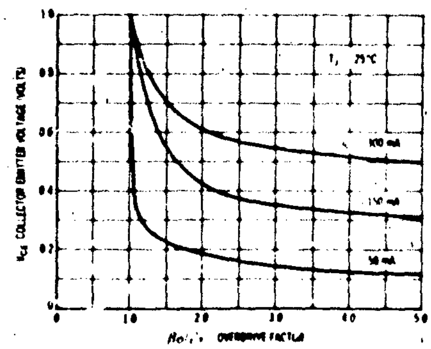


FIGURE 2 – COLLECTOR CHARACTERISTICS IN SATURATION REGION



This graph shows the effect of base current on collector current. β_e (current gain at the edge of saturation) is the current gain of the transistor at 1 volt, and β_f (forced gain) is the ratio of I_C/I_B in a circuit.

EXAMPLE: For type 2N2219, estimate a base current (I_B) to insure saturation at a temperature of 25°C and a collector current of 150 mA.

Observe that at I_C = 150 mA an overdrive factor of at least 2.5 is required to drive the transistor well into the saturation region. From Figure 1, it is seen that h_{FE} @ 1 volt is approximately 0.62 of h_{FE} @ 10 volts. Using the guaranteed minimum gain of 100 @ 150 mA and 10 V, β_e = 62 and substituting values in the overdrive equation we find:

$$\frac{\beta_e}{\beta_f} = \frac{h_{FE} @ 1.0\,V}{I_C/I_B} = 2.5 = \frac{62}{150/I_B} \qquad I_B \geq 6.0\ mA$$

FIGURE 3 – "ON" VOLTAGES

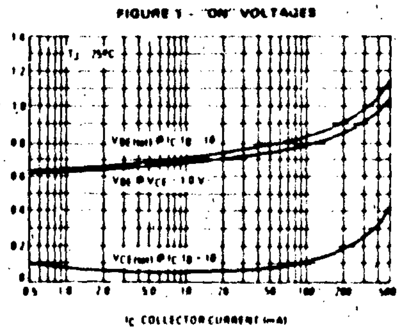


FIGURE 4 – TEMPERATURE COEFFICIENTS

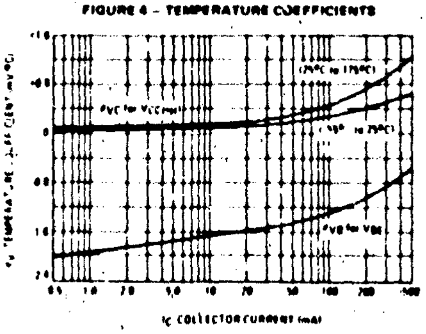


Figure III-5. 2N2222A Manufacturer Specification Sheets (Continued)

NOISE FIGURE

$V_{CE} = 10\ V, T_A = 25^{\circ}C$

FIGURE 5 – FREQUENCY EFFECTS

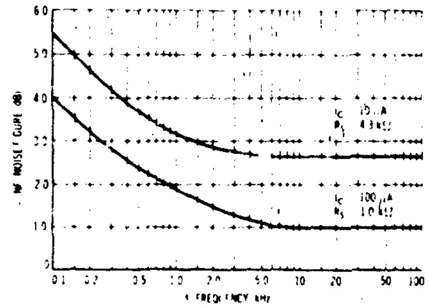
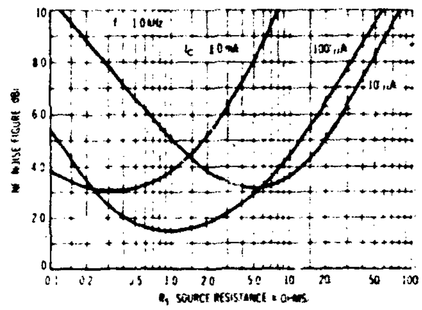


FIGURE 6 – SOURCE RESISTANCE EFFECTS



h PARAMETERS

$V_{CE} = 10\ Vdc, f = 1.0\ kHz, T_A = 25^{\circ}C$

This group of graphs illustrates the relationship between h_{fe} and other "h" parameters for this series of transistors. To obtain these curves, a high gain and a low gain unit were selected and the same units were used to develop the correspondingly numbered curves on each graph.

FIGURE 7 – INPUT IMPEDANCE

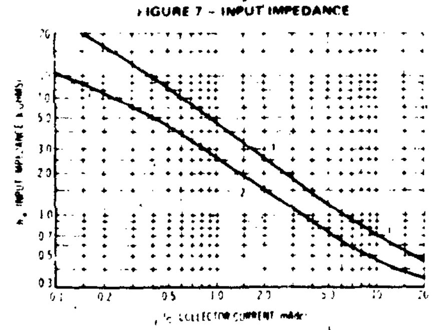


FIGURE 8 – VOLTAGE FEEDBACK RATIO

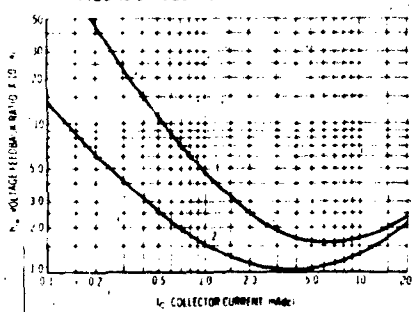


FIGURE 9 – CURRENT GAIN

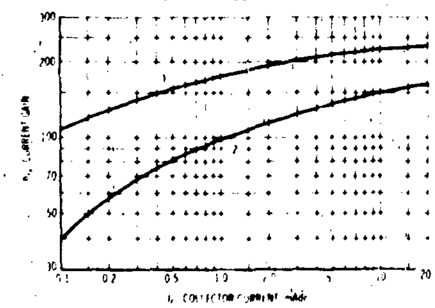


FIGURE 10 – OUTPUT ADMITTANCE

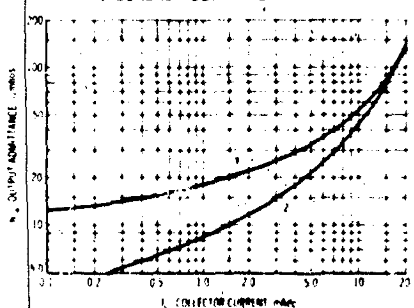


Figure III-5. 2N2222A Manufacturer Specification Sheets (Continued)

SWITCHING TIME CHARACTERISTICS

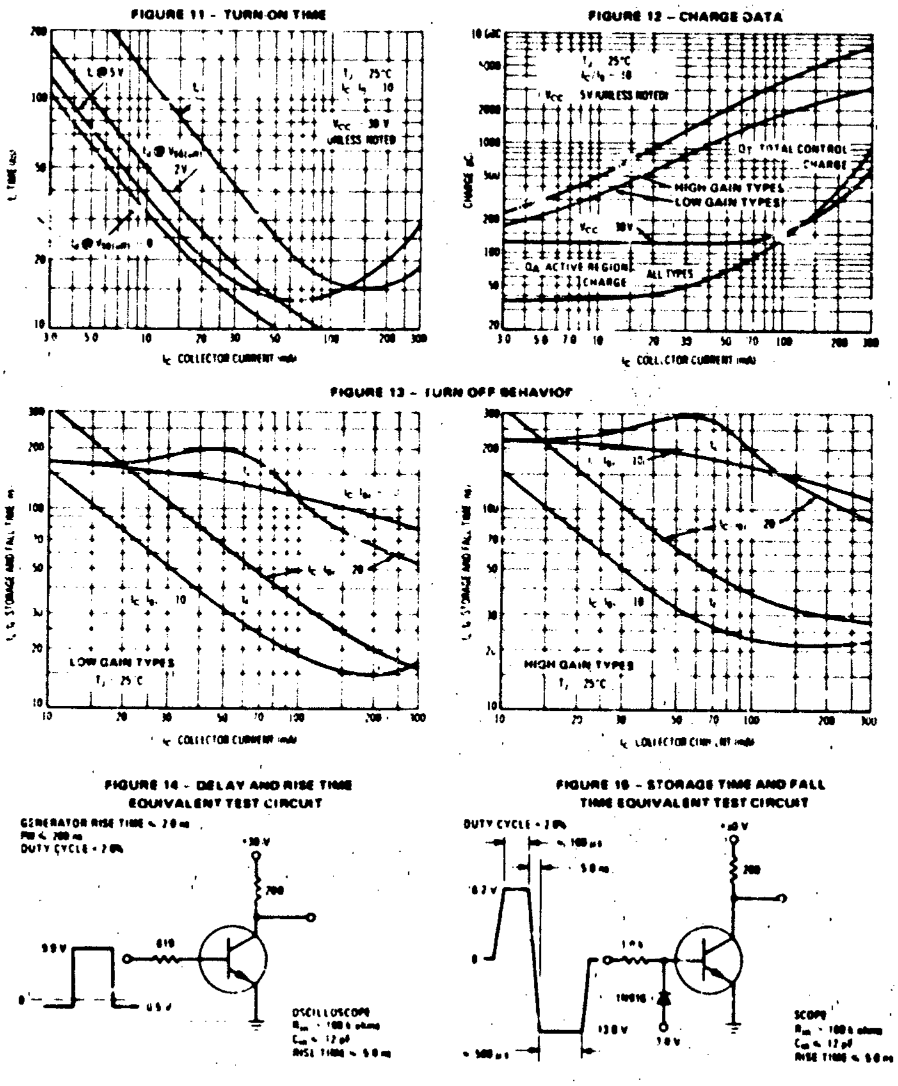


Figure III-5. 2N2222A Manufacturer Specification Sheets (Continued)

2N2218S,AS, 2N2219S,AS, 2N2221,A, 2N2222,A, 2N5581, 2N5582 (continued)

FIGURE 16 – CURRENT GAIN BANDWIDTH PRODUCT AND COLLECTOR BASE TIME CONSTANT DATA

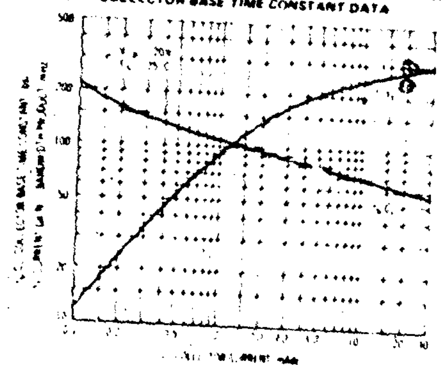


FIGURE 17 – CAPACITANCES

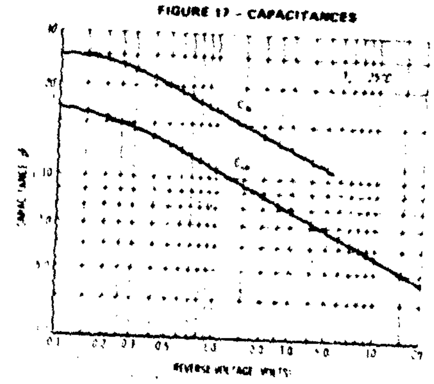
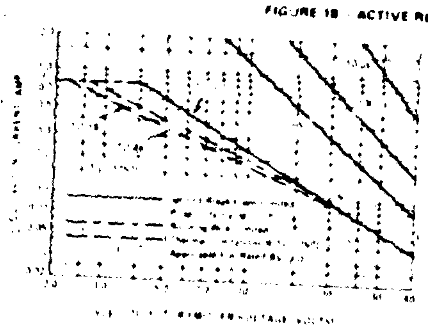


FIGURE 18 – ACTIVE REGION SAFE OPERATING AREAS



This graph shows the maximum I_C-V_{CE} limits of the device both from the standpoint of thermal dissipation (at 25°C case temperature) and secondary breakdown. For case temperatures other than 25°C, the thermal dissipation curve must be modified in accordance with the derating factor in the Maximum Ratings table.

To avoid possible device failure, the collector load line must fall below the limits indicated by the applicable curve. Thus, for certain operating conditions the device is thermally limited, and for others it is limited by secondary breakdown.

For pulse applications, the maximum I_C-V_{CE} product indicated by the dc thermal limits can be exceeded. Pulse thermal limits may be calculated by using the transient thermal resistance curve of Figure 19.

FIGURE 19 – THERMAL RESPONSE

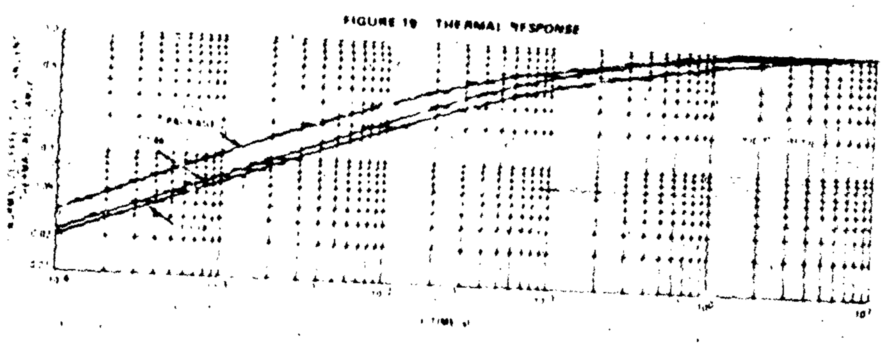
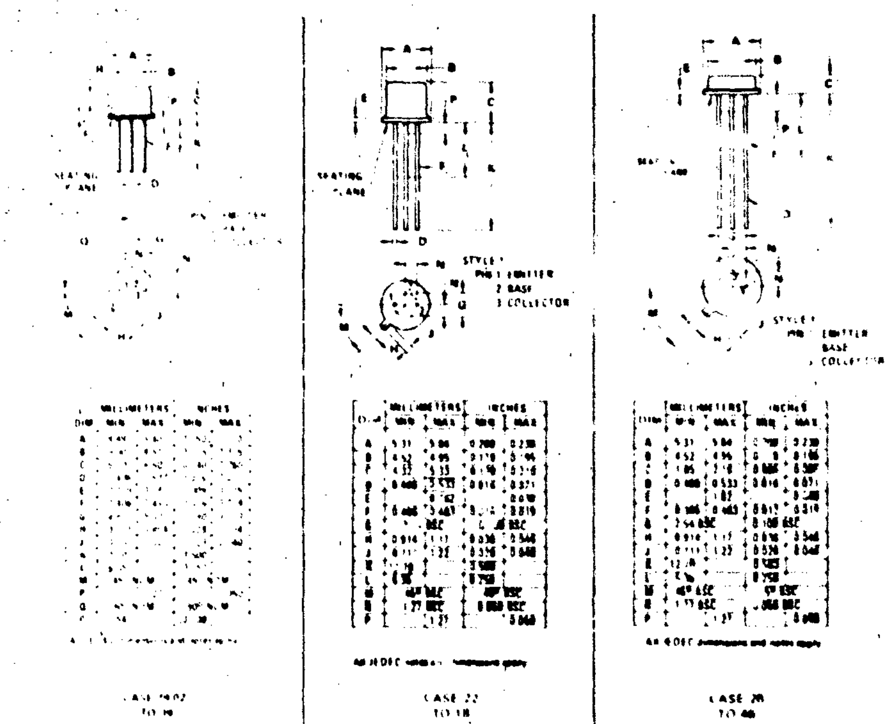


Figure III-5. 2N2222A Manufacturer Specification Sheets (Continued)

2N2218S,AS, 2N2219S,AS, 2N2221,A, 2N2222,A, 2N5581, 2N558? (continued)

OUTLINE DIMENSIONS



2N2223, A

For Specifications, See 2N2060 Data.

Figure III-5: 2N2222A Manufacturer Specification Sheets (Concluded)

d) Example - 2N2222A

The curve tracer photograph presented in figure III-6 shows the inverse characteristic of a 2N2222A transistor. The point chosen to model was $I_E = 4$ mA and $V_{EC} = 2$ V. The nearest corresponding point is:

$$V_{EC} = 2\ V,\ I_E = 4.4\ mA,\ I_B = 5(100\ \mu A) = 500\ \mu A$$

$$\beta_I = \frac{4.4\ mA}{500\ \mu A} = 8.8$$

$$\alpha_I = \frac{8.8}{(1 + 8.8)} = 0.898$$

3) I_S

a) Definition

I_S is the transistor saturation current. It is defined by the reciprocity relation:

$$I_S = \alpha_F\ I_{ES} = \alpha_I\ I_{CS}$$

b) Typical Value

I_S is proportional to the emitter-base junction area and may vary significantly between device types. A typical value is 10^{-16} amperes.

c) Measurement

I_S can be found by measuring I_C at $V_{BC} = V_{BE}$. This cannot be done by shorting the base to collector. One method is to display collector current versus collector-emitter voltage at a constant value of base-emitter voltage. I_S is then the measured value of I_C divided by the value of exp (qV_{BE}/KT). The information required to

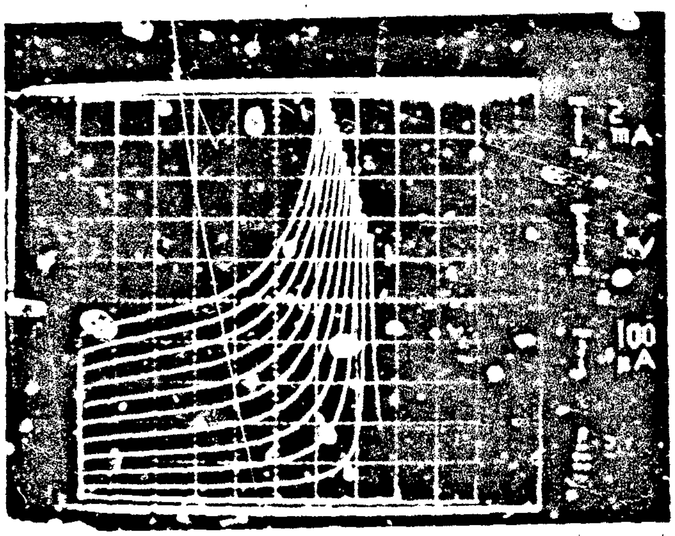


Figure III-6. 2N2222A Inverse Characteristics

compute I_S (I_C at $V_{CE} = V_{BE}$) may be available in the manufacturer specification sheets.

d) Example - 2N2222A

1 From Measurement

I_S was obtained from the photograph shown in figure III-7.

$$V_{CE} = V_{BE} = 0.6 \text{ volt}$$

$$I_C = 0.38 \text{ mA}$$

$$I_S = \frac{0.38 \text{ mA}}{\exp \frac{0.6 \text{ V}}{0.0259 \text{ V}}} = 3.30 \times 10^{-14} \text{ amperes}$$

2 From Data Sheets

I_S can be obtained from the manufacturer specification sheets shown in figure III-5. The "On" voltage plot yields a point where $V_{BE} = V_{CE} = 1$ volt. At this point, $I_C = 430$ mA.

$$I_S = \frac{430 \text{ mA}}{\exp \frac{1 \text{ V}}{.0259 \text{ V}}} = 7.33 \times 10^{-18} \text{ amperes}$$

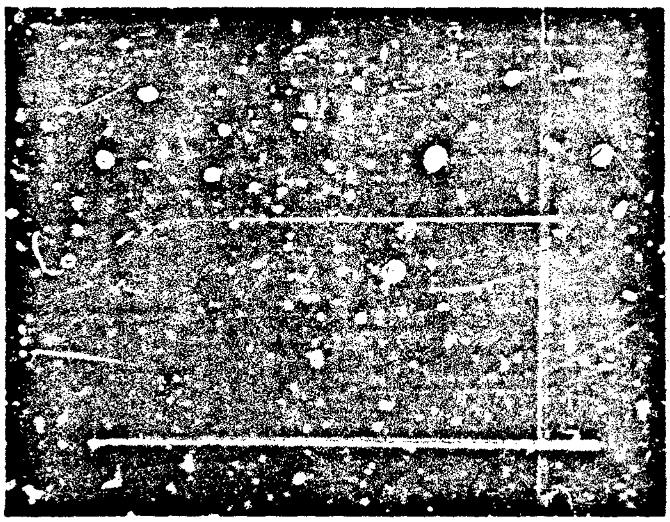
4) T

See discussion of T in chapter II.a.1.

2. Modeling Breakdown

a. Description

An important characteristic of transistor models is their behavior in an electrical overstress environment. Even before the onset of breakdown, the collector multiplication effects seriously alter the behavior of the transistor.



VERT:
0.1 mA/div
HORIZ:
0.1 V/div
V_{BE} = 0.6 V

Figure III-7. I_C Versus V_{CE}

b. <u>Advantages</u>

Addition of the breakdown characteristic to the transistor model improves simulation accuracy of the model. Inclusion of the breakdown characteristic will allow the prediction of transistor failure by overheating.

c. <u>Cautions</u>

Model complexity and simulation time will increase with the inclusion of the breakdown characteristic.

d. <u>Characteristics</u>

Breakdown can be simulated with the inclusion of the two current generators shown in figure III-8.

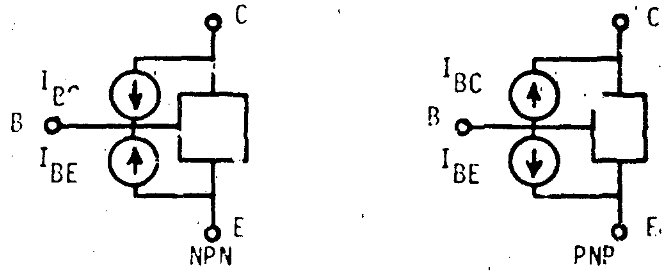


Figure III-8. Inclusion of Breakdown

The characteristic produced when the breakdown generators are included is shown in figure III-9.

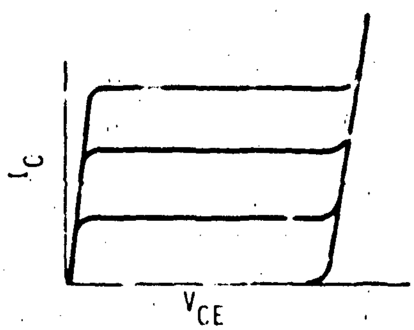


Figure III-9. Avalanche Breakdown

e. Defining Equations

$I_{BC} = I_C (M_C - 1)$

$I_{BE} = I_E (M_E - 1)$

$$M_C = \frac{1}{1 - \left(\frac{V_{BC}}{BV_{CBO}}\right)^{N_C}}$$

$$M_E = \frac{1}{1 - \left(\frac{V_{BE}}{BV_{EBO}}\right)^{N_E}}$$

f Parameterization (BV_{CBO}, BV_{EBO}, N_C, N_E)

1) Definition

BV_{CBO} is the collector-to-base breakdown voltage BV_{EBO} is the emitter-to-base breakdown voltage. N_C and N_E are the constants which model the multiplication region of the collector-base and base-emitter junctions, respectively.

2) Typical Values

BV_{CBO} and BV_{EBO} may vary from less than 5 volts to over 2000 volts. N_C and N_E are typically between 2 and 4 for silicon devices.

3) Measurement

BV_{CBO} and N_C may be determined with the aid of BV_{CEO}. BV_{CEO} is the maximum voltage in the common-emitter configuration with the base lead open. BV_{CBO} is the maximum voltage in the common-base configuration with the emitter lead open. N_C may be determined through use of the expression:

$$N_C = \frac{\log \beta_F}{\log\left(\frac{BV_{CBO}}{BV_{CEO}}\right)}$$

BV_{EBO} and N_E may be determined in a similar manner through use of BV_{EBO}, BV_{ECO}, and β_I.

4) Example 2N2222A

a) From Measurement

BV_{CBO} was determined from the photograph shown in figure III-10. The breakdown voltage can be seen to be 102 volts.

From the $I_B = 0$ trace shown in figure III-4, BV_{CEO} was found to be 59 volts. N_C may now be calculated as:

$$N_C = \frac{\log 30}{\log\left(\frac{102\ V}{59\ V}\right)} = 9.93$$

The photograph shown in figure III-11 allows determination of BV_{EBO}. This voltage can be seen to be 8.4 volts. Figure III-6 yields a BV_{ECO} of 7.6 volts.

$$N_E = \frac{\log 8.8}{\log\left(\frac{8.4\ V}{7.6\ V}\right)} = 21.73$$

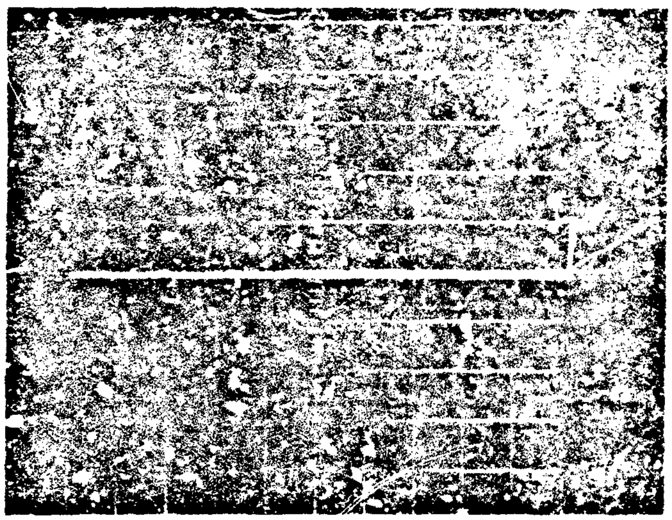
b) From Data Sheets

The manufacturer specification sheets (figure III-5) list a max/min β_F of 100-300, a minimum BV_{CEO} of 40 volts, and a minimum of BV_{CBO} of 75 volts. Choosing $\beta_F = 200$,

$$N_C = \frac{\log 200}{\log\left(\frac{75\ V}{40\ V}\right)} = 8.43$$

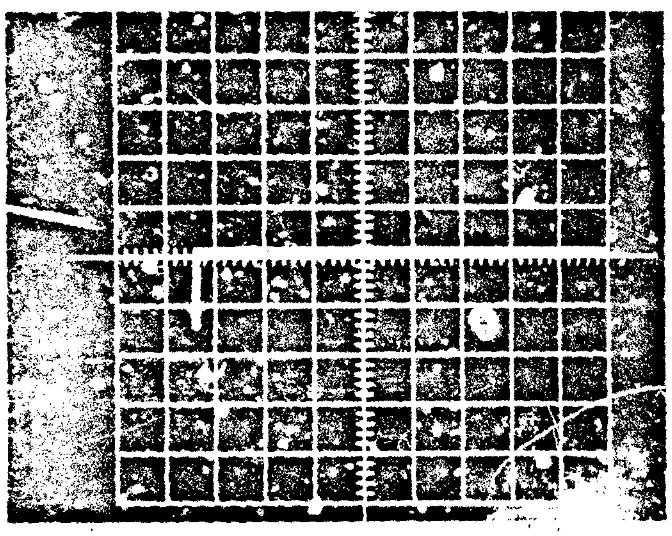
g. Example Computer Run

To simultaneously obtain the characteristic of the example basic transistor model and the avalanche breakdown characteristic, the general purpose transistor model was made to produce a "curve tracer" characteristic. The model was exercised by SCEPTRE. An incremental base current was produced using the RERUN feature. The test circuit is demonstrated in figure III-12. The input listing for this run is given in figure III-13. The results from this run were plotted to give figure III-14. These results may be compared to the photograph shown in figure III-4.



HORIZ:
10 V/DIV
VERT:
50 [illegible]A/DIV

Figure III-10. Collector-Base Reverse Characteristics



HORIZ:
1 V/div
VERT:
10 μA/div

Figure III-11. Emitter-Base Reverse Characteristics

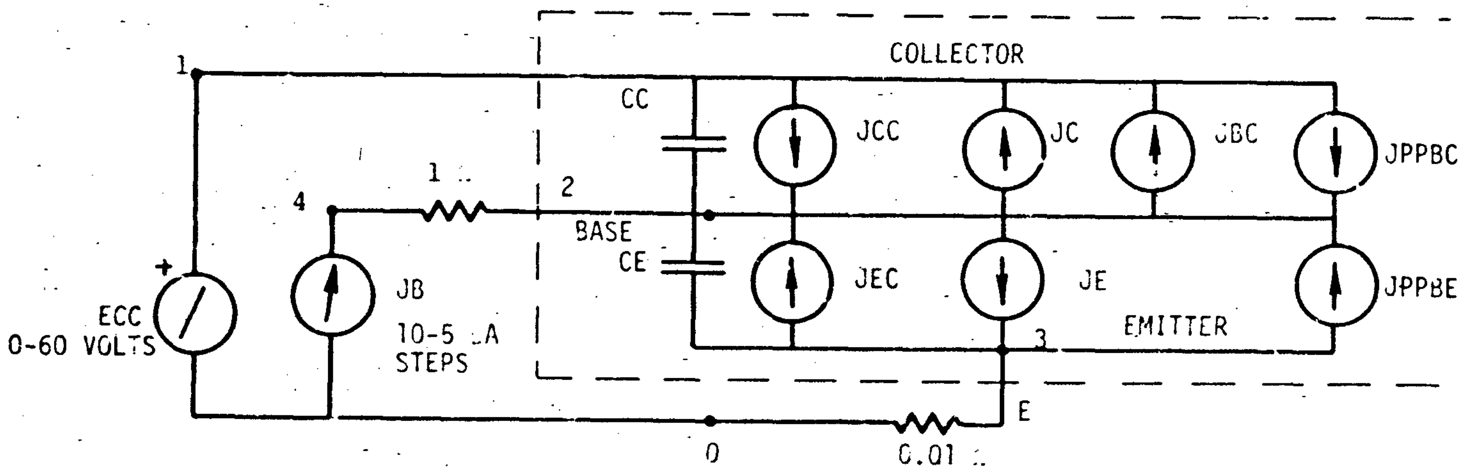


Figure III-12. Test Circuit

```
S C E P T R E   NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2         5/75
 02/28/78      08.57.55.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD "DOCUMENT" AS THE FIRST CARD
OF THE INPUT TEXT

COMPUTER TIME ENTERING SETUP PHASE-
          CPA         .388 SEC.
          PP         0.000 SEC.
          IO         0.000 SEC.


CIRCUIT DESCRIPTION
ELEMENTS
EC1,0-1=TABLE 1(TIME)
JCC,1-2=X1(3.30E-14*(EXP(38.61*VJE)-1.))
JEC,3-2=X4(3.30E-14*(EXP(38.61*VJC)-1.))
JC,2-1=Q1(JEC,0.995)
JE,2-3=Q1(JCC,0.99567)
JBC,1-2=Q2(JCC,VJBC,102.,3.93)
JPPBC,1-2=TABLE 2(TIME)
JPPBE,3-2=0
CC,1-2=1.E-12
CE,3-2=1.E-12
JB,0-4=0
RB,4-2=1.
RBIAS,3-0=0.01
OUTPUTS
IECC,PLOT(ECC)
IECC,JBC,JB,ECC
FUNCTIONS
Q1(A,B)=(A/B)
Q2(A,B,C,D)=(A*(1./(1.-AMIN1(.9999,(ABS(B/C))**D)))-1.))
TABLE 1
0,0,11.E-3,60
TABLE 2
0,0,1,0
RUN CONTROLS
STOP TIME=11.E-3
MINIMUM STEP SIZE=1.E-39
MAXIMUM PRINT POINTS=100
RERUN DESCRIPTION(10)
ELEMENTS
JB=5.E-6,10.E-6,15.E-6,20.E-6,25.E-6,
30.E-6,35.E-6,40.E-6,45.E-6,50.E-6
END
SYSTEM NOW ENTERING SIMULATION
```

Figure III-13. SCEPTRE Input for Basic Transistor and Breakdown

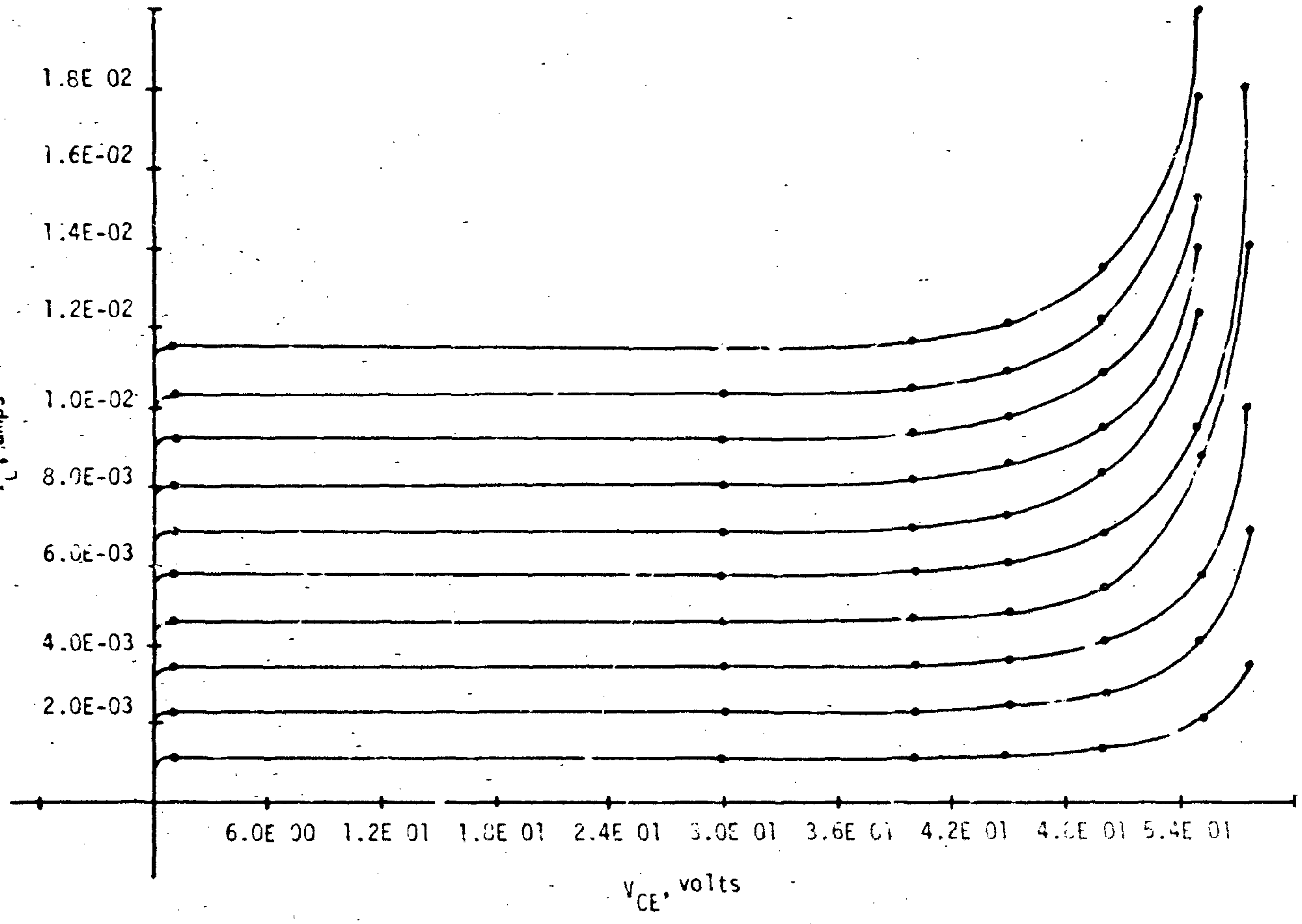


Figure III-14. EM_1 Characteristics

3. Addition of Charge Storage Elements and Ohmic Resistance

a. Description

The addition of ohmic resistance, diffusion capacitance, and depletion capacitance to the basic transistor model forms what may be described as the general purpose transistor model. The general purpose transistor model is the model commonly included in model libraries and in the internal transistor models of circuit analysis codes.

b. Advantages

The general purpose transistor model may be applied to transient analyses. The model represents a good compromise between accuracy, ease of parameterization, speed, and useful results.

c. Cautions

A large amount of time is required to develop the extra parameters required for the general purpose transistor model. Sophisticated electronic measurement equipment is also required.

d. Characteristics

The placement of the parasitic capacitors and resistors is shown in figure III-15.

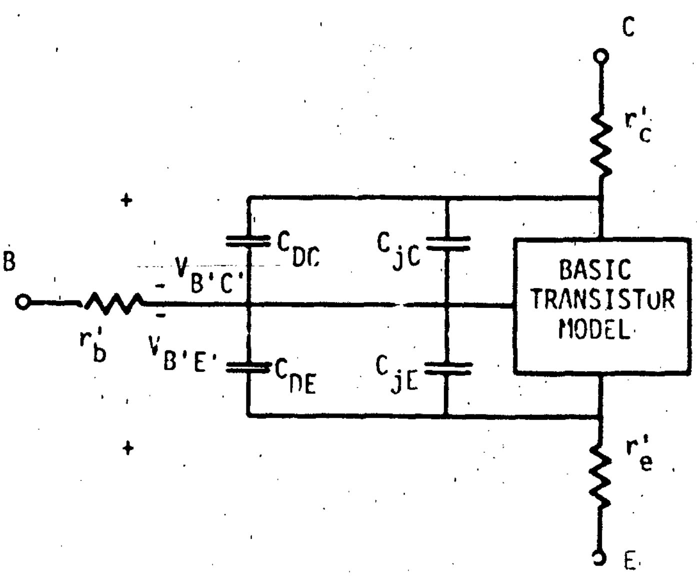


Figure III-15. Inclusion of Parasitic Element (NPN)

The effect of r_c' on the model characteristic is illustrated in figure III-16.

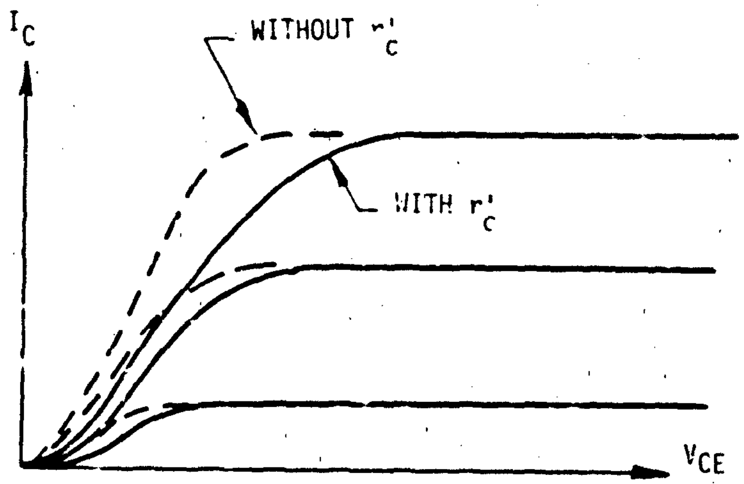


Figure III-16. Effect of r_c'

The effect of r_b' and r_e' on the model characteristic is illustrated in figure III-17.

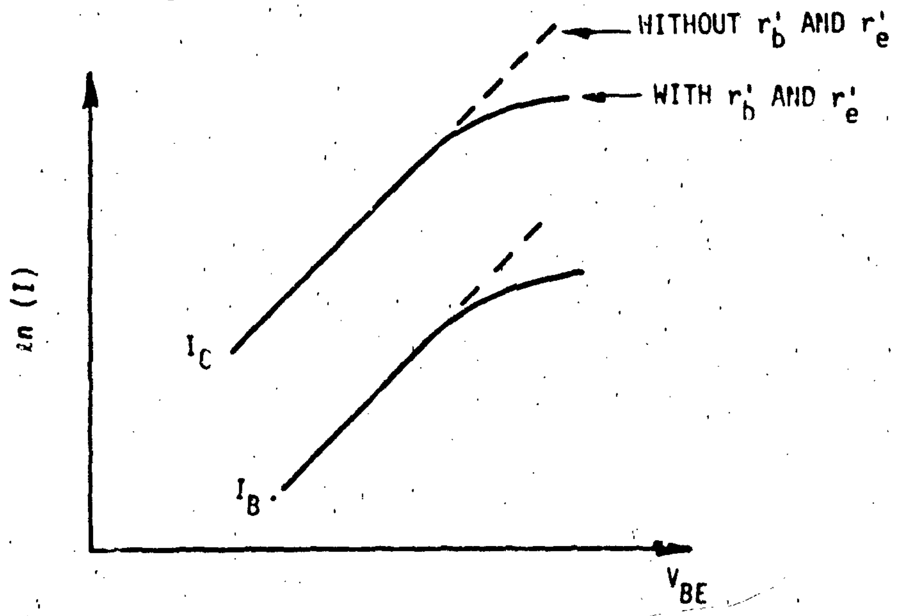


Figure III-17. Effect of r_b' and r_e'

The depletion capacitors model the stored charge associated with the junction transition regions (see chapter II). The variations of these capacitors with voltage is illustrated in figure III-18. The diffusion capacitors model the stored charge in the collector, base, and emitter regions which must be removed during switching. The minority charge distribution before and after switching is illustrated in figure III-19. In the figure, all the charge represented by the difference in the shaded areas between the two biases must be removed during the change in bias. This mobile charge, therefore, is also stored charge.

e. Defining Equations

$$C_{jE} = \frac{C_{jeo}}{\left(1 - \frac{V_{B'E'}}{\psi_E}\right)^{m_E}}$$

$$C_{jC} = \frac{C_{jco}}{\left(1 - \frac{V_{B'C'}}{\psi_C}\right)^{m_C}}$$

$$C_{DE} = \frac{q}{KT} \tau_F (I_{CC} + I_S)$$

$$C_{DC} = \frac{q}{KT} \tau_R (I_{EC} + I_S)$$

f. Parameterization

1) r'_e

a) Definition

r'_e is a constant valued resistor which models the resistance between the emitter region and the emitter terminal.

b) Typical Value

A typical value of r'_e is 1 ohm.

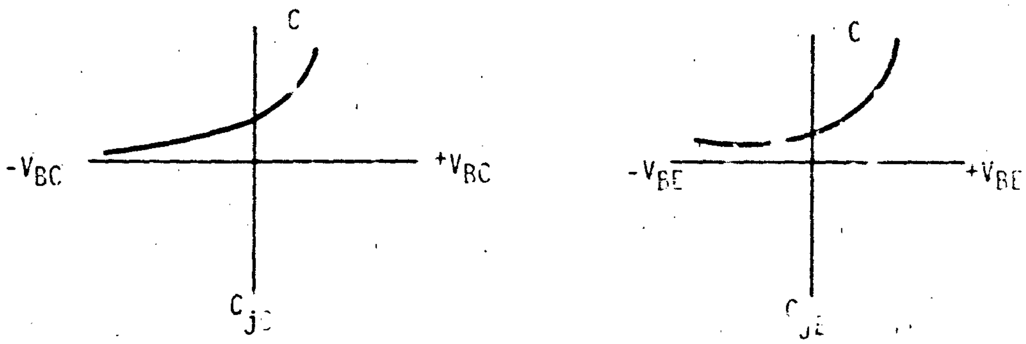
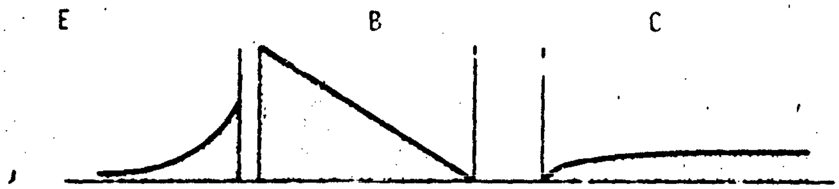
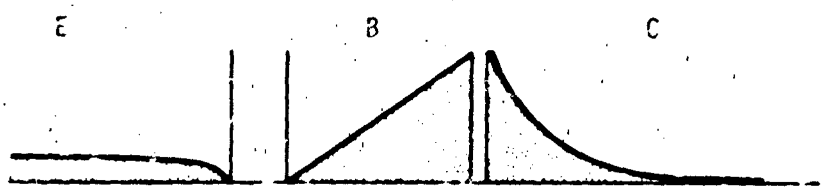


Figure III-18. Voltage Behavior of Junction Capacitance



(a) In Normal Operating Mode



(b) In Inverse Operating Mode

Figure III-19. Minority Charge Distribution in a Biased Transistor

c) Measurement

The value of r'_e can be determined by obtaining the base current as a function of collector-emitter voltage for a transistor with an open-circuited collector. This test configuration is illustrated in figure III 20. The straight line portion of the curve is $1/r'_e$. The low current "flyback" effect is caused by the decrease of inverse α at low currents. The slope should be determined as closely as possible to the flyback region.

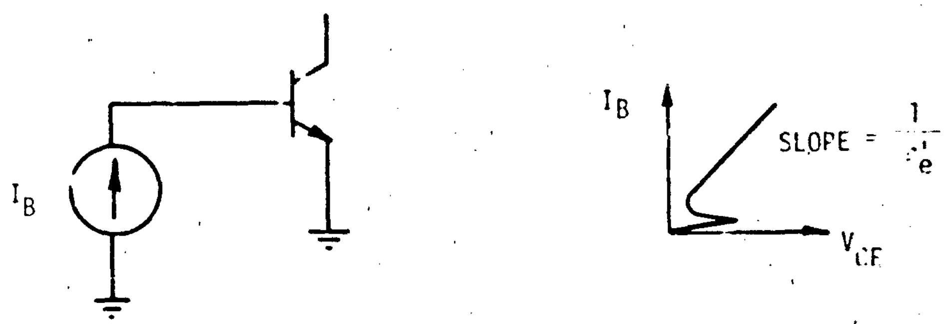


Figure III-20. Setup to Measure r'_e

d) Example - 2N2222A

r'_e was obtained from the photograph shown in figure III-21. ΔV of the straight line portion of this curve is about 20 mV, and ΔI is about 80 mA.

$$r'_e = \frac{20\ \text{mV}}{80\ \text{mA}} = 0.25\ \Omega$$

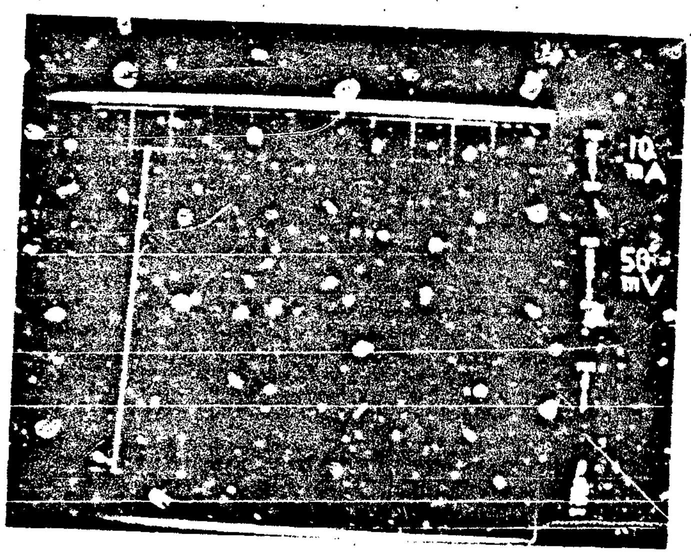


Figure III-21. Determination of r_e'

2) r_c'

a) Definition

r_c' models the resistance between the collector region and the collector terminal. r_c' is actually a current dependent resistor, but is usally modeled as a constant valued resistor.

b) Typical Value

A typical value of r_c' is 10 ohms.

c) Measurement

r_c' may be obtained from a curve tracer photograph at low values of V_{CE}. The two limiting values of r_c' are r'_{CSAT} and $r'_{CNORMAL}$. These resistance values are obtained from the transistor characteristic as illustrated in figure III-22. The $r'_{CNORMAL}$ line is drawn through the "knees" of the characteristic. The choice of r_c' depends on how the transistor is biased. Generally, a single value of r_c' between r'_{CSAT} and $r'_{CNORMAL}$ is chosen.

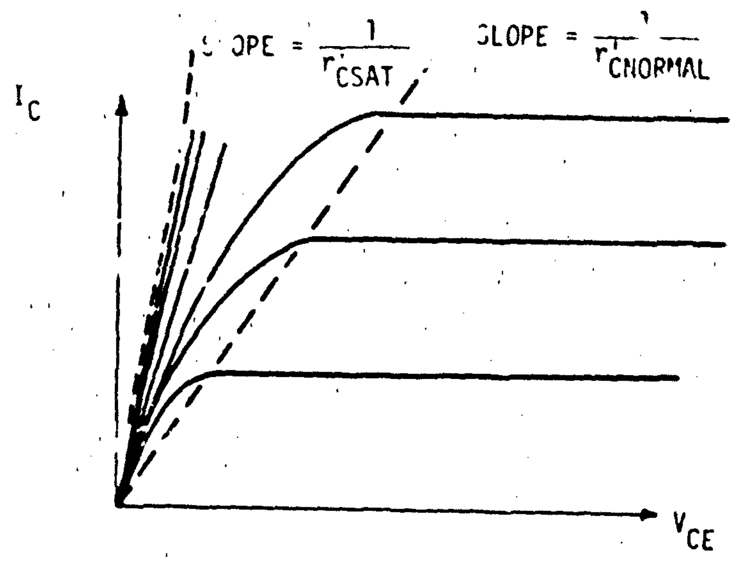


Figure III-22. Method of Determining r_c'

d) Example - 2N2222A

1 From Measurement

r'_c was determined from the curve tracer photograph shown in figure III-23. r'_{CSAT} is approximately:

$$\frac{100 \text{ mV} - 50 \text{ mV}}{4 \text{ mA} - 1 \text{ mA}} = 16.7 \text{ ohms}$$

$r'_{CNORMAL}$, the inverse of the slope of the line passing through the knees, is about:

$$\frac{200 \text{ mV} - 150 \text{ mV}}{4.5 \text{ mA} - 0.5 \text{ mA}} = 12.5 \text{ ohms}$$

r'_c was chosen to be the average of the two resistance values, rounded to 15 ohms.

2 From Data Sheets

r'_c may be estimated from the manufacturer specification sheets by application of:

$$r'_c = \frac{V_{CESAT} - 0.2 \text{ V}}{I_C}$$

where 0.2 V is a typical value of ideal saturation voltage allowing the ohmic voltage drop to be estimated. I_C should be the highest current available on the data sheets.

3) r'_b

a) Definition

r'_b models the resistance between the base region and the base terminal. r'_b varies with the operating point of the transistor but is generally given a constant value.

b) Typical Value

A typical value for r'_b is 100 ohms.

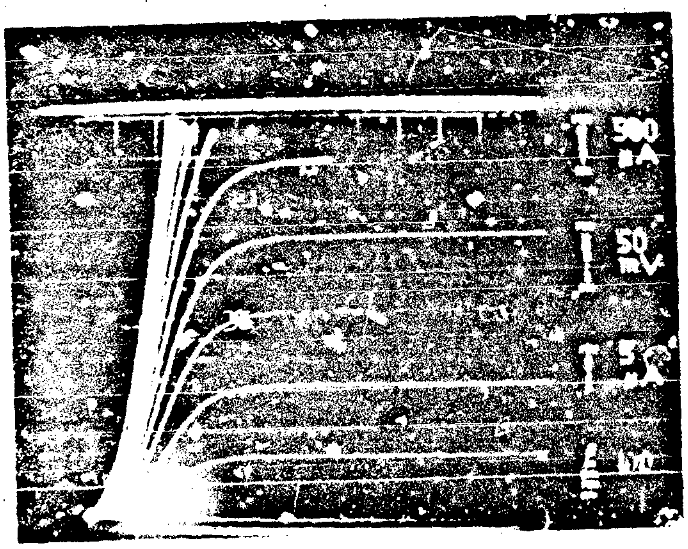


Figure III-23. Obtaining r_c'

c) Measurement

r_b' is a difficult parameter to measure because it is modeled as a lumped constant resistance although it is actually a distributed variable resistance. The value obtained for r_b' depends strongly on the measurement technique used as well as the transistor's operating conditions. Some measurement techniques are discussed below.

1 Pulse Measurement Method

This was the method applied for the example determination of r_b'. The test circuit required is shown in figure III-24. The current pulse applied to the base causes the device to turn off. The voltage across r_b' drops to zero while the base capacitance keeps the junction potential, V_{BE}, constant. r_b' can then be determined by:

$$r_b' = \frac{\Delta V_{BE}}{I \text{ pulse generator}}$$

When the voltage drop no longer appears vertical on an oscilloscope trace, the constant-resistance model for r_b is no longer valid. Adjusting the time base of the oscilloscope until this condition is reached gives some indication of the switching times at which the simple r_b' model is not adequate.

2 Noise Measurement Technique

This technique is difficult for those who do not have experience with noise measurement.

If flicker noise is assumed to be negligible, r_b' can be estimated as:

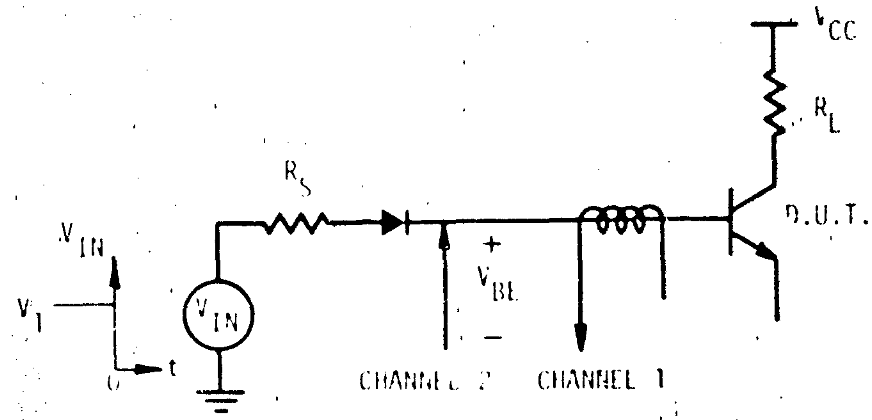
$$r_b' = \frac{\overline{(Vi^2)}}{(4\ KT\ \Delta f)} - \frac{1}{2\ g_{mF}}$$

where:

Δf = the bandwidth of the measurement

g_{mF} = calculation from the known collector current

$\overline{Vi^2}$ = the transistor's equivalent input mean square voltage



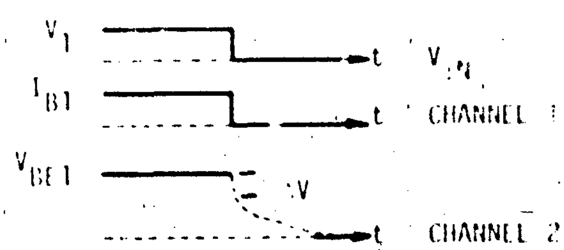


Figure III-24. Measurement Setup to Determine r_b' by the Pulse Method

The magnitude of Vi^2 is determined from:

$$Vi^2 = \frac{\overline{Vo^2}}{G^2}$$

where:

Vo^2 = the measured output mean square noise voltage from the test system

G = the voltage gain from the test device in ac ... system output

This measurement is performed with an ac short circuit between the transistor's base and emitter. Also, Vo^2 must be read on a true rms voltmeter.

3 dc Measurement Technique

A plot of log (I_B) versus V_{BE} (V_{BC} = 0) over a wide range of currents yields a straight line which begins to become nonlinear at the higher currents. The voltage deviation from the straight line is:

$$\Delta V = I_B \, r_b' + I_E \, r_e'$$

This effect is considered in greater detail in section B.4 of this chapter. Knowing the more easily obtainable parameters r_e', I_B, and I_C (I_E = $I_C + I_B$), r_b' may be obtained.

4 Estimation From Data Sheets

r_b' may be estimated from the manufacturer specification sheets as:

$$r_b' = \frac{V_{BESAT} - 0.6 \text{ V}}{I_B}$$

where 0.6 V represents a diode voltage drop and I_B is the highest available base current on the data sheets.

d) Example - 2N2222A

1 From Measurement

r_b' was determined using the setup of figure III-24. A current probe of 50 mV/mA was used to obtain base current. V_{CC} was set to 10 V, R_L was 100 Ω, and a Schottky barrier diode (1N6263) acted as the clamping diode. The result obtained is shown in the photograph presented in figure III-25. The top trace is from the current probe and corresponds to 10 mV/div. The bottom trace is V_{BE} and corresponds to 20 mV/div. I_B is a positive pulse from ground. Therefore:

$$I_B = 10 \text{ mV} \left(\frac{1}{50 \frac{\text{mV}}{\text{mA}}} \right) = 0.2 \text{ mA}$$

ΔV is the rapid voltage decline at the end of the current pulse.

$$\Delta V = 20 \text{ mV}$$

$$r_b' = \frac{20 \text{ mV}}{0.2 \text{ mA}} = 100 \text{ ohms}$$

2 From Data Sheets

The data sheets shown in figure III-5 list a V_{BESAT} of 2.0 V max at a base current of 50 mA.

$$r_b' = \frac{2.0 \text{ V} - 0.6 \text{ V}}{50 \text{ mA}} \doteq 28 \text{ ohms}$$

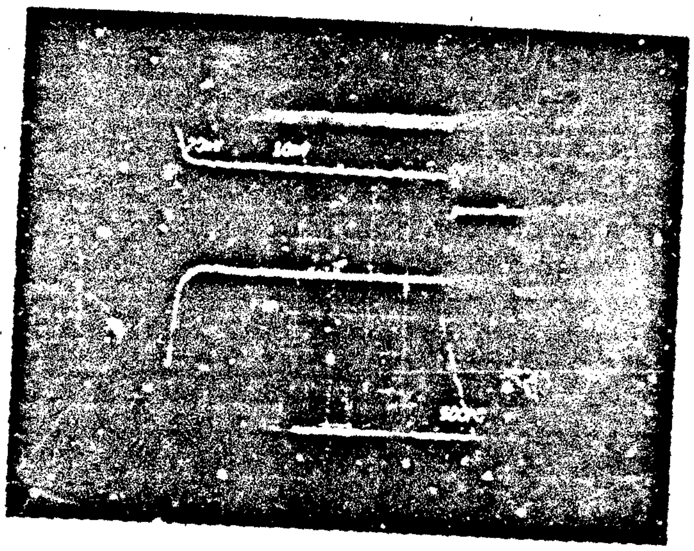


Figure III-28. Determining r_b'

4) C_{jo}, ψ, m

a) Definition

C_{jo}, ψ, and m are the three parameters which describe the transistion capacitance associated with the collector-base junction or the base-emitter junction. The two capacitors are nonlinear and voltage dependent.

b) Typical Value

A typical value of C_{jo}, ψ, and m are 10 pF, 0.6 V, and 0.5, respectively.

c) Measurement

C_{jeo}, ψ_E, and m_E are determined by capacitance measurements between the base terminal and the emitter terminal with the collector terminal open. The voltage $V_{B'E'}$ is adjusted so the junction is reverse biased.

C_{jco}, ψ_C, and m_C are determined by capacitance measurement between the base terminal and the collector terminal with the emitter terminal open. Again, the junction should not be forward biased.

The data obtained should be reduced using the graphical techniques discussed in chapter II.B.6.

It may be necessary to subtract out a constant capacitance from the measured value. This extra capacitance term is usually around 0.5 pF and is the stray capacitance associated with the transistor package (C_k).

d) Example 2N2222A

1 C_{jeo}, ψ_E, m_E, From Measurement

Base-emitter capacitance measurements with a Boonton 700A capacitance bridge at different bias values produced the data shown in table III-2.

TABLE III-2. EXPERIMENTAL EMITTER CAPACITANCE VALUES

V_{BE}	C_{jE}
0 volts	22.62 pF
-0.1	21.55
-0.2	20.66
-0.3	19.91
-0.5	18.68
-0.7	17.70
-1.0	16.53
-2.0	14.00
-3.0	12.48
-5.0	10.56

The initial guess for ψ is 0.6 volt, and the initial guess for C_K is 0.5 pF. The data reduce to the values shown in table III-3.

TABLE III-3. REDUCED EMITTER CAPACITANCE DATA

$(\phi\text{-}V)$	$(C_{meas} - C_K)$
0.6 V	22.12 pF
0.7	21.05
0.8	20.15
0.9	19.41
1.1	18.18
1.3	17.20
1.6	16.03
2.6	13.50
3 6	11.98
5.6	10.06

The results are plotted in figure III-26. The resulting line is straight enough to be considered an adequate fit. The value of -m is the inverse slope of the line and can be calculated from two points as:

$$-m = \frac{\log 22.12 \text{ pF} - \log 11.98 \text{ pF}}{\log 0.6 \text{ V} - \log 3.6 \text{ V}}$$

$$m = +0.342$$

indicating a nearly perfect linear doping gradient.

C_{jeo} can be calculated from the capacitance formula and a single raw data point as:

$$C_{jeo} = C_{jE} \left(1 - \frac{V_{BE}}{\psi_E}\right)^{m_E}$$

Choosing the 1.0 V point,

$$C_{jeo} = 16.53 \text{ pF} \left[1 - \frac{(-1.0 \text{ V})}{0.6 \text{ V}}\right]^{0.342}$$

$$C_{jeo} = 23.12 \text{ pF}$$

this compares favorably to the measured value of C_{jeo} which is 22.62 pF.

2 From Data Sheets

The specification sheets for the 2N2222A (figure III-5) plot C_{ib} and C_{ob} as a function of bias. C_{ib} is the emitter junction capacitance. C_{jeo}, ψ_E, and m_E can be found by taking data off of this curve and reducing the data as done previously. C_{ib} data from the plot are shown below.

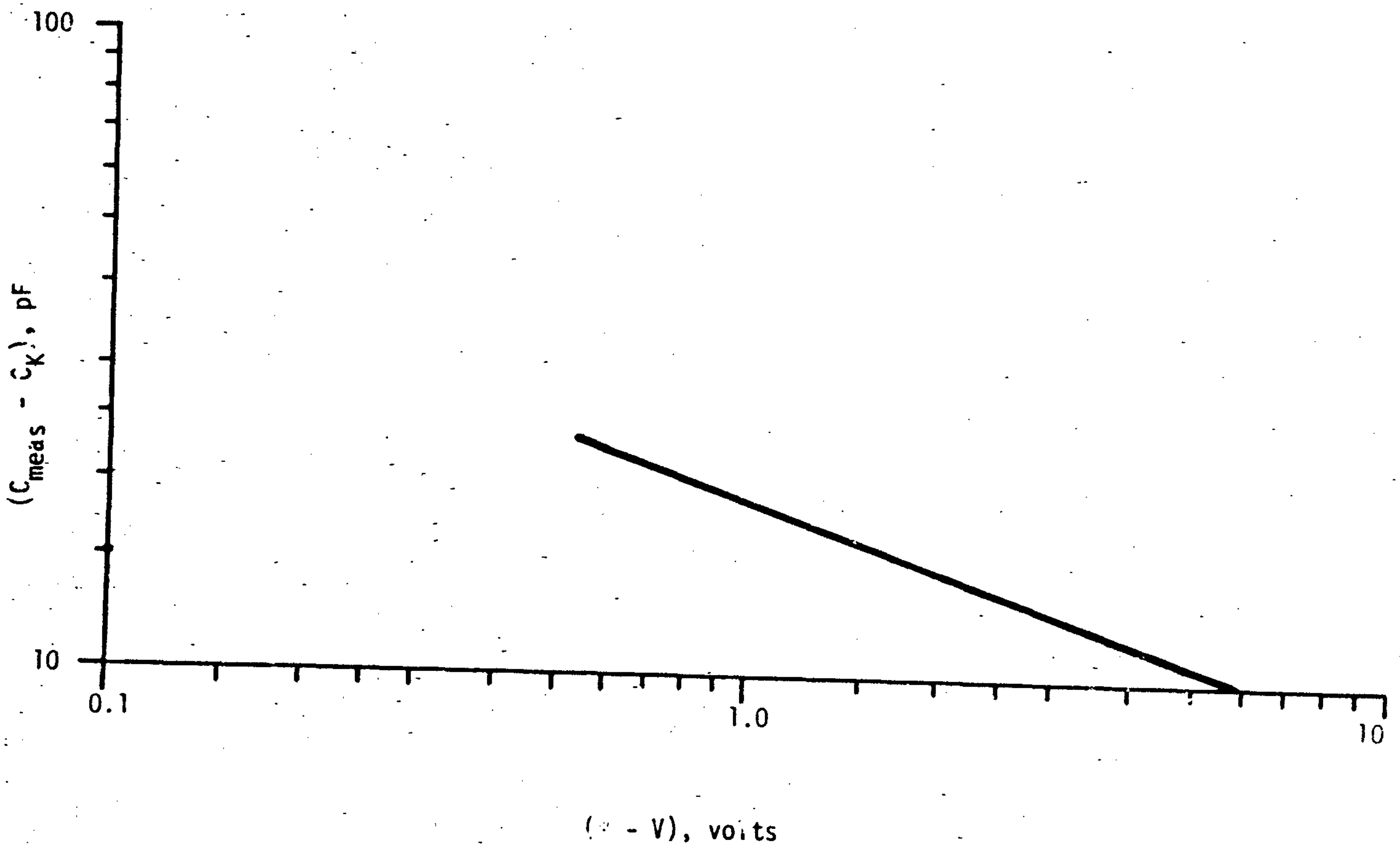


Figure III-26. Reduced C-V Data

V_{BE}	C_{jE}
-0.1 V	25 pF
-0.5	20
-1.5	15

Assuming $\psi = 0.6$ V and $C_K = 0$,

$(\Psi - V)$	$(C\ C_K)$
0.7 V	25 pF
1.1 V	20 pF
2.1 V	15 pF

Again, a straight line results indicating a correct choice of ψ (figure III-27).

$$-m = \frac{\log 25\ \text{pF} - \log 15\ \text{pF}}{\log 0.7\ \text{V} - \log 2.1\ \text{V}} = -0.465$$

which is the m value for a junction with a nearly abrupt doping gradient. This value disagrees to the measured value in terms of how the doping profiles will look.

$$C_{jeo} = 25\ \text{pF}\left[1 - \frac{(-0.1\ \text{V})}{0.6\ \text{V}}\right]^{0.465} = 26.86\ \text{pF}$$

which is about 4 pF higher than the measured value.

3 C_{jco}, ψ_c, m_c From Measurement

Base-collector capacitance measurements with a Boonton 700A capacitance bridge at different bias values produced the data shown in table III-4.

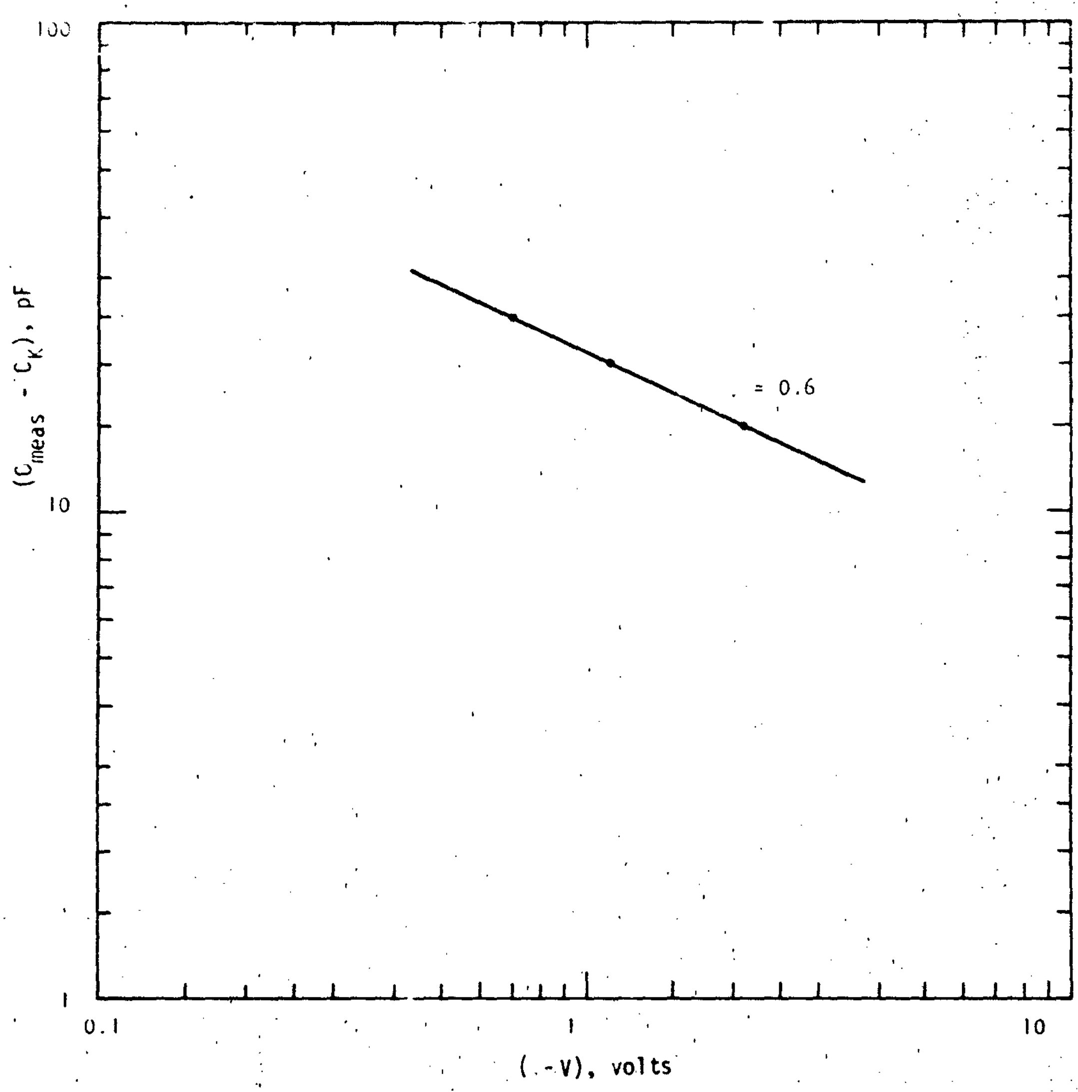


Figure III-27. Reduced C-V Data from Specification Sheet

TABLE III-4. EXPERIMENTAL BASE-COLLECTOR CAPACITANCE VALUES

V_{BC}	C_{jC}
0 V	10.78 pF
-0.1	10.15
-0.2	9.65
-0.3	9.24
-0.5	8.61
-0.7	8.12
-1.0	7.57
-2.0	6.46
-3.0	5.82
-5.0	5.05
-7.0	4.59
-10.0	4.18
-20.0	4.17
-30.0	3.38

The initial guess for ψ is 0.6 volt and the initial guess for C_K is 0.5 pF. The data now reduce to the values shown in table III-5.

TABLE III-5. REDUCED BASE-COLLECTOR CAPACITANCE VALUE

$(\Psi - V)$	$(C_{meas} - C_K)$
0.6 V	10.28 pF
0.7	9.65
0.8	9.15
0.9	8.74
1.1	8.11
1.3	7.62
1.6	7.07
2.6	5.96
3.6	5.32
5.6	4.55
7.6	4.09
10.6	3.68
20.6	3.67
30.6	2.88

The results are plotted in figure III-23. The data seem to form a straight line except for one point which may be a bad data point.

$$-m = \frac{\log 9.65\ \text{pF} - \log 2.88\ \text{pF}}{\log 0.7\ \text{V} - \log 30.6\ \text{V}} = -0.320$$

$$C_{jco} = 9.65\ \text{pF}\left[1 - \frac{(-0.7\ \text{V})}{0.6\ \text{V}}\right]^{0.32}$$

$$C_{jco} = 12.36\ \text{pF}$$

The measured value of C_{jco}, which appeared to be a bad point, was 10.28 pF.

4 C_{jco}, ψ_c, m_c From Data Sheets

The specification sheets given in figure III-5 contain a plot of C_{ob} which corresponds to C_{jC}. C_{jco}, ψ_c, and m_c can be found by taking data off of this curve and reducing the data as indicated previously. C_{ob} data from the plot are shown below.

V_{BC}	C_{jC}
-0.10 V	17 pF
-0.25	15
-0.50	13
-1.25	10
-8.00	6
-15.00	5

Assuming ψ = 0.6 V and C_K = 0,

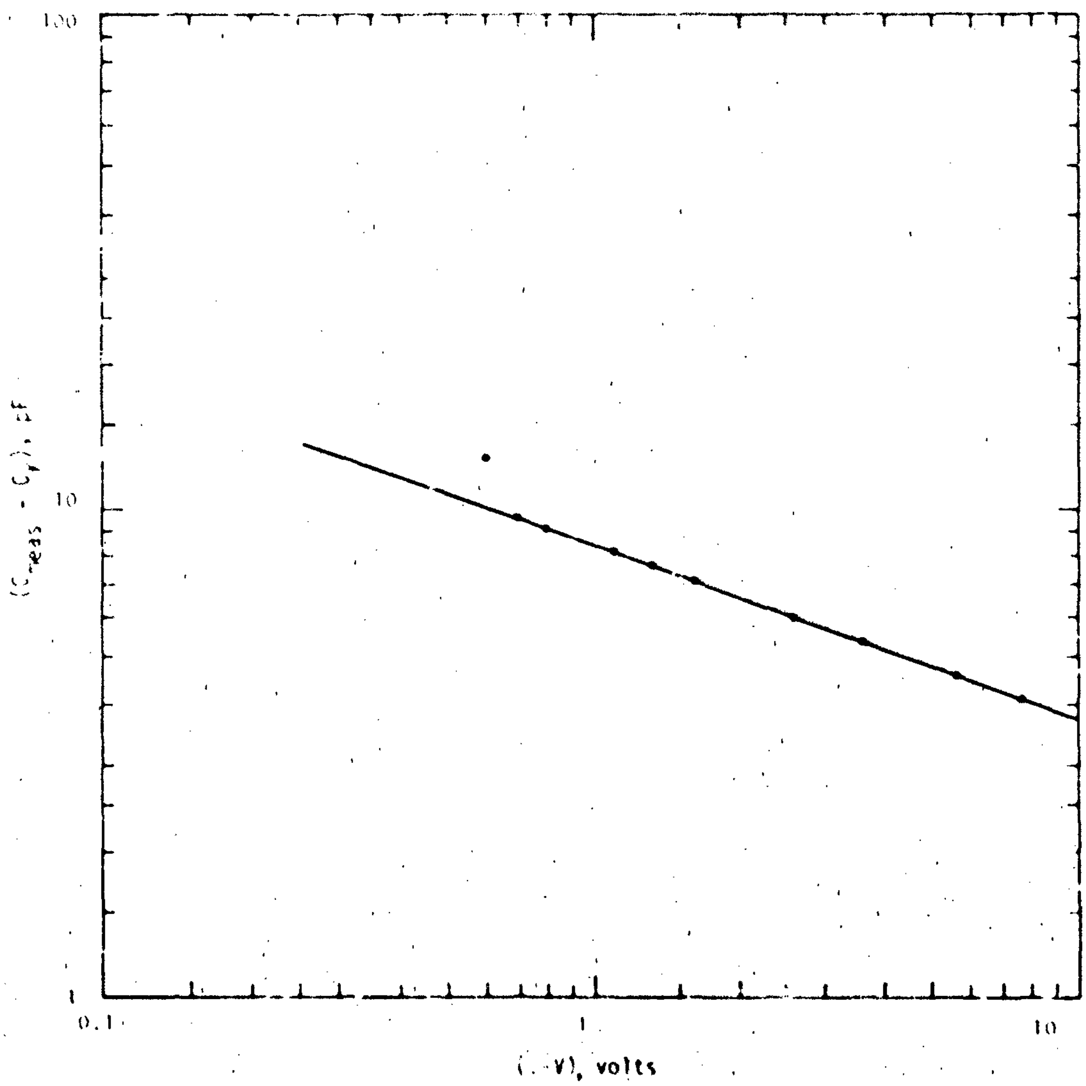


Figure III-28. Reduced C-V Data for Collector Junction

$(\psi - V)$	$(C_{meas} - C_K)$
0.70 V	17 pF
0.85	15
1.10	13
1.85	10
8.60	6
15.60	5

The plot of these data is shown in figure III-29. A definite concave curve is obtained indicating that a smaller value of ψ_c should be tried. Assuming ψ = 0.2 V and C_K = 0,

$(\Psi - V)$	$(C_{meas} - C_K)$
0.30 V	17 pF
0.45	15
0.70	13
1.45	10
8.20	6
15.20	5

The resulting plot, which is a straight line, is shown in figure III-30.

$$-m = \frac{\log 17\text{ pF} - \log 6\text{ pF}}{\log 0.3\text{ V} - \log 8.2\text{ V}} = -0.315$$

$$C_{Jco} = 15\text{ pF}\left[1 - \frac{(-0.1\text{ V})}{0.2\text{ V}}\right]^{0.315} = 17.04\text{ pF}$$

The values of ψ, m, and C_{jco} obtained from direct measurement are:

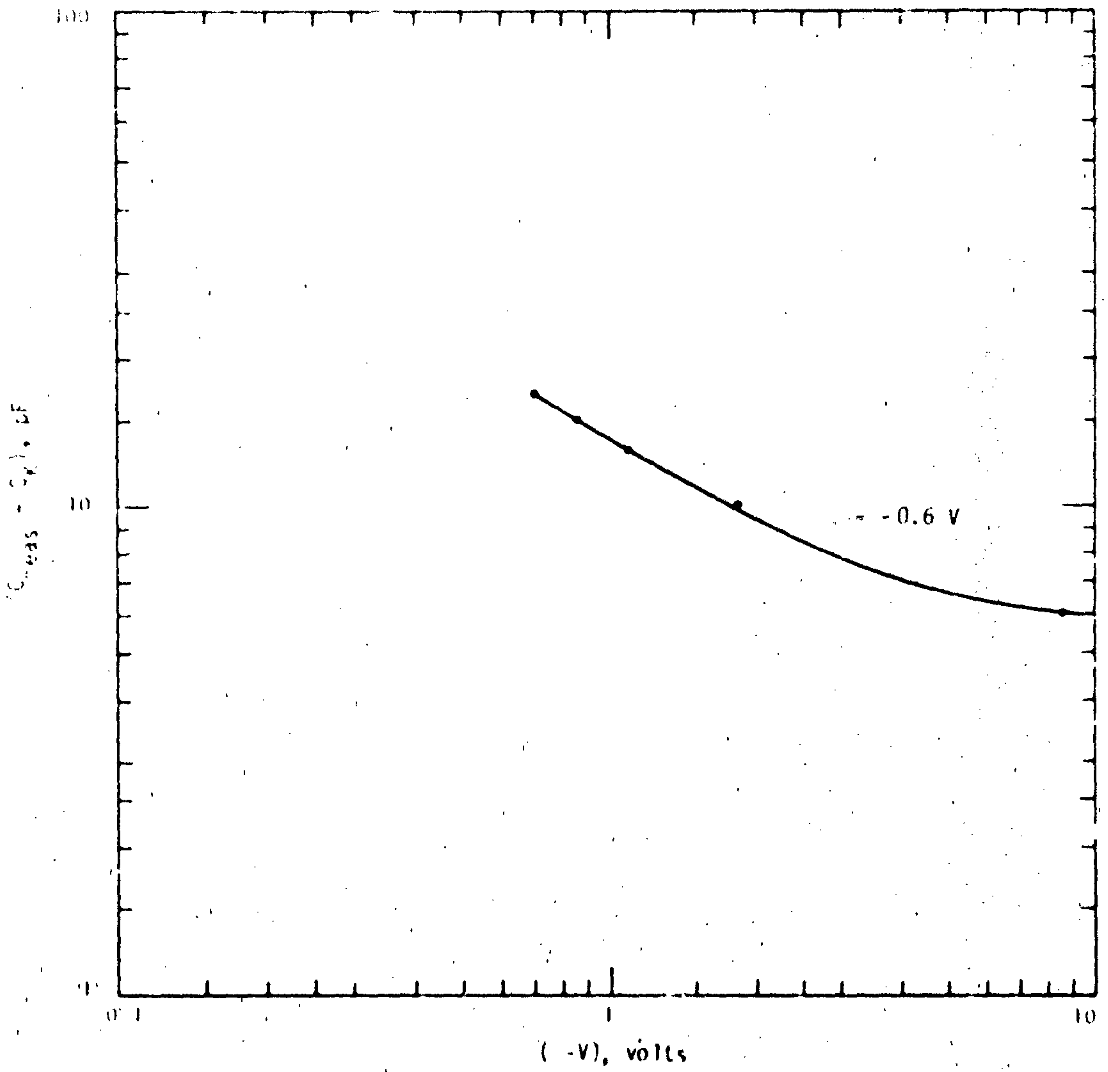


Figure III-29. Reduced Collector C-V Data Obtained from Specification Sheet

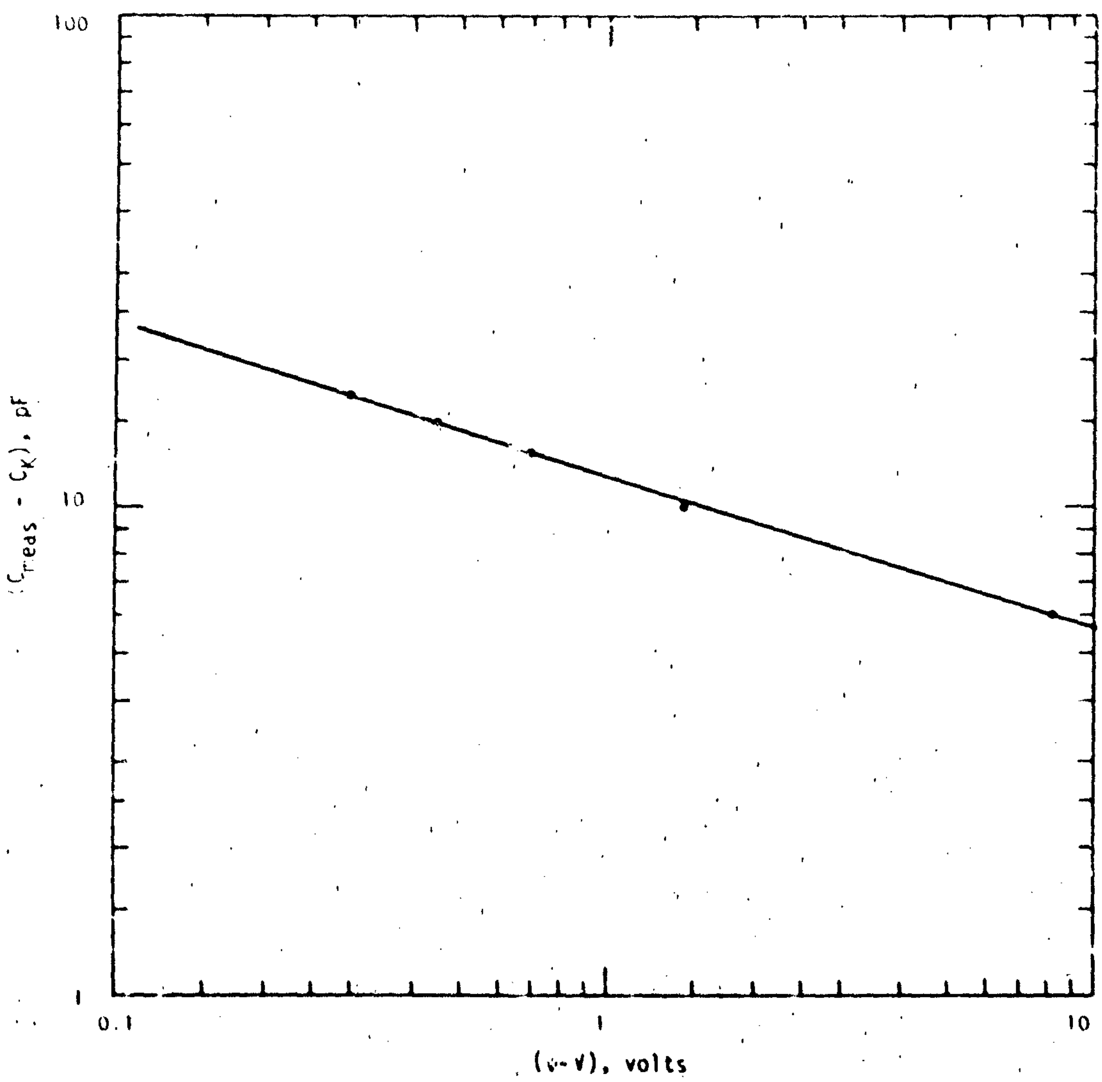


Figure III-30. Reduced C-V Data with New ψ

$\varphi_c = 0.6$ V

$m = 0.320$

$C_{jco} = 12.36$ pF

5) τ_F

a) Definition

τ_F is the total transit time. τ_F is used to model the charge stored in the transistor when the base-emitter junction is forward biased. The element used to model the stored charge is the diffusion capacitor C_{DE}.

b) Typical Value

A typical value of τ_F is 0.1 nanoseconds.

c) Measurement

τ_F may be determined from f_T, the transistor's unity-gain frequency. f_T is the frequency at which the common emitter, zero load, small signal current gain extrapolates to unity.

f_T varies with collector current. In a region where f_T varies little with I_C, τ_F is given by:

$$\tau_F = \left(\frac{1}{2\pi\, f_T}\right) - C_{jC}\, r'_c$$

When f_T varies strongly with I_C, plot $1/f_T$ as a function of $1/I_C$ and extrapolate the straight line portion of the line to $1/I_C = 0$. The frequency value obtained is f_A. τ_F is now found as:

$$\tau_F = \frac{1}{2\pi}\left(\frac{1}{f_A}\right) - C_{jC}\,(V_{B'C'})\, r'_e$$

τ_F is also equal to:

$$\tau_F = \frac{t_r}{(\beta_F + 1)}$$

where t_r is the collector current risetime.

Some techniques of determining f_T are:

(1) An f_T meter.

(2) Small signal measurement. The test setup for this method is shown in figure III-31. The transistor is biased to the desired operating point. The frequency is increased incrementally until β decreases to $\beta_0/2$. The frequency at which this occurs is f_β. From the one pole rolloff transistor model, f_T will be:

$$f_T = \beta_0 f_\beta$$

It is important that the impedance in the collector circuit be as small as possible. If the collector circuit resistance is not zero, the following correction must be applied:

$$f_T = \frac{1}{(1/f_{TMEAS} - 2\pi C_{jC} R_{COLLECTOR})}$$

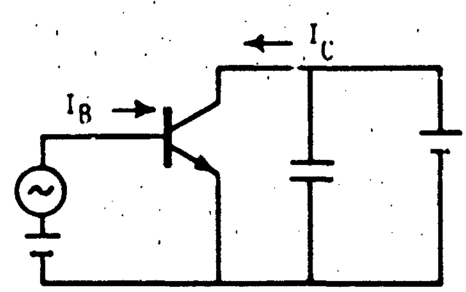


Figure III-31. Small Signal Measurement

(3) S-parameter measurement. β_o as a function of frequency can be determined from S-parameter measurements. The value of β_o at a given frequency is:

$$\left|\frac{S_{12}}{S_{21}}\right|$$

Again, f_T is given by:

$$f_T = \beta_o f_\beta$$

β_o = low frequency β

f_β = f at $\beta = \beta_o/2$

d) Example - 2N2222A

1 From Measurement

τ_F was measured using the small signal test configuration illustrated in figure III-32. Current probes were used to monitor base current and collector current. V_{CC} and the variable resistor were used to obtain the desired value of bias. The data obtained are shown in table III-6. The results are plotted in figure III-33.

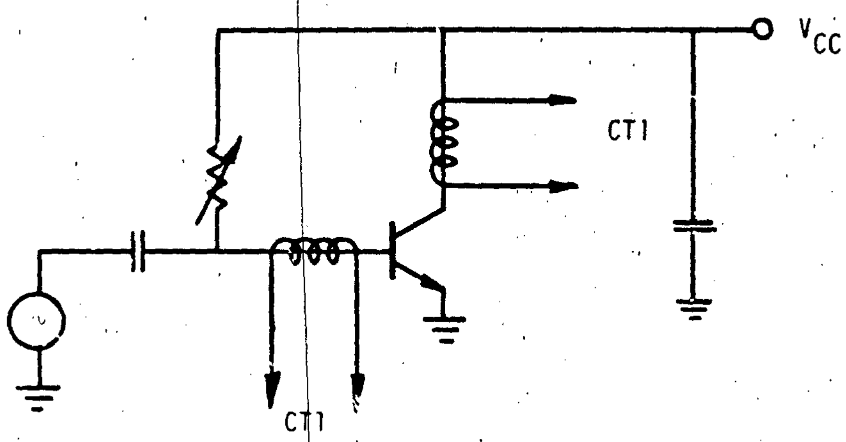


Figure III-32. Determination of τ_F

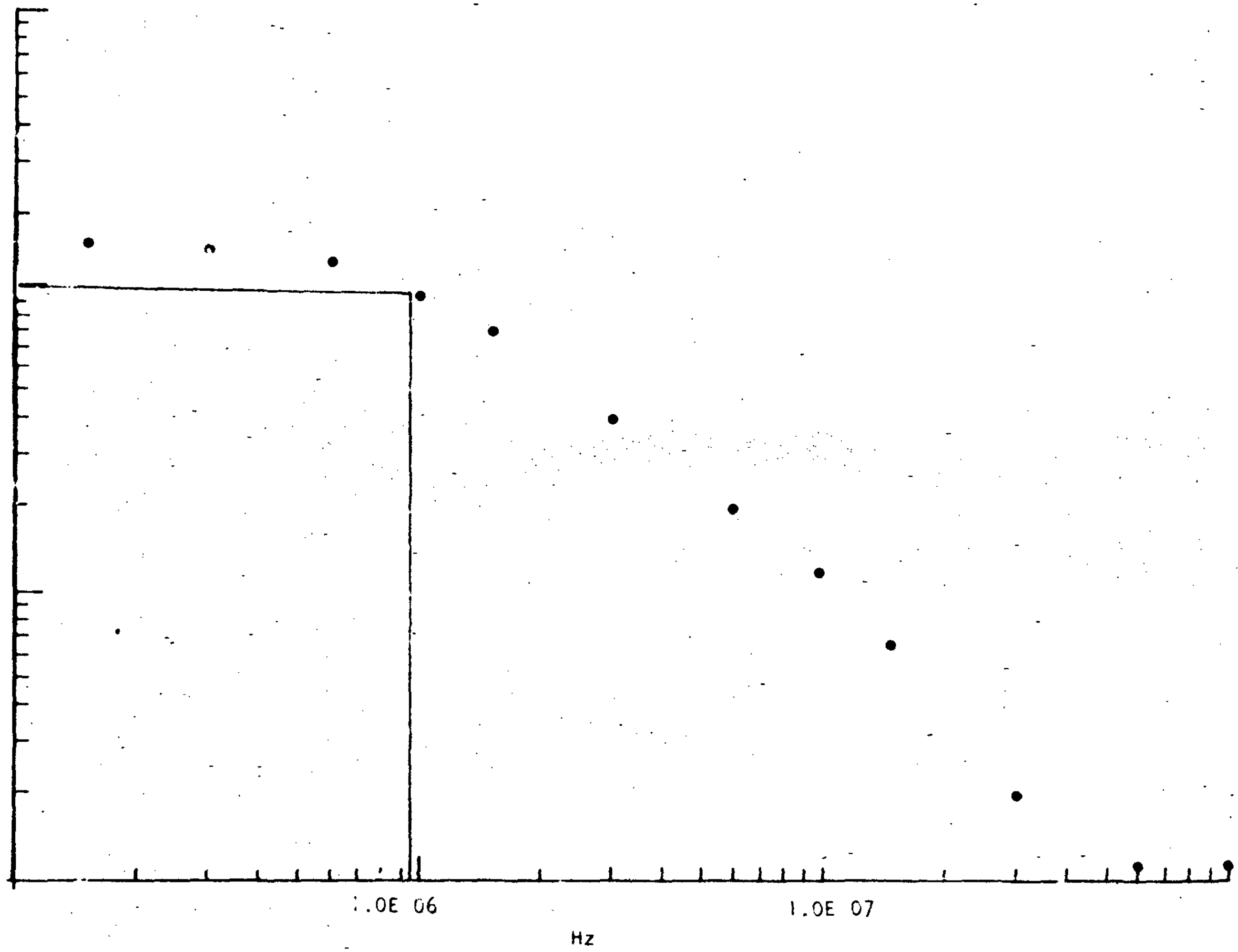


Figure III-33. Frequency Dependence of ε

TABLE III-6. MEASURED FREQUENCY RESPONSE

F	I_b	I_c	β_{ac}
100.0 kHz	0.08 mA	13.00 mA	162.50
150.0	0.10	16.00	160.00
300.0	0.10	15.20	152.00
600.0	0.10	14.00	140.00
1.0 MHz	0.10	10.40	104.00
1.5	0.10	8.00	80.00
3.0	0.10	4.00	40.00
6.0	0.10	2.00	20.00
10.0	0.10	1.20	12.00
15.0	0.08	0.54	6.75
30.0	0.09	0.18	2.00
60.0	0.12	0.14	1.17
100.0	0.12	0.14	1.17

The -3 dB frequency occurs where:

$$\beta = \frac{\beta_o}{\sqrt{2}} = \frac{163}{\sqrt{2}} = 115.26$$

This occurs at about 950 kHz.

$$f_T = (163)(950\text{ kHz}) = 155\text{ MHz}$$

$$C_{jC} \text{ at } (4\text{ V} - 0.6\text{ V}) = 5.8\text{ pF}$$

$r'_{CNORMAL} = 12.5\ \Omega$

$$\tau_F = \frac{1}{2\pi\ (155\ MHz)} - (5.8\ pF)(12.5\ \Omega)$$

$\tau_F = 9.54 \times 10^{-10}$ seconds

2 From Data Sheets

The manufacturer specification sheets (figure III-5) plot f_T versus collector current. From the f_T curves at $I_C = 10$ mA:

$r'_{CNORMAL} = 12.5\ \Omega$

C_{jC} at 20 V ≈ 4.5 pF

f_T (at V_{CB} = 20 V, I_C = 10 mA) = 230 MHz

$$\tau_F = \frac{1}{2\pi\ (230\ MHz)} - (4.5\ pF)(12.5\ \Omega)$$

$\tau_F = 6.36 \times 10^{-10}$ seconds

6) τ_R

a) Definition

τ_R is the total reverse transit time. τ_R is used to model the stored charge when the collector-base junction is forward biased. The element which models this stored charge is the diffusion capacitance C_{DC}.

b) Typical Value

A typical value of τ_R is 10 ns.

c) Measurement

If β_R is much greater than unity, τ_R may be obtained by the same method as τ_F, but with the collector and emitter

terminals interchanged. If β_R is less than unity, τ_R may be calculated from τ_{SAT}, the saturation delay time constant, as:

$$\tau_R = \tau_{SAT} \left(\frac{1 - \alpha_F \alpha_R}{\alpha_R} \right) - \left(\frac{\alpha_F}{\alpha_R} \right) \tau_F$$

τ_{SAT} in turn is determined from t_s, the transistors saturation delay time by

$$\tau_{SAT} = t_s \left\{ \ln \left[\frac{I_{BF} + I_{BR}}{(I_{CF}/\beta_F) + I_{BR}} \right] \right\}^{-1}$$

where:

I_{BF} = the forward base current
I_{BR} = the reverse base current
I_{CF} = the forward collector current

A test circuit for obtaining the necessary values is given in figure III-34.

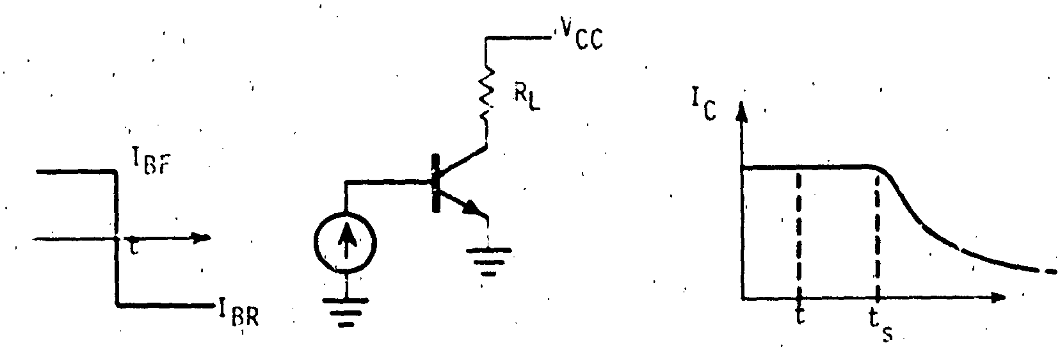


Figure III-34. Measuring Saturation Time

d) Example - 2N2222A

1 From Measurement

Since β_R is significantly greater than unity in the 2N2222A the small signal setup used to measure τ_F was also utilized to measure τ_R. The data obtained for this measurement are shown in table III-7. The results are plotted in figure III-35.

TABLE III-7. REVERSE FREQUENCY RESPONSE

I_E = 1 mA dc
V_{EC} = 4.5 V

f	I_b	I_E	β_{ac}
100.0 kHz	0.08 mA	0.51 mA	6.38
150.0	0.10	0.61	6.10
300.0	0.10	0.44	4.40
600.0	0.10	0.28	2 80
1.0 MHz	0.10	0.18	1.80
1.5	0.10	0.13	1.30
3.0	0.10	0.07	0.70

The -3 dB point is:

$$\beta = \frac{6.4}{\sqrt{2}} = 4.53$$

This corresponds to about the 300 kHz point.

$$f_T = (6\ 4)(300\ \text{kHz}) = 1.92\ \text{MHz}$$

$$\tau_R = \frac{1}{2\pi\ (1.92\ \text{MHz})} = 8.29 \times 10^{-8}\ \text{seconds}$$

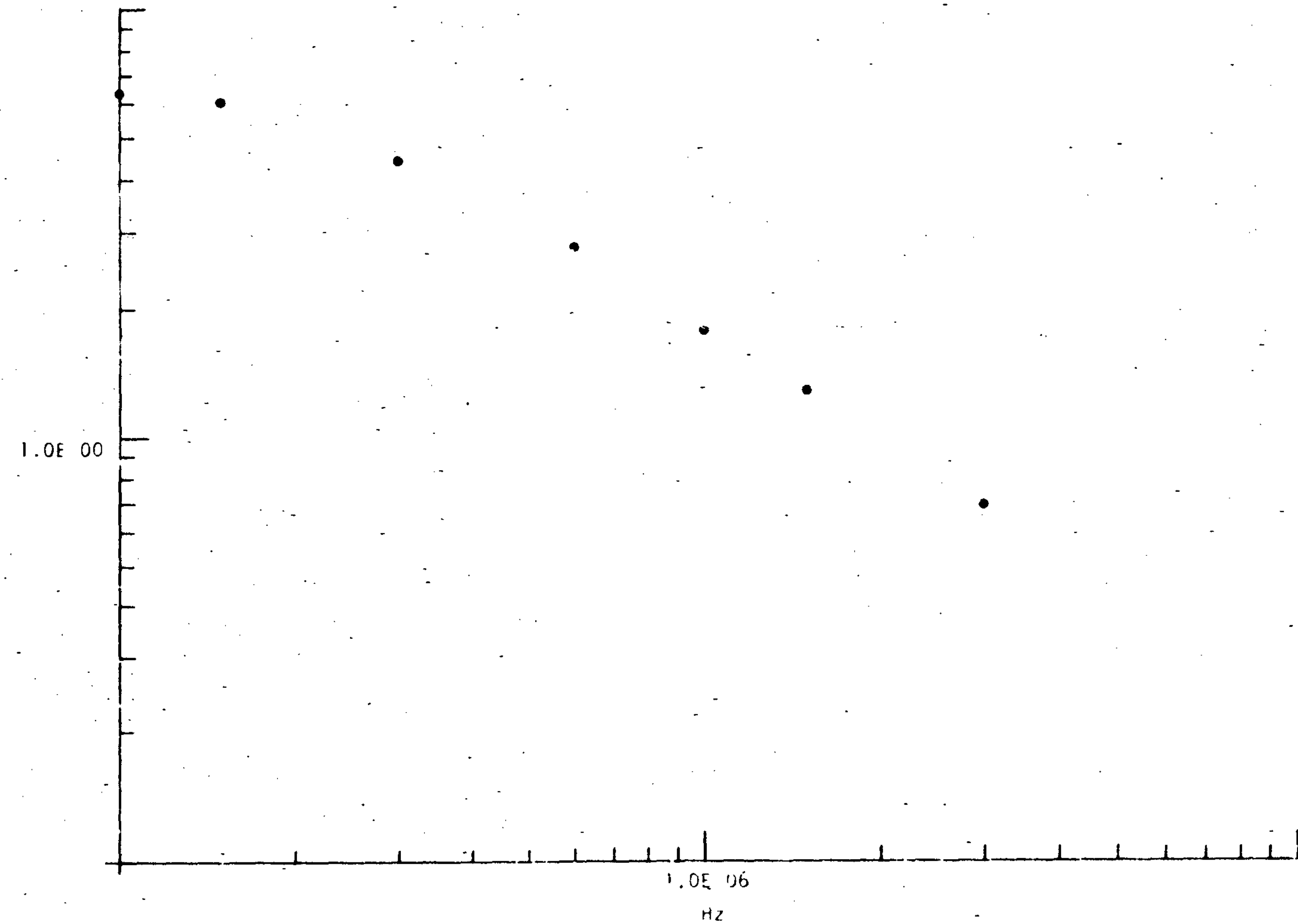


Figure III-35. Inverse β as a Function of Frequency

2 From Data Sheets

τ_R can be found from storage time information. The manufacturer specification sheets (figure III-5) give storage time data for the 2N2222A. From this data,

$$\tau_{SAT} = (225 \text{ ns}) \left\{ \ln \left[\frac{15 \text{ mA} + 15 \text{ mA}}{(150 \text{ mA}/163) + 15 \text{ mA}} \right] \right\}^{-1}$$

$$\tau_{SAT} = 3.55 \times 10^{-7} \text{ seconds}$$

$$\tau_R = (3.55 \times 10^{-7}) \left[\frac{1 - \left(\frac{163}{164}\right)\left(\frac{6.4}{7.4}\right)}{\left(\frac{6.4}{7.4}\right)} \right] - \left[\frac{\left(\frac{163}{164}\right)}{\left(\frac{6.4}{7.4}\right)} \right] 5.36 \times 10^{[illegible]}$$

$$\tau_R = 5.69 \times 10^{-8} \text{ seconds}$$

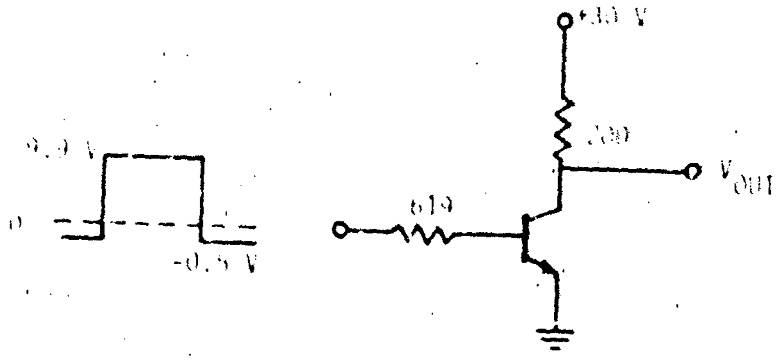
g. Computer Example

To verify the validity of the charge storage modeling portions of the general purpose transistor model, the 2N2222A model was placed in a transient test circuit described by the manufacturer specification sheets. The simulated circuit used to test the transient response of the 2N2222A transistor model is illustrated in figure III-36.

The SCEPTRE listing which simulated the transient test is given in figure III-37. Three plots resulting from this input are shown in figure III-38. These three plots represent the pulse generator voltage, collector current, and the collector voltage, respectively.

The delay time is the time required for collector current to begin to respond to the base input pulse. The predicted delay time can be seen to be about 4 ns. The specification sheets for the 2N2222A list a maximum delay time of 10 ns.

The simulated collector risetime is about 20 ns. The specification sheets allow a risetime of no more than 25 ns.



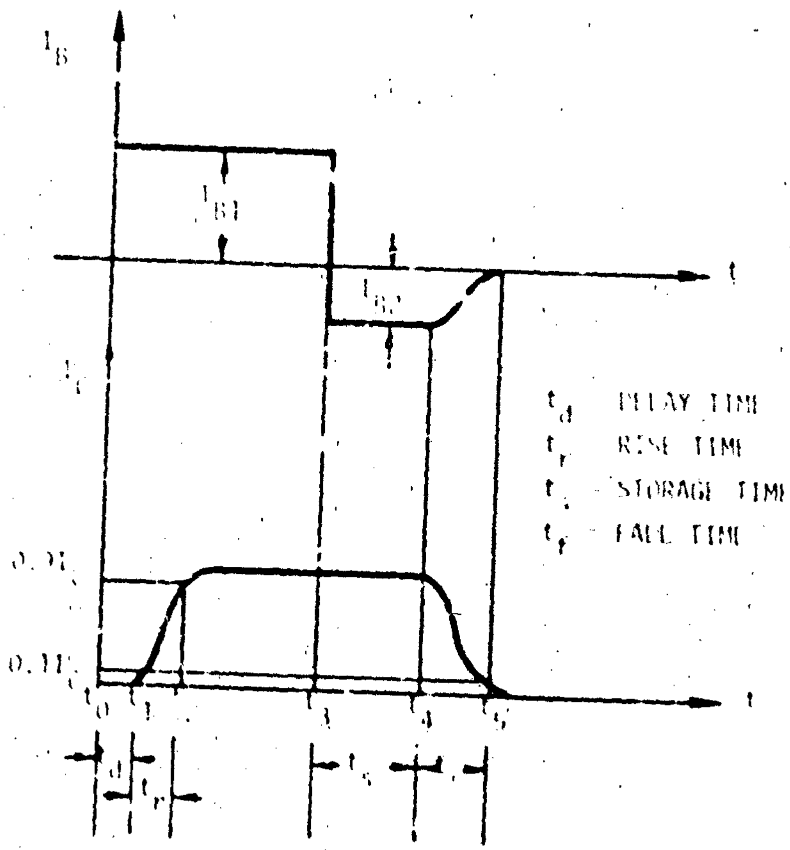


Figure III-36. Transient Analysis Circuit

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S C E P T R E   NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.3.2        6/75
02/26/76     07.53.44.

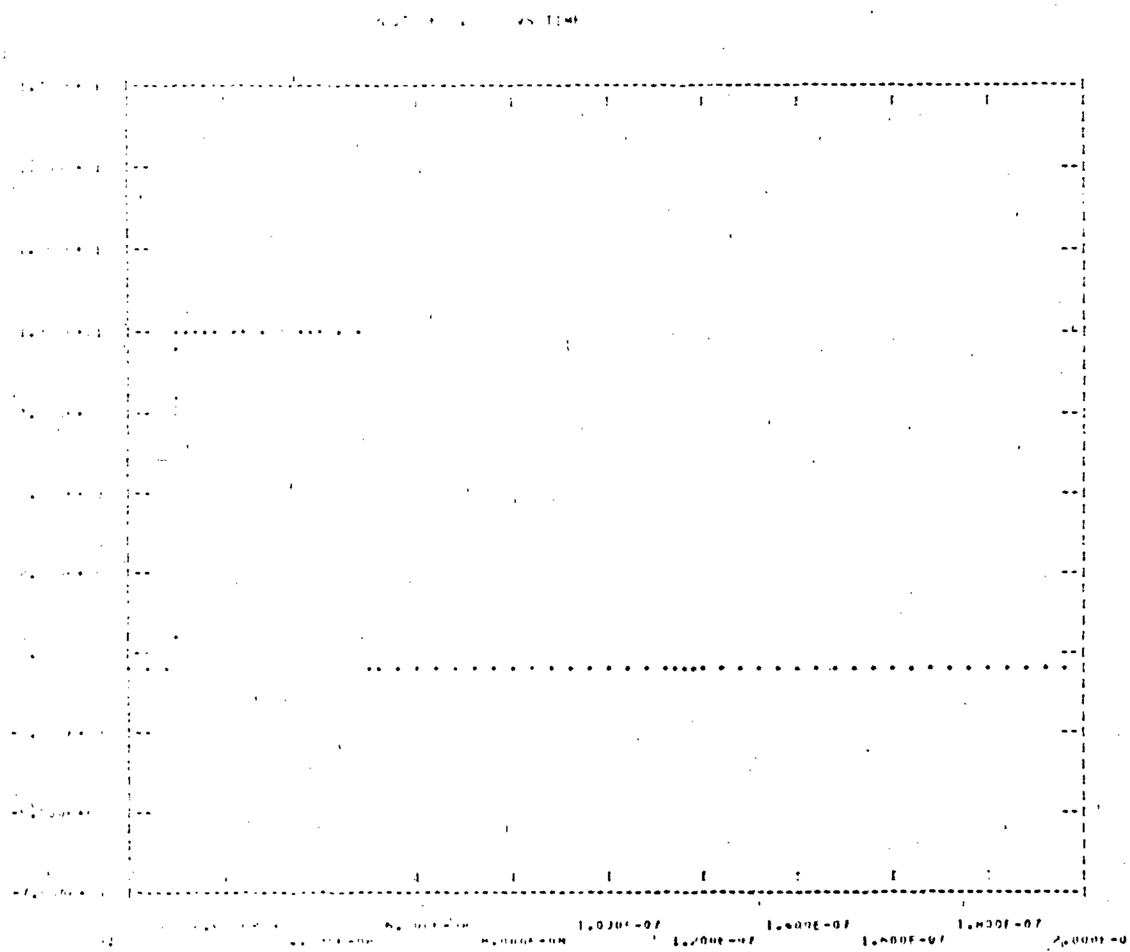

FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD "DOCUMENT" AS THE FIRST CARD
OF THE INPUT TEXT


COMPUTER TIME ENTERING SETUP PHASE=
         CPA         .259 SEC.
         PP         0.000 SEC.
         IO         0.000 SEC.


MODEL DESCRIPTION
MODEL 2N2222 (4-0-5)
ELEMENTS
JPC,1-2=Q2(JCC,VJBC,102.,4.,43)
JCC,1-2=X2(3.3E-14*(EXP(38.61*VJC)-1.))
JEC,3-2=X3(3.30E-14*(EXP(38.61*VJC)-1.))
JC,2-1=X4(JEC/20.494)
JE,2-3=X5(JCC/20.49267)
RC,5-1=15
RE,3-0=0.25
RB,4-2=100.
CC,2-1=Q1(12.36E-12,VCC,0.6,0.32,39.6,JEC,4.29E-4,3.30E-14)
CE,2-3=Q1(16.53E-12,VCE,0.6,0.3,2,38.6,JCC,9.54E-10,3.30E-14)
FUNCTIONS
Q1(A,B,C,D,E,F,G,H)=(A/(1.-AMIN1(B/C,0.94))**D+E*G*(F*H))
Q2(A,B,C,D)=(A*((1./(1.-AMIN1(.9599,ABS(B/C)**D))))-1.))
CIRCUIT DESCRIPTION
ELEMENTS
T1,3-1-4=MODEL 2N2222
E1,1-2=TABLE 1(TIME)
R1,2-3=619
RC,5-4=200
JO,4-1=0
E2,1-5=10
FUNCTIONS
TABLE 1
0.,-.5,10.E-9,-.5,10.1E-9,9.9,50.E-9,9.9,50.1E-9,-.5,90.E-9,-.5
OUTPUTS
VJO,IRCT1,E1,PLOT
RUN CONTROLS
MAXIMUM PRINT POINTS=100
RUN INITIAL CONDITIONS
STOP TIME=500.E-9
END

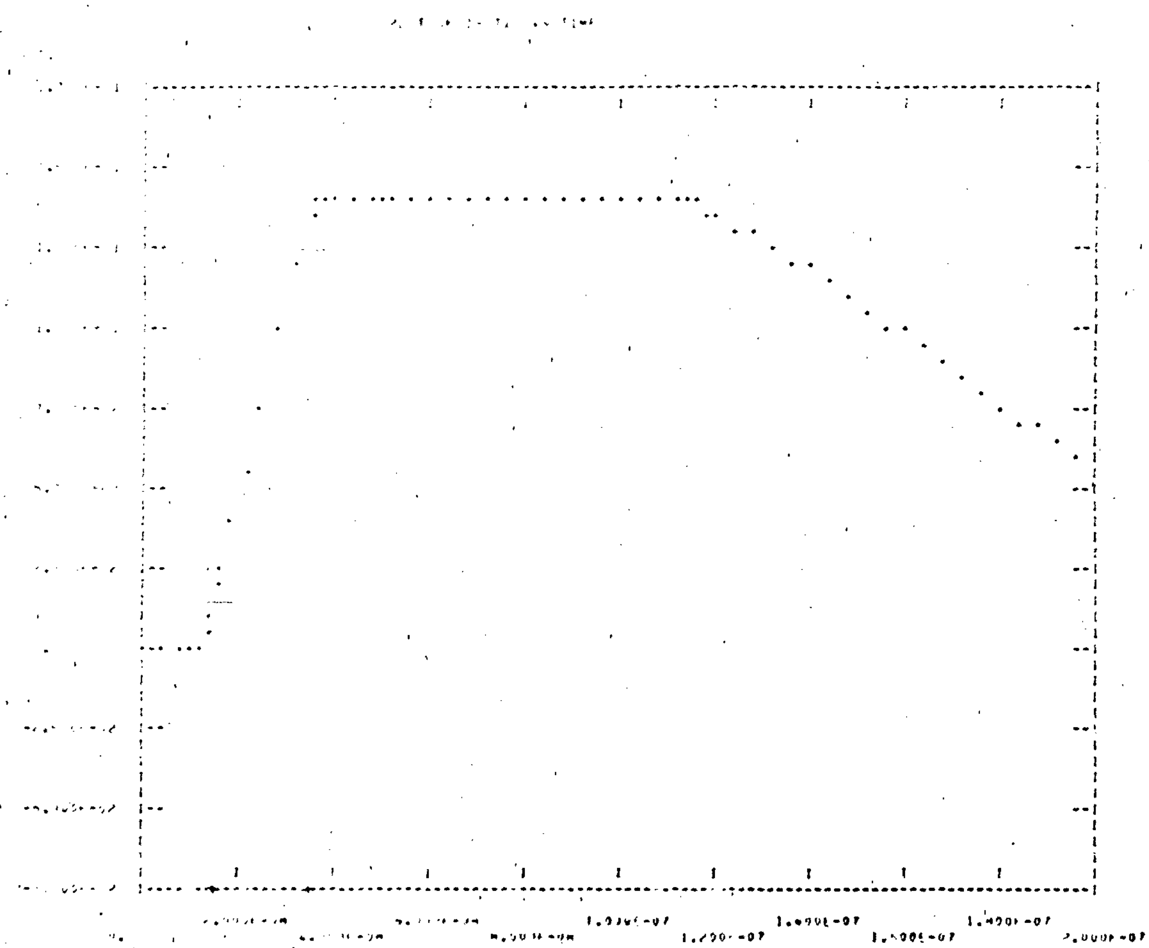

SYSTEM NOW ENTERING SIMULATION
```

Figure III-37. Transient Test Listing



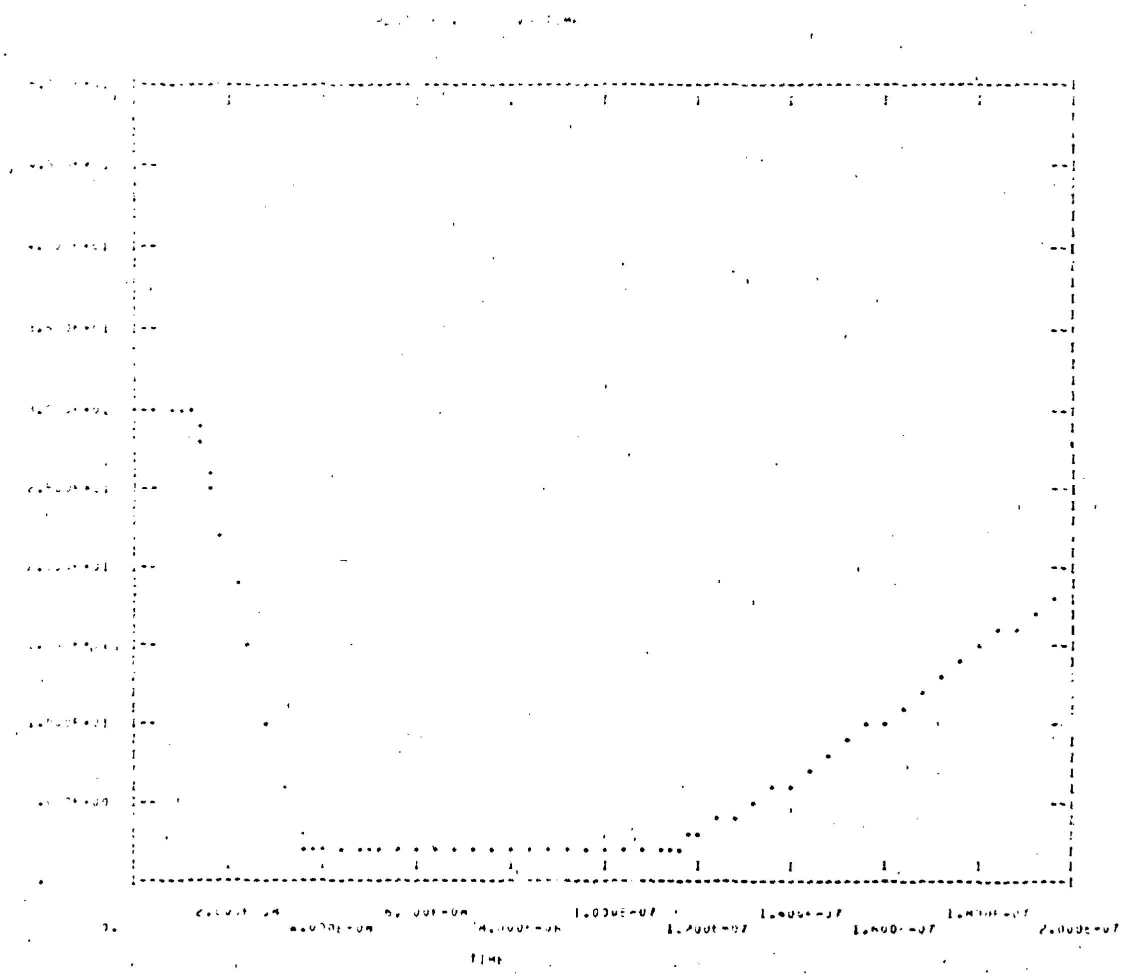
(a) Pulse Generator Voltage

Figure III-38. 2N2222A Transient Response



(b) Collector Current

Figure III-38. 2N2222A Transient Response (Continued)



(c) Collector Voltage

Figure III-38. 2N2222A Transient Response (Concluded)

The test circuit shown in figure III-36 is not the same circuit applied by the data sheets for storage and falltime; however, a comparison will be made. Storage time is the time required for the collector current to begin to turn off in response to a cutoff in base drive. The simulated storage time is about 68 ns. The maximum allowable storage time for the 2N2222A is 225 ns.

The simulated collector current falltime is about 125 ns. The falltime required in the specification sheets is less than 60 ns.

4. Modeling Variable Beta

a. Description

The most important second order effects in transistors are variations in β. The two variations considered in this section are β as a function of collector current and β as a function of collector-base voltage. These two variations may be treated together.

β variations produced by changes in collector current occur in three ranges. In region 1, low injection, β falls off with decreasing base current due to the dominance of charge recombination at low currents. In region 2, the constant β region, current gain reaches its maximum value. In region 3, the high injection region, the minority carrier concentration approaches the doping density, the net result being an increase in the conductance of the base and a falloff in β.

β variations produced by increases in the collector-base voltage are caused by the modulation of the base width. In the normal operating region, an increase in V_{BC} will increase the depletion width at this junction. The increasing depletion width cuts into the base and decreases the effective width of the base. More injected carriers succeed in crossing the smaller base, and β increases.

b. Advantages

Inclusion of variable β effects will yield greater accuracy in simulation.

c. Cautions

Addition of variable β effects are often unnecessary. The model produced is complex and difficult to parameterize. Computation time is increased.

d. Characteristics

1) Empirical Description

One method of modeling variable current gain is to describe β as an analytical function which is "fitted" to the observed gain variations. An alternate approach is to describe current gain as a function of I_C or V_{BC} through the use of piecewise linear tables.

2) Internal Model Description

Internal models of circuit analysis codes often are fixed in how β variations may be described. For example, computer programs such as SLIC and SINC use parameters called β_{FMAX}, I_{CMAX}, β_{FLOW}, I_{CLOW}, B_{CEC}, and V_{CE} to describe variable β. The significance of these parameters is illustrated in figure III-39.

The Gummel-Poon transistor model parameters which incorporate variable β are described in figure III-40.

3) Modification of Ebers-Moll Model

The Ebers-Moll model may be modified to resemble the Gummel-Poon model in its description to incorporate variable β. Two extra elements are required along with the modification of the defining equations. The modified Ebers-Moll model is shown in figure III-41.

4) Defining Equations

For the modified Ebers-Moll model:

$$I_{CL} = C_4 \, I_S \, (0) \left[\exp\left(\frac{qV_{BC}}{N_{CL}KT}\right) - 1 \right]$$

$$I_{EL} = C_2 \, I_S \, (0) \left[\exp\left(\frac{qV_{BE}}{N_{EL}KT}\right) - 1 \right]$$

$$I_{CC} \text{ (modified)} = \frac{I_S \, (0)}{\left(1 + \frac{V_{BC}}{V_A}\right)\left[1 + \theta \exp\left(\frac{qV_{BE}}{2KT}\right)\right]} \left[\exp\left(\frac{qV_{BE}}{KT}\right) - 1 \right]$$

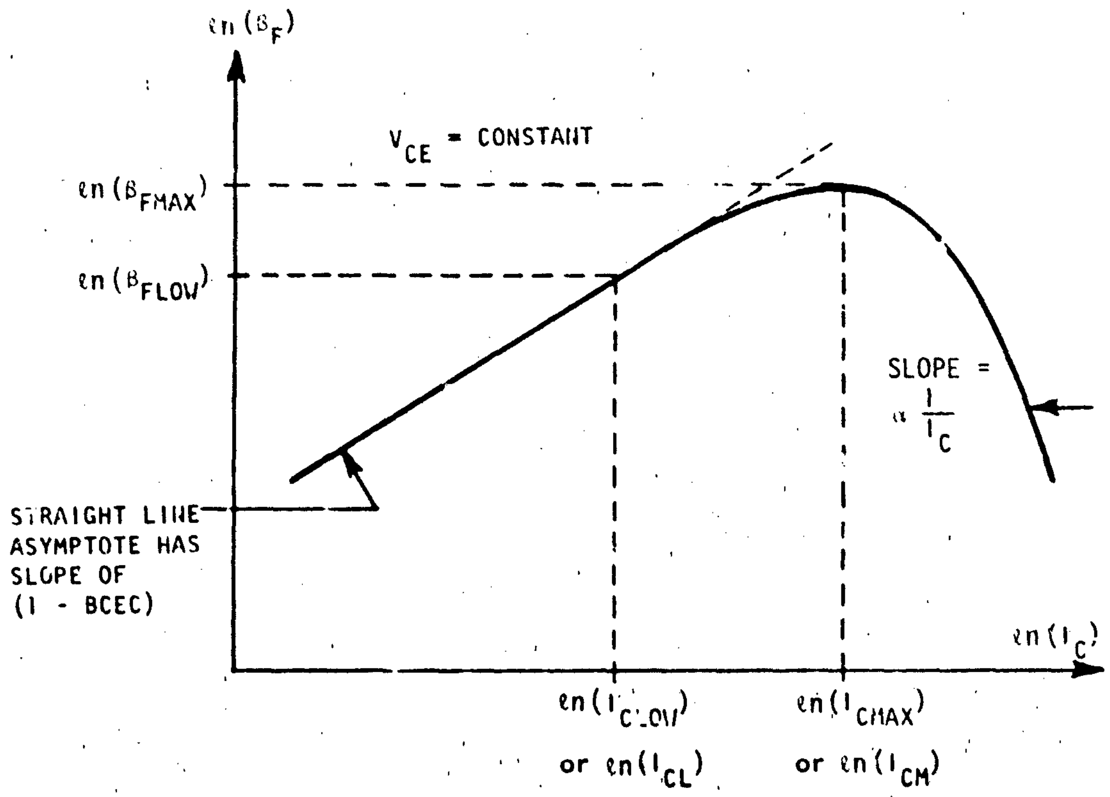


Figure III-39. Definition of β_{FMAX}, I_{CMAX}, β_{FLOW}, I_{CLOW}, B_{CEC}, AND V_{CE}

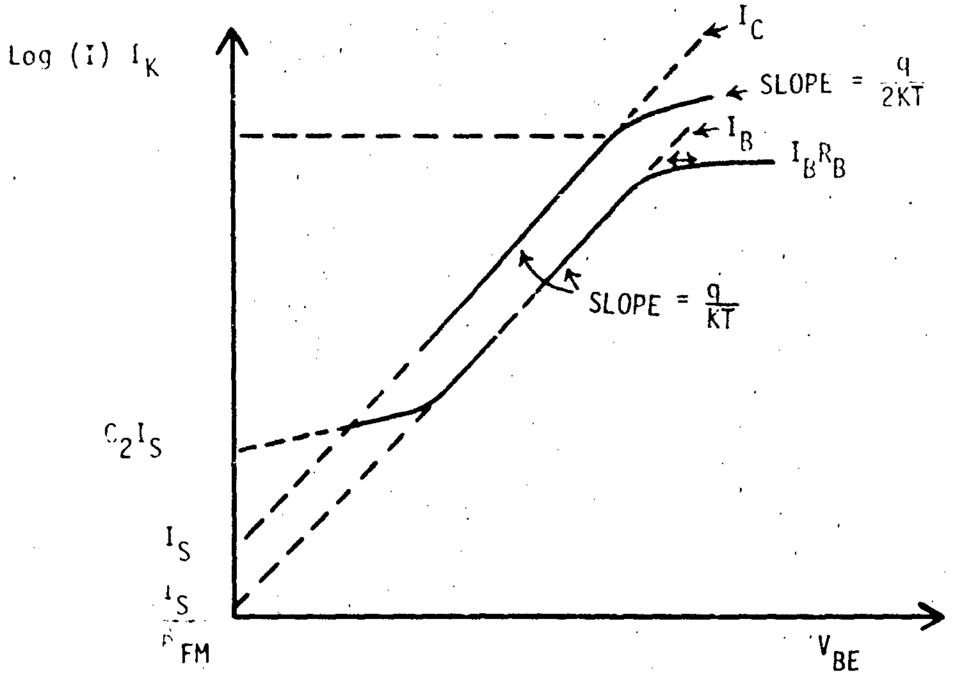


Figure III-40. Gummel-Poon Model Description

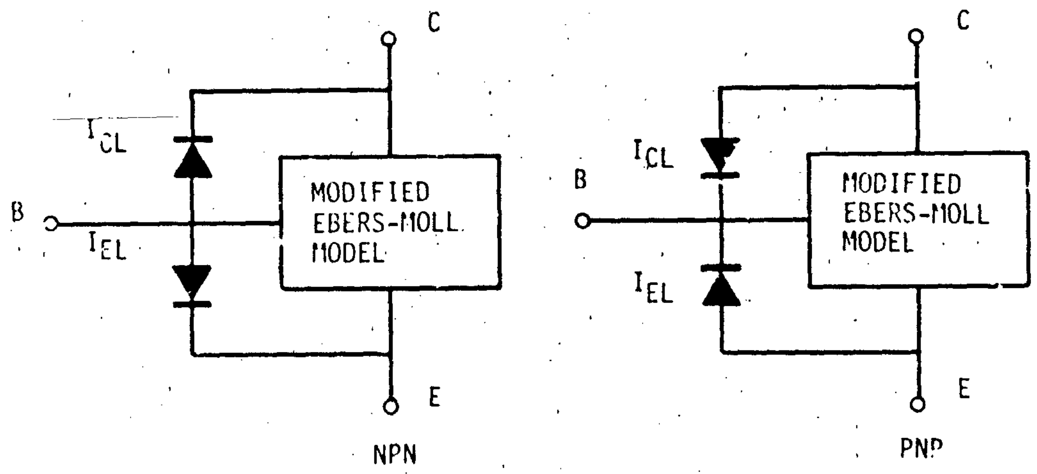


Figure III-41. Inclusion of Variable β in the Ebers-Moll Model

For the Gummel-Poon model:

$$I_{CC}\ (\text{modified}) = \frac{I_S(0)}{Q_B}\left[\exp\left(\frac{qV_{BE}}{KT}\right)-1\right]$$

$$I_B = \frac{I_S(0)}{\beta_F}\left[\exp\left(\frac{qV_{BE}}{KT}\right)-1\right] + C_2 I_S(0)\left[\exp\left(\frac{qV_{BE}}{N_{EL}KT}\right)-1\right]$$

$$Q_B = \frac{1}{2}\left(Q1 + \sqrt{Q1^2 + 4Q_2}\right)$$

$$Q_1 = 1 + \frac{V_{BC}}{V_A} + \frac{V_{BE}}{V_B}$$

$$Q_2 = B\,\frac{I_S(0)}{I_K}\left[\exp\left(\frac{qV_{BE}}{KT}\right)-1\right] + \frac{I_S(0)}{I_{KR}}\left[\exp\left(\frac{qV_{BC}}{KT}\right)-1\right]$$

where B is the base push-out factor (see reference III-2). B may be approximated by unity.

The empirical analytic expressions applied in NET-2 to model variable current gain are:

$$\beta_F = B_f\left(A_1 + A_2V_{BE} + A_3V_{BE}^2 + A_4V_{BE}^3\right)$$

$$\beta_I = B_i\left(B_1 + B_2V_{CB} + B_3V_{CB}^2 + B_4V_{CB}^3\right)$$

e. Parameterization C_2, N_{EL}, θ

1) Definition

C_2, N_{EL}, and θ define the variation of β_F with I_C. They are defined in terms of plots of $\ln(I_C, I_B)$ versus $V_{B'E'}$ for $V_{B'C'} = 0$. This plot is illustrated in figure III-42. C_2 and N_{EL} describe the low injection component of I_B which describes the falloff in β_F for low currents. The parameter θ models the falloff in β due to high injection.

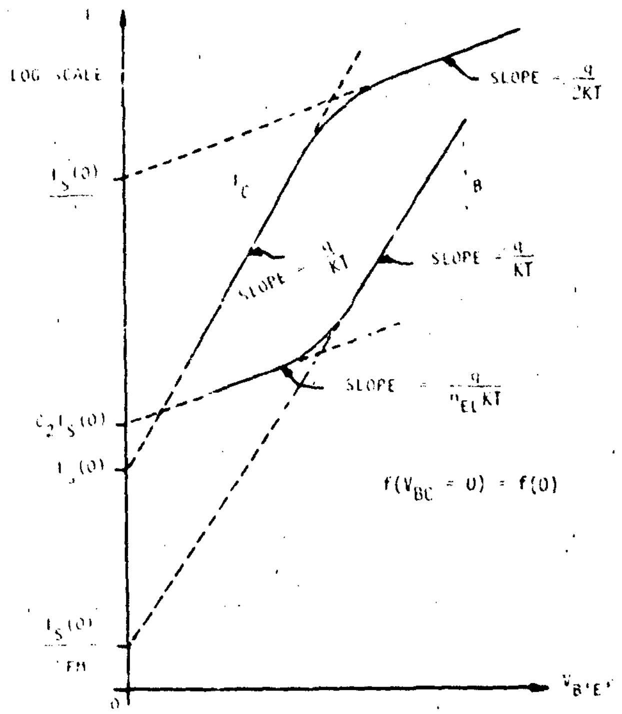


Figure III-42. Example Data Plot

2) <u>Typical Values</u>

Typical values for C_2, N_{EL}, and θ are 1000, 2, and 10^{-6}, respectively.

3) <u>Measurement</u>

I_C and I_B must be measured over a wide range of V_{BE} values. The data are then graphed on a semilog plot. This plot must now be corrected for the voltage drops across r_e' and r_b'. To accomplish this, first identify the ideal line segment for base current. Extrapolate this line out to the high current and voltage region. Assume that any deviation from the ideal base current line is due to $(I_B r_b' + I_E r_e')$. Subtract this voltage from the I_C line. This process is illustrated in figure III-43.

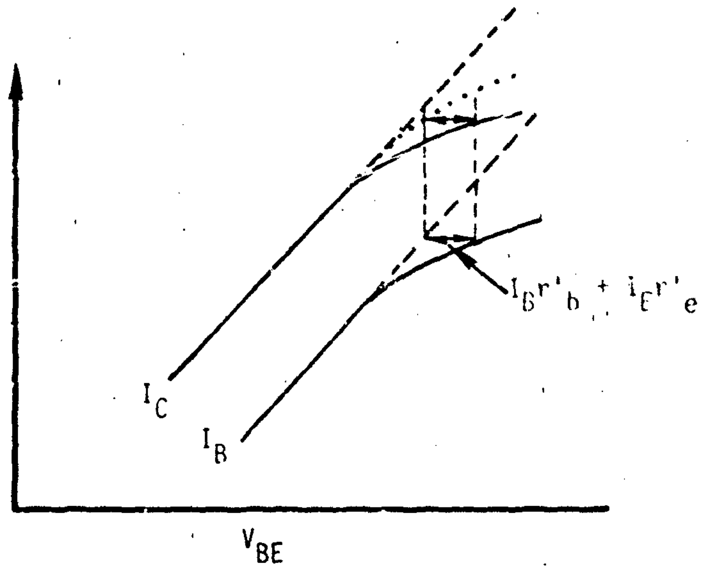


Figure III-43. Voltage Corrections

If the corrected I_C lies to the left of the ideal I_C curve, back correct the corrected I_C line by the amount ΔVm, where ΔVm is the maximum voltage deviation to the left of the ideal I_C line. This "over correction" may be caused by current crowding effects. Extrapolation of the various asymptotes to the $V_{BE} = 0$ V axis will yield C_2, N_{EL}, θ, and I_S as illustrated by figure III-42.

4) Examples - 2N2222A*

a) From Measurement

C_2, N_{EL}, and θ were determined using the test configuration of figure III-44. In this figure, V represents a high input impedance voltmeter and I represents a current meter. Data obtained using the configuration are shown in table III-8.

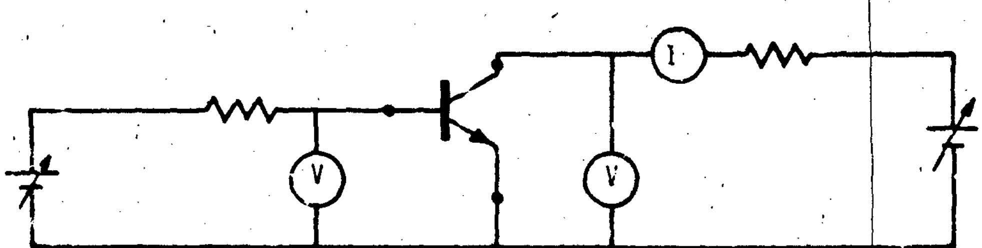


Figure III-44. Test Configuration

TABLE III-8. MEASURED β VARIATIONS

FORWARD ACTIVE REGION

$V_{BE} = V_{CE}$	I_B	I_C
0.562 V	1 μA	0.055 mA
0.582	2	0.135
0.594	3	0.222
0.615	6	0.519
0.629	10	0.942
0.649	20	2.000
0.661	30	3.200
0.681	60	7.200
0.683	100	12.000
0.706	200	24.200
0.718	300	39.500
0.734	600	85.000
0.744	1 mA	130.000
0.767	2	192.000
0.787	3	240.000
0.820	6	370.000

*NOTE: Due to the failure of the device which was used in earlier examples, a new device was chosen yielding a composite model for the remaining sections.

The plotted data with the necessary corrections are shown in figure III-45. The following steps were devised to identify the straight line segments.

Lines of slope q/KT were fit to the I_C and I_B data. At the point where high current β falloff was observed, a line of slope q/2KT was constructed.

$I_S(0)$ can be seen to be 3 x 10^{-14} amperes.

$$\frac{I_S(0)}{\theta} = 6 \times 10^{-8}$$

$$\theta = \frac{3 \times 10^{-14}}{6 \times 10^{-8}} = 5 \times 10^{-7}$$

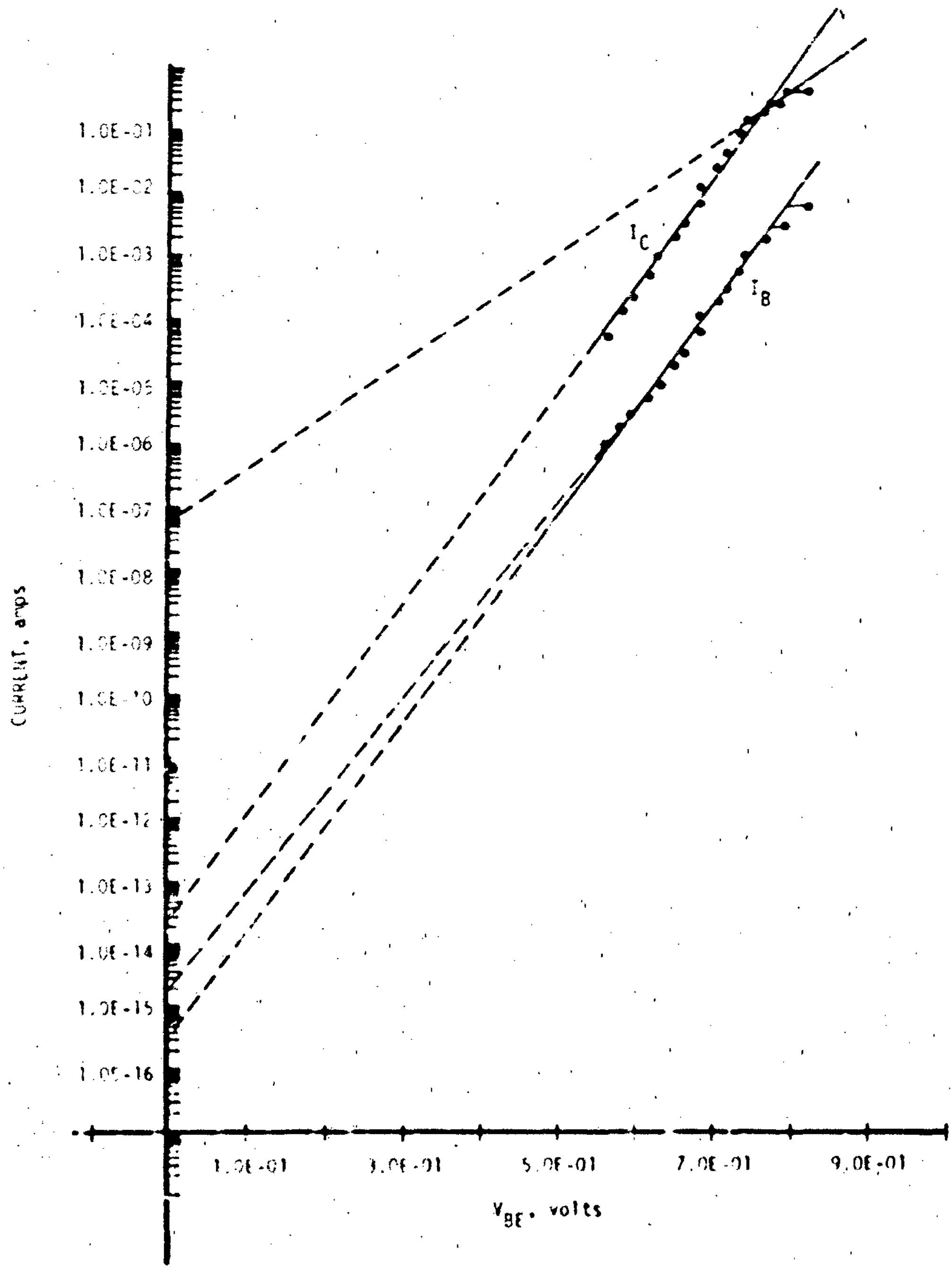


Figure III-45 I_C and I_B as a Function of V_{BE}

The low I_B asymptote is not clearly visible. However, an asymptote was constructed for illustrative purposes.

$$C_2 I_S = 2 \times 10^{-15}$$

$$C_2 = \frac{2 \times 10^{-15}}{3 \times 10^{-14}} = 6.67 \times 10^{-2}$$

$$\text{Slope} = \frac{q}{N_{EL}\ KT} = \frac{(\ln 3\ \mu A - \ln 2 \times 10^{-15}\ A)}{(0.594\ V - 0\ V)}$$

$$= 35.57$$

$$N_{EL} = \frac{1}{(0.0259)(35.57)} = 1.085$$

$$\frac{I_S(0)}{\beta_{FM}} = 3 \times 10^{-16}$$

$$\beta_{FM} = \frac{3 \times 10^{-14}}{3 \times 10^{-16}} = 100$$

b) From Data Sheets

Manufacturer device specification sheets often give β versus I_C data. These data may be used directly for models which describe β as a function of I_C, or β_{FM}, C_2, N_{EL}, and θ may be extracted from this information. The β versus I_C data for the 2N2222A transistor are included in figure III-5.

5) C_4, N_{CL}, θ_R

a) Definition

These three parameters define the variation of β_R with I_E and are analogous to β_{FM}, C_2, N_{EL}, and θ, respectively, with V_{BE} replaced by V_{BC}, I_C replaced by I_E, V_{BC} replaced by V_{BE}, and β_F replaced by β_R.

b) Typical Values

Typical values of C_4, N_{CL}, and θ_R are 1, 2, and 1×10^{-6}, respectively.

c) Measurement

The β_R versus I_E parameters are obtained by the same method used with the β_F versus I_C parameters, except the emitter and collector terminals are interchanged.

d) Example - 2N2222A

C_4, N_{CL}, and θ_R were determined with the same test configuration as figure III-44, but with the collector and emitter leads of the transistor interchanged. The data obtained are shown in table III-9. The plotted data are shown in figure III-46.

TABLE III-9. MEASURED INVERSE α VARIATIONS

INVERSE ACTIVE REGION

$V_{BC} = V_{EC}$	I_R	I_E
0.555 V	0.01 mA	0.050 mA
0.576	0.02	0.120
0.588	0.03	0.200
0.610	0.06	0.455
0.626	0.10	0.840
0.647	0.20	1.800
0.662	0.30	2.950
0.679	0.60	6.220
0.695	1.00	10.000
0.718	2.00	18.200
0.726	3.00	26.200
0.747	6.00	50.000
0.762	10.00	72.400
0.790	30.00	140.000

$I_S(0) = 3 \times 10^{-14}$ amperes

$$\frac{I_S(0)}{\theta_R} = 2 \times 10^{-8}$$

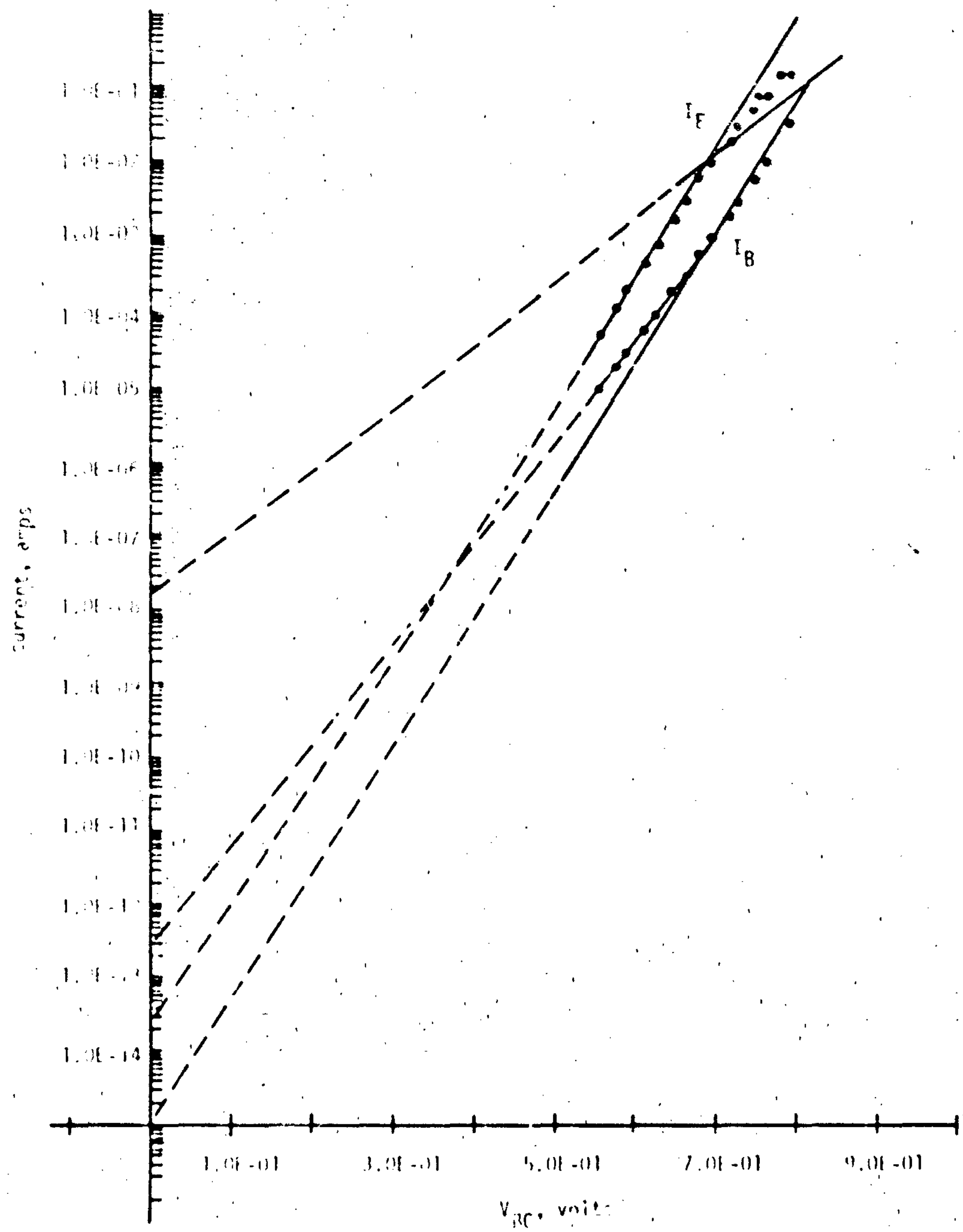


Figure III-46. I_E and I_B as a Function of V_{BC} in the Inverse Mode

$$\beta_R = 1.5 \times 10^{-6}$$

$$C_4 \; I_S \; (0) = 2 \times 10^{-13}$$

$$C_4 = 6.67$$

$$\text{Slope} = \frac{q}{N_{CL}\;KT} = \frac{(\ln 0.6 \text{ mA} - \ln 2 \times 10^{-13} \text{ A})}{(0.679 \text{ V} - 0 \text{ V})}$$

$$= 32.1$$

$$N_{CL} = \frac{1}{(32.1)(0.0259)} = 1.2$$

$$\frac{I_S \; (0)}{\beta_{RM}} = 1 \times 10^{-15}$$

$$\beta_{RM} = 30$$

6) V_A, V_B

a) Definition

V_A and V_B are the Early voltage and the inverse Early voltage, respectively. The definition of the Early voltage is illustrated by figure III-47.

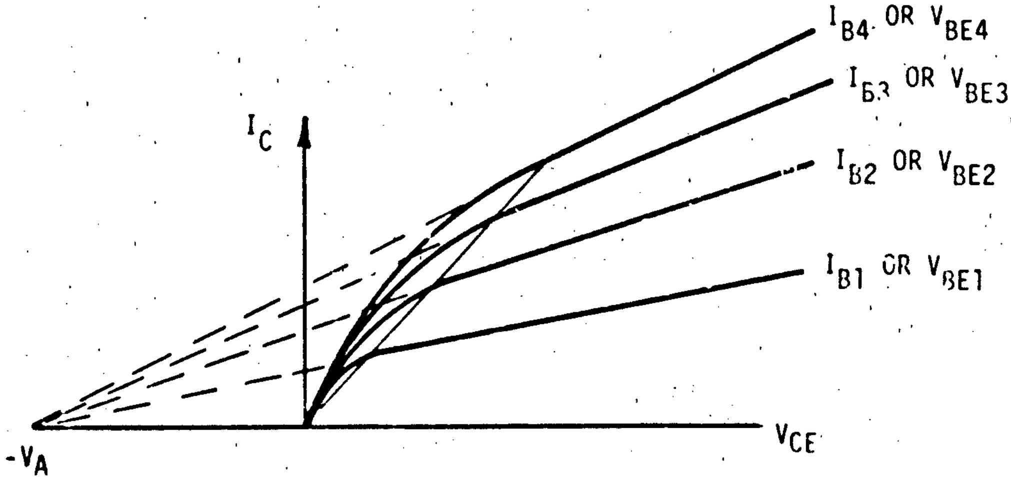


Figure III-47. Definition of Early Voltage

b) Typical Values

A typical value of V_A is 100 volts. A typical value of V_B is 10 volts.

c) Measurement

The slope of I_C as a function of V_{CE} for a constant V_{BE} at $V_{CE} = V_{BE}$ is defined as g_{0A}. The definition of g_{0A} is illustrated in figure III-48. The corresponding slope in the inverse region is defined as g_{0B} as illustrated in figure III-49.

g_{0A} and g_{0B} are given as:

$$g_{0A} = \frac{I_C\ (0)}{V_A\ (1 + V_{BE}/V_B)}$$

$$g_{0B} = \frac{I_E\ (0)}{V_B\ (1 + V_{BC}/V_A)}$$

V_A and V_B can now be solved for as follows:

$$V_A = \frac{I_C\ (0)\ I_E\ (0) - g_{0A}\ g_{0B}\ V_{BE}\ V_{BC}}{g_{0A}\ I_C\ (0) + g_{0A}\ g_{0B}\ V_{BE}}$$

$$V_B = \frac{I_C\ (0)\ I_E\ (0) - g_{0A}\ g_{0B}\ V_{BE}\ V_{BC}}{g_{0B}\ I_E\ (0) + g_{0A}\ g_{0B}\ V_{BC}}$$

If only V_A is desired, the approximation

$$V_A = \frac{I_C\ (0)}{g_{0A}}$$

may be used.

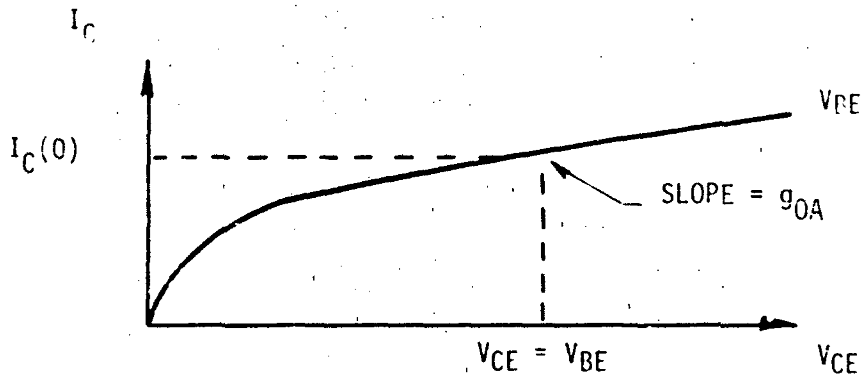


Figure III-48. Definition of g_{OA}

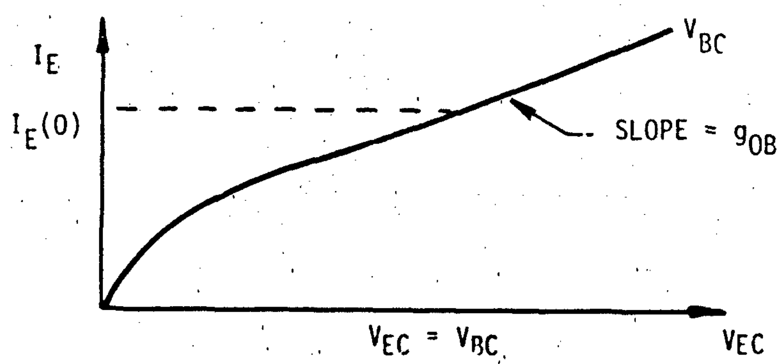


Figure III-49. Definition of g_{OB}

d) Example - 2N2222A

g_{0A} can be obtained from figure III-50. The top trace represents a V_{BE} of 535 mV. I_C (0) at $V_{BE} = V_{CE}$ is 37.5 μA.

$$g_{0A} = \frac{40\ \mu A - 37.5\ \mu A}{10\ V - 0.535\ V} = 2.64 \times 10^{-7} \text{ siemens}$$

The first approximation to V_A is:

$$V_A = \frac{37.5\ \mu A}{2.64 \times 10^{-7} \text{ siemens}} = 142 \text{ volts}$$

The inverse parameters can be determined from figure III-51. At $V_{BC} = V_{EC} = 0.6$ V, $I_E(0) = 0.32$ mA,

$$g_{0B} = \frac{(3.4 \times 10^{-4}\ A - 3 \times 10^{-4}\ A)}{(1.0\ V - 0.2\ V)} = 5 \times 10^{-5} \text{ siemens}$$

It should be noted that V_B cannot be calculated by the same approximation used to calculate V_A because the approximate method of determining V_A assumed a negligible effect from the emitter-base space charge layer. This assumption is not valid when determining V_B.

$$V_A = \frac{(37.5\ \mu A)(0.32\ mA) - (2.64 \times 10^{-7})(5 \times 10^{-5})(0.535\ V)(0.6\ V)}{(2.64 \times 10^{-7})(0.32\ mA) + (2.64 \times 10^{-7})(5 \times 10^{-5})(0.535\ V)}$$

V_A = 131 volts

$$V_B = \frac{(37.5\ \mu A)(0.32\ mA) - (2.64 \times 10^{-7})(5 \times 10^{-5})(0.535\ V)(0.6\ V)}{(5 \times 10^{-5})(37.5\ \mu A) + (2.64 \times 10^{-7})(5 \times 10^{-5})(0.6\ V)}$$

V_B = 6.38 volts

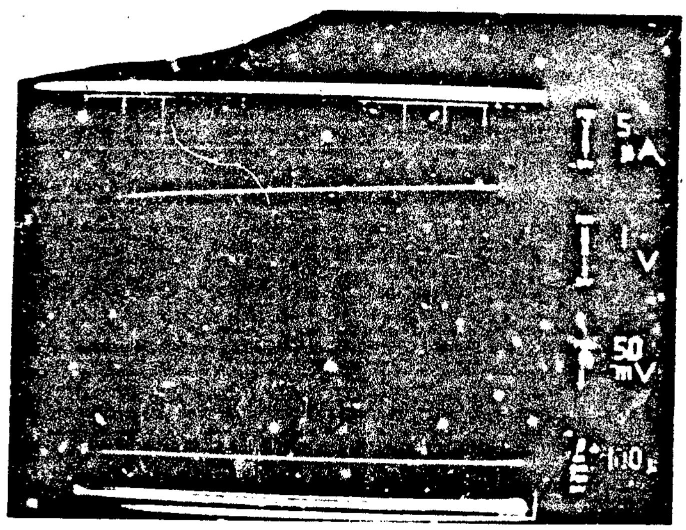


Figure III-50. 2N2222A I_C Versus V_{CE}

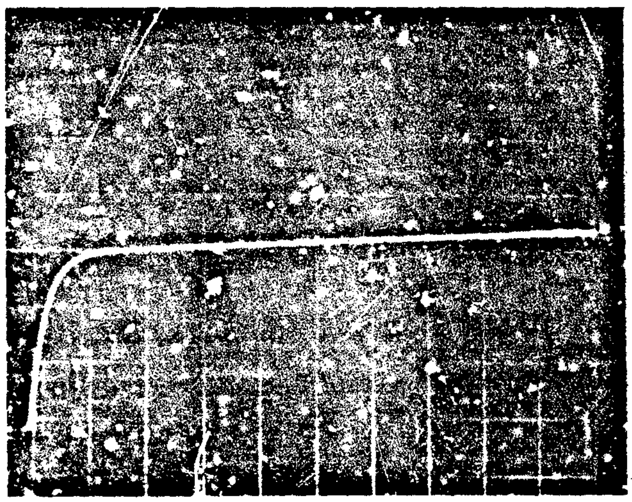


Figure III-51. Determination of Inverse Early Voltage.

f. Computer Example

To verify the modified Ebers-Moll model, it was attempted to recover the I_C, I_B, and V_{BE} data from the transistor model. The circuit simulation of figure III-52 was applied.

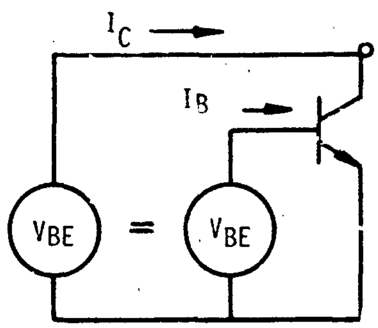


Figure III-52. Test Simulation

One difficulty encountered was the problem of r_b', r_e', and r_c'. These resistors were defined for an earlier transistor and now form the ohmic impedance of a composite model. To avoid this difficulty, r_c', r_e', and r_c' were made very small, and the data were compared to the corrected raw data.

The transistor model implemented contained only the dc portion of the model as shown by the listing in figure III-53. The data produced by the model and the experimental data are plotted together in figure III-54.

To demonstrate the Early voltage inclusion in a model, the Gummel-Poon model was put through a curve tracer simulation circuit. To obtain the curve tracer, the circuit of figure III-55 was simulated using the SPICE code.

Figure III-56 is the SPICE listing for this simulation. Figure III-57 is the transistor characteristic of the composite 2N2222A model.

5. Modeling Other Second Order Effects

a. Description

Other second order effects which may be important considerations are:

```
S C E P T R E    NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2       5/76
 03/01/78     13.12.53.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD  "DOCUMENT"  AS THE FIRST CARD
OF THE INPUT TEXT

COMPUTER TIME ENTERING SETUP PHASE-
          CPA         .083 SEC.
          PP         0.000 SEC.
          IO         0.000 SEC.

CIRCUIT DESCRIPTION
ELEMENTS
JCC,1-2=X1(3.E-14*(EXP(38.61*VJE)-1.)*P1/P2)
JCL,2-1=X2(2.E-13*(EXP(VJC*32.1)-1.))
JEL,2-3=X8(2.E-15*(EXP(VJE*35.57)-1.))
JEC,3-2=X3(3.E-14*(EXP(38.61*VJC)-1.))
JC,2-1=X4(JEC/0.9677)
JE,2-3=X5(JCC/0.9901)
RC,5-1=0.01
RE,3-0=0.01
RB,4-2=0.01
CC,2-1=1.E-12
CE,2-3=1.E-12
EB,0-4=TABLE 2(TIME)
ECC,0-5=X9(EB)
DEFINED PARAMETERS
P1=X6(1.-VJC/142.)
P2=X7(1.+5.E-7*(EXP(VJE*19.31)))
FUNCTIONS
TABLE 2
0,0,1,1
OUTPUTS
EB,IRC,IRB
RUN CONTROLS
STOP TIME=1
MINIMUM STEP SIZE=1.E-39
MAXIMUM PRINT POINTS=500
END


SYSTEM NOW ENTERING SIMULATION




COMPUTER TIME AT TERMINATION OF SETUP PHASE-
          CPA         .347 SEC.
          PP         0.000 SEC.
          IO         0.000 SEC.
```

Figure III-53. Listing for Variable β Test

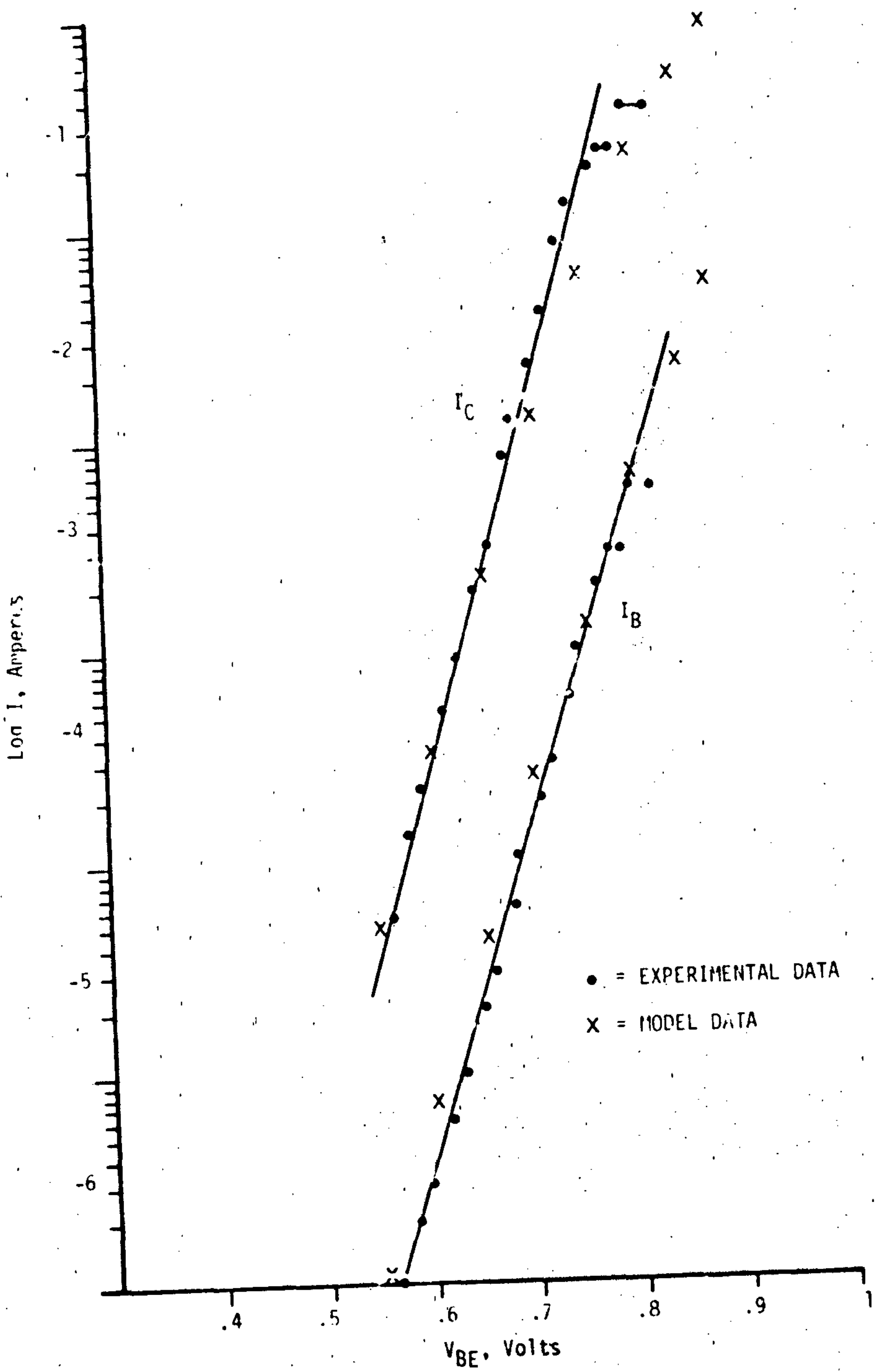


Figure III-54. Model Results

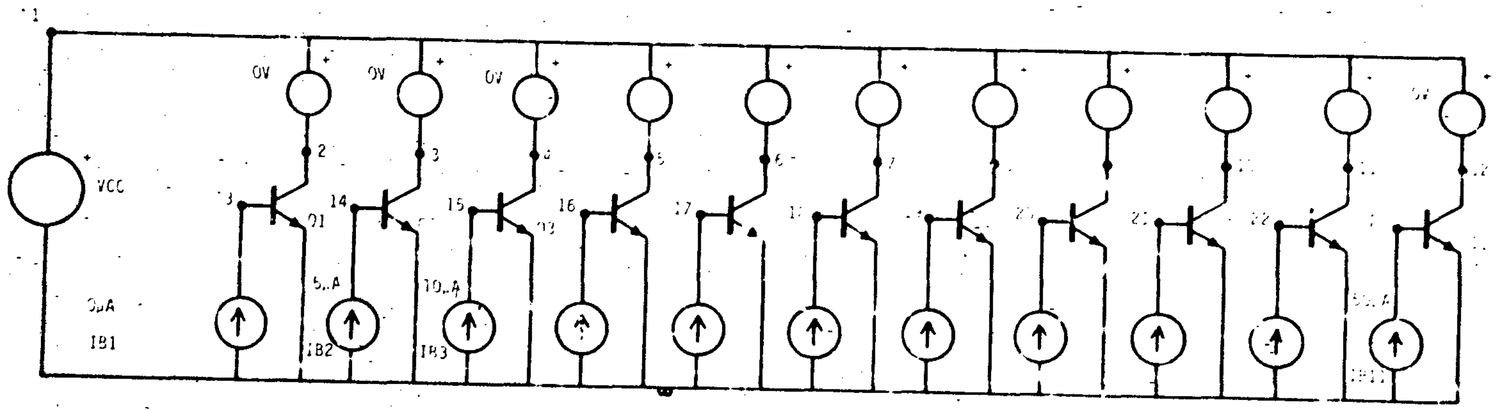


Figure III-55. SPICE Test Circuit

```
***** 03/01/78 ******** SPICE 20.2 (26SEP75) ******** 14.30.39.*****

*GUMMEL-POON TRANSISTOR MODEL

     INPUT LISTING                         TEMPERATURE =   27.000 DEG C

*****************************************************************************

VCC 1 0 0
V1 1 2 0
V2 1 3 0
V3 1 4 0
V4 1 5 0
V5 1 6 0
V6 1 7 0
V7 1 8 0
V8 1 9 0
V9 1 10 0
V10 1 11 0
V11 1 12 0
IB1 0 13 0
IB2 0 14 5.E-6
IB3 0 15 1.E-5
IB4 0 16 1.5E-5
IB5 0 17 2.0E-5
IB6 0 18 2.5E-5
IB7 0 19 3.0E-5
IB8 0 20 3.5E-5
IB9 0 21 4.0E-5
IB10 0 22 4.5E-5
IB11 0 23 5.0E-5
Q1 2 13 0 Q0
Q2 3 14 0 Q0
Q3 4 15 0 Q0
Q4 5 16 0 Q0
Q5 6 17 0 Q0
Q6 7 18 0 Q0
Q7 8 19 0 Q0
Q8 9 20 0 Q0
Q9 10 21 0 Q0
Q10 11 22 0 Q0
Q11 12 23 0 Q0
.MODEL Q0 NPN(BF=100 BR=30 IS=3.E-14 RB=100 RC=1[illegible]
+       C2=6.67E-2 NE=1.035 IK=192.E-3 IKR=[illegible]
+               TF=9.55E-10 TR=8.29E-9 CJE=23.1[illegible]
+               CJC=12.36E-12 PC=0.6 MC=0.32 EG=1.11)
.DC VCC 0 50 1.
.PLOT DC I(V1) I(V2) I(V3) I(V4) I(V5) I(V6) I(V7) [illegible]
.END
```

Figure III-56. SPICE Input

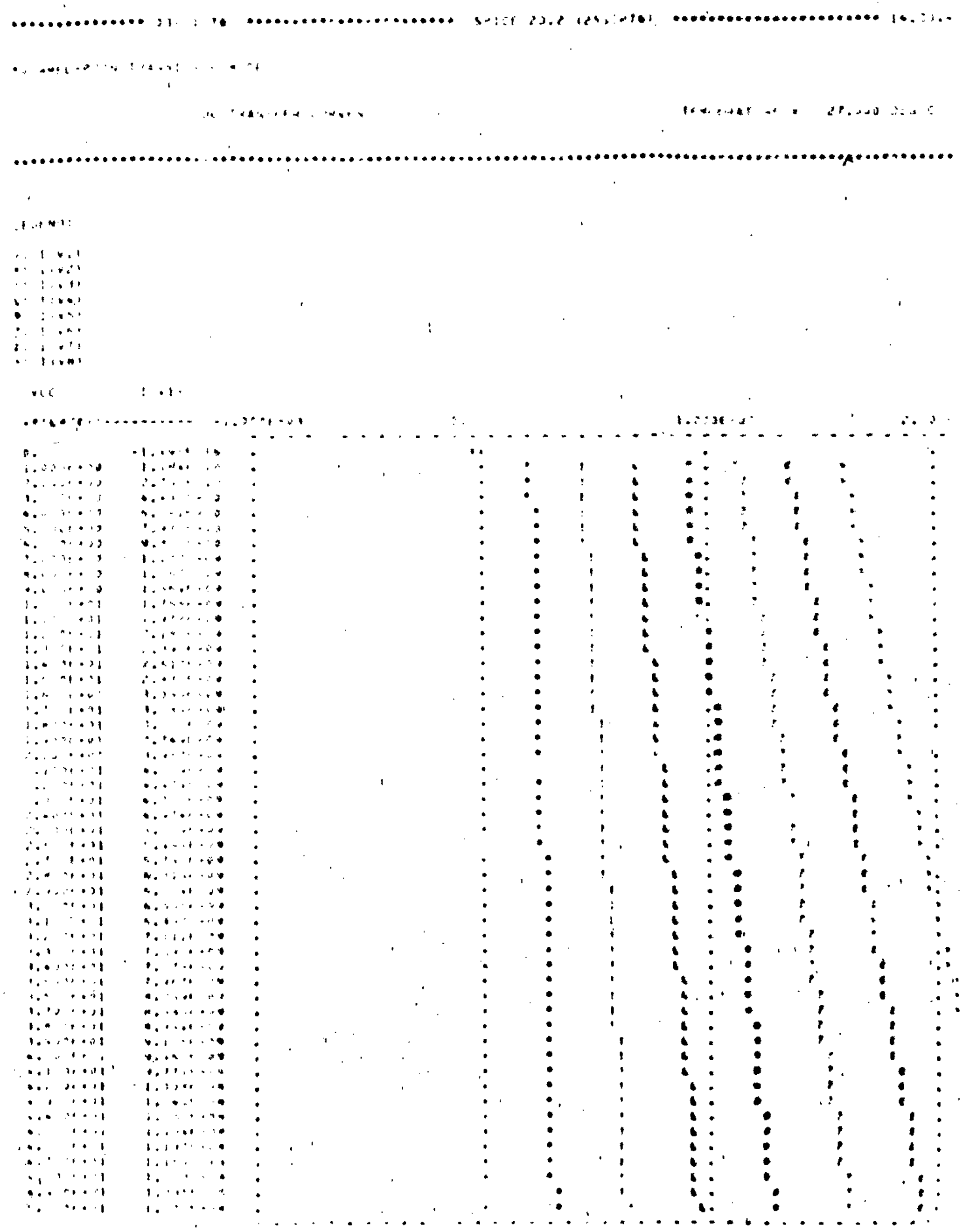


Figure III-57. Simulated "Curve Trace"

(1) Distributed Junction Capacitance

(2) Transit Time Variations with Collector Current

(3) Parameter Variations with Temperature

Techniques for modeling these second order effects are discussed in this section.

b. Advantages

Increased simulation accuracy may be obtained by inclusion of second order effects.

c. Cautions

Inclusion of second order effects increases complexity, simulation time, and parameterization time. Second order effects should only be modeled when the extra accuracy is absolutely necessary.

d. Characteristics

The collector-to-base capacitance is not a simple capacitance, but is distributed across the high base sheet resistance. The simplest lumped model for this distributed transition capacitance is given by figure III-58 RATIO is a parameter which defines how C_{jC} is split.

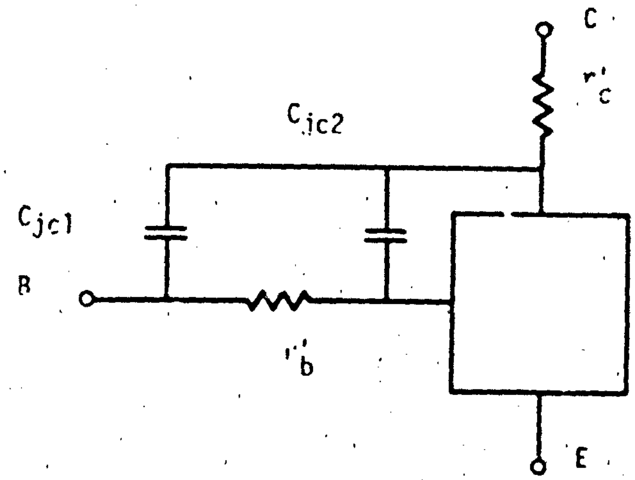


Figure III-58. Distributed Base Capacitance

e. <u>Defining Equations</u>

$$C_{jc1} = (C_{jC})(\text{RATIO})$$

$$C_{jc2} = (C_{jC})(1 - \text{RATIO})$$

$$\text{PARAMETER }(T) = \text{PARAMETER }(\text{Tnom})\left[1 + TC_1 (T - \text{Tnom}) + TC_2 (T - \text{Tnom})^2\right]$$

f. <u>Parameterization</u>

1) <u>RATIO</u>

a) <u>Definition</u>

RATIO defines the split of the collector-base junction capacitor C_{jC} across the base resistor r_b'.

b) <u>Typical Value</u>

A typical value of RATIO is 0.8. RATIO must lie between 0 and 1.

c) <u>Measurement</u>

RATIO is a difficult parameter to determine from terminal measurements. It can be determined easily if the topology of the device is known from:

$$\text{RATIO} = \left(1 - \frac{A_E}{A_B}\right)$$

where A_E is the area of the emitter and A_B is the area of the base including the emitter area.

2) <u>$\tau_F (I_C)$</u>

a) <u>Definition</u>

$\tau_F (I_C)$ models the variation of total transit time with collector current. It may be described by a piecewise linear table, a fit to an empirical function, or by fitting to:

$$\tau_F = \tau_{FLO}\left[1 + \frac{1}{4}\left(\frac{L_E}{W}\right)^2\left(\frac{I_C}{I_{CO}} - 1\right)^2\right]$$

where:

L_E = the smallest emitter width

W = the base width

I_{CO} = the current at which τ_F starts to rise

This expression is applicable if the data form is as shown in figure III-59. Two points on the curve could be taken and the two simultaneous equations solved for L_E/W and I_{CO} or a curve fitting routine could be used.

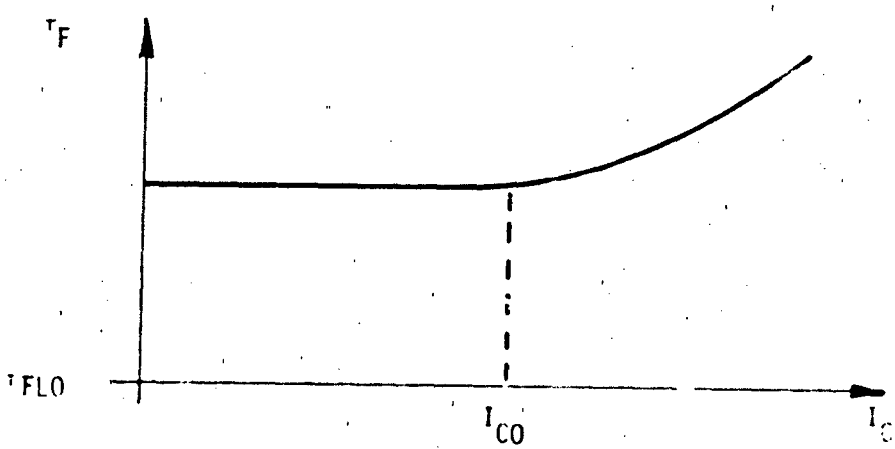


Figure III-59. Dependence of τ_F on Collector Current

b) <u>Example - 2N2222A</u>

The manufacturer specification sheets shown in figure III-5 give a plot of f_T versus collector current. This plot may be reduced to a plot of τ_F versus collector current applying:

$$\tau_F = \frac{1}{2\pi\ f_T} - C_{jC}\ r_c'$$

where:

$C_{jC} = 4.5$ pF

$r'_c = 12.5\ \Omega$

which produces the total transit time data listed in table III-10.

TABLE III-10. τ_F VARIATIONS

I_C	f_T	τ_F
0.1 mA	12 MHz	1.32×10^{-8} seconds
0.2	23	6.86×10^{-9}
0.5	54	2.89×10^{-9}
1.0	90	1.71×10^{-9}
2.0	140	1.08×10^{-9}
3.0	170	8.80×10^{-10}
5.0	200	7.4×10^{-10}
10.0	240	6.07×10^{-10}
20.0	280	5.12×10^{-10}
30.0	300	4.74×10^{-10}

Figure III-60 is a plot of τ_F (I_C). It does not appear that the parameters L_E/W and I_{Co} are applicable to the 2N2222A.

3) TC_1, TC_2

TC_1 and TC_2 are the first and second order temperature coefficients of parameters which may vary with temperature. PARAM is the temperature variable parameter. TC_1 and TC_2 describe a simple fit to experimental data obtained from an environmental chamber.

6. Photocurrent Effects

a. Description

Photocurrents in the transistor are produced in a similar manner as within the diode. The geometry, however, is more complex.

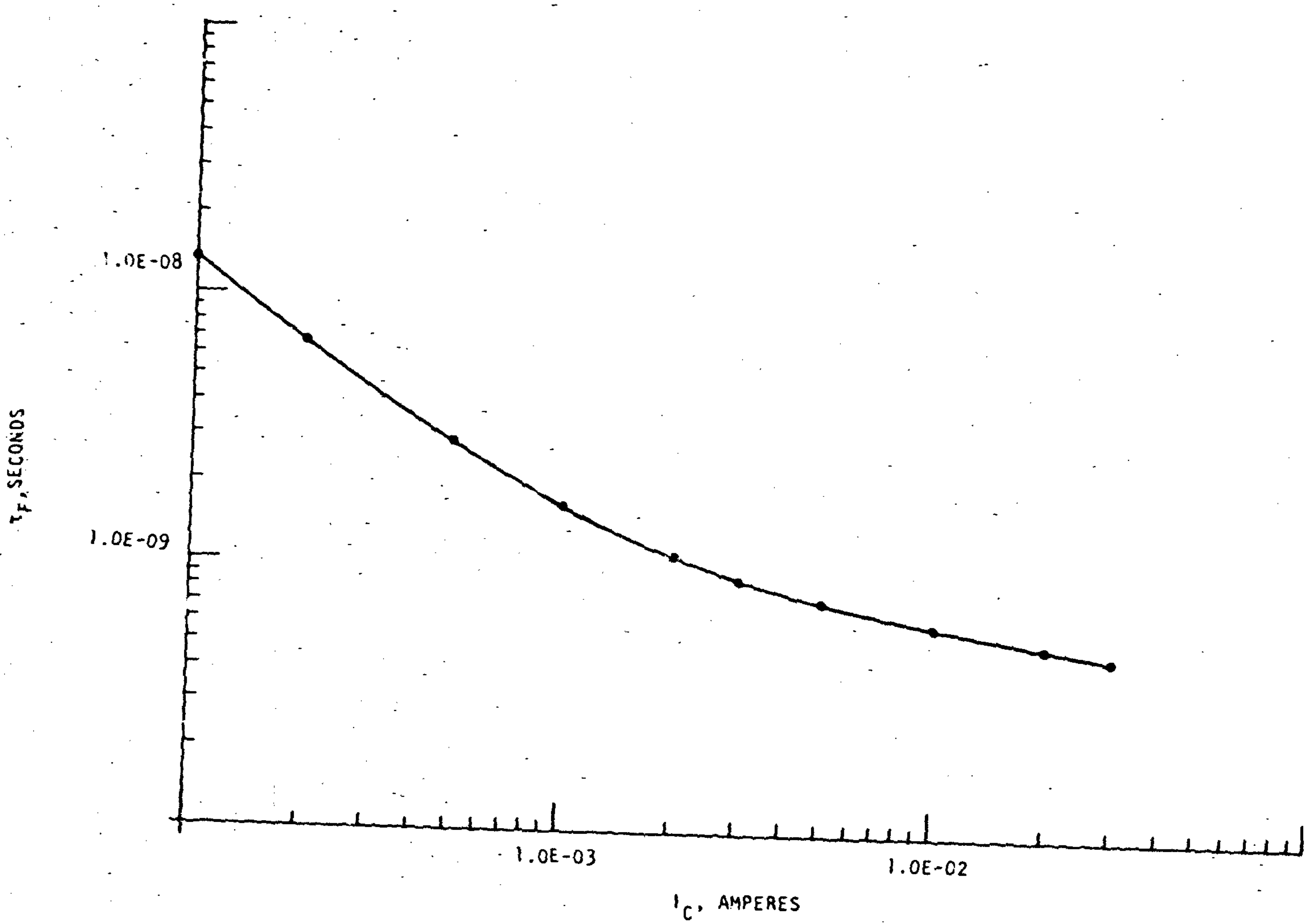


Figure III-60. Total Transit Time Versus Collector Current

Consider the schematic transistor of figure III-61 which is in the normal operating region. When exposed to ionizing radiation, photocurrent is produced at the base-collector junction and at the base-emitter junction. The base-emitter photocurrent is often ignored since it is usually much smaller than the base-collector photocurrent. Photocurrent at the base-collector junction will consist of a prompt component consisting of pairs generated within the depletion region, W_c, and a delayed component of minority electron and holes one diffusion length away from the depletion region edge (L_{pc}, L_{ec}).

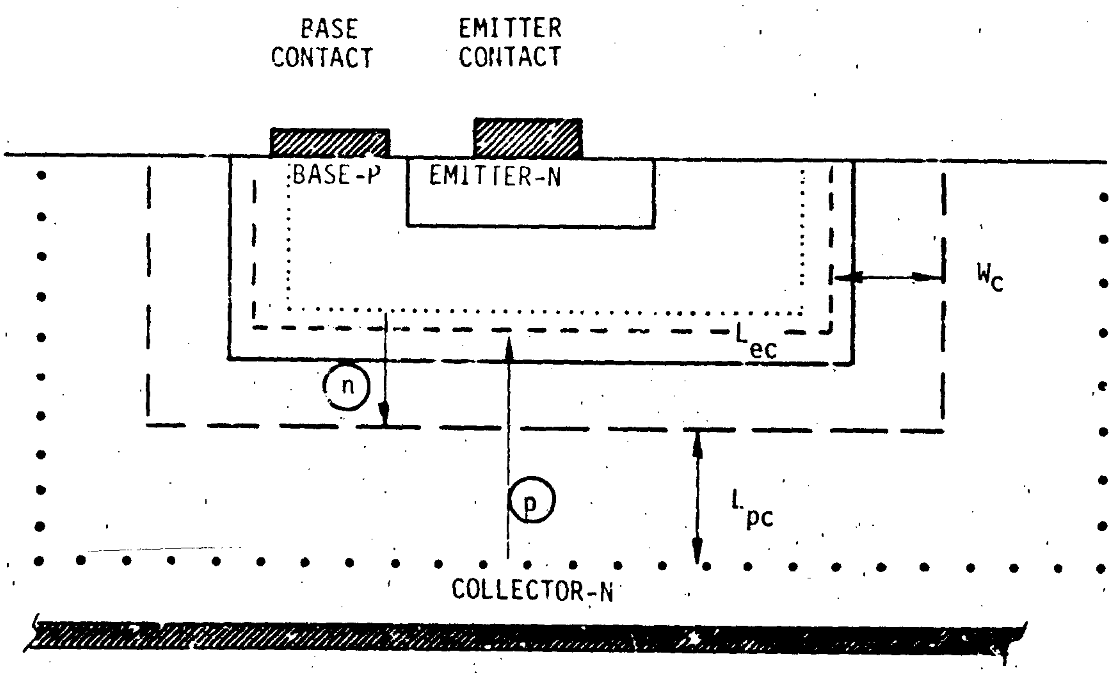


Figure III-61. Transistor Geometry (NPN)

If a detailed time dependent prediction is desired, the photocurrent generators should be treated in the manner discussed in chapter II.B.8. The physical parameter estimation techniques found by terminal measurements for the diode may be applied to the base-collector terminals of the transistor.

One of the simplest yet effective ways to predict photocurrent magnitude is by the use of the equations developed by J. K. Notthoff (see ref. III-3). Notthoff's equations are time independent and predict the peak primary photocurrent. They allow calculation of primary photocurrent from manufacturer data sheets and require no measurements or tests to be performed.

Primary photocurrent which is produced across the base-collector junction may flow across the base-emitter junction to be multiplied by the β of the transistor. The resulting collector current is the secondary photocurrent of the transistor. The magnitude of the secondary photocurrent will be a strong function of r_b' and external resistance in the base lead.

To obtain only the primary photocurrent, ionizing radiation tests often measure only the photocurrent flowing from the collector to the base by leaving the emitter lead open. This measured primary photocurrent can then define a base-collector current generator through tables, double exponentials, etc. A drawback of this method is that changes in bias and dose rate are not easily handled.

b. Advantages

Inclusion of photocurrent generators will allow the prediction of circuit response to ionizing radiation. Determination of the value of the photocurrent generator from experimental data is the simplest method. Prediction from terminal measurements allows time dependent predictions. Implementation of Notthoff's equations require only the data sheet information.

c. Cautions

Prediction from experimental data allows no flexibility for parameter changes. Prediction from terminal measurements requires laboratory facilities. Prediction from Notthoff's equation does not allow time dependency.

d. Characteristics

The placement of photocurrent generators (I_{pp}) is illustrated in figure III-62.

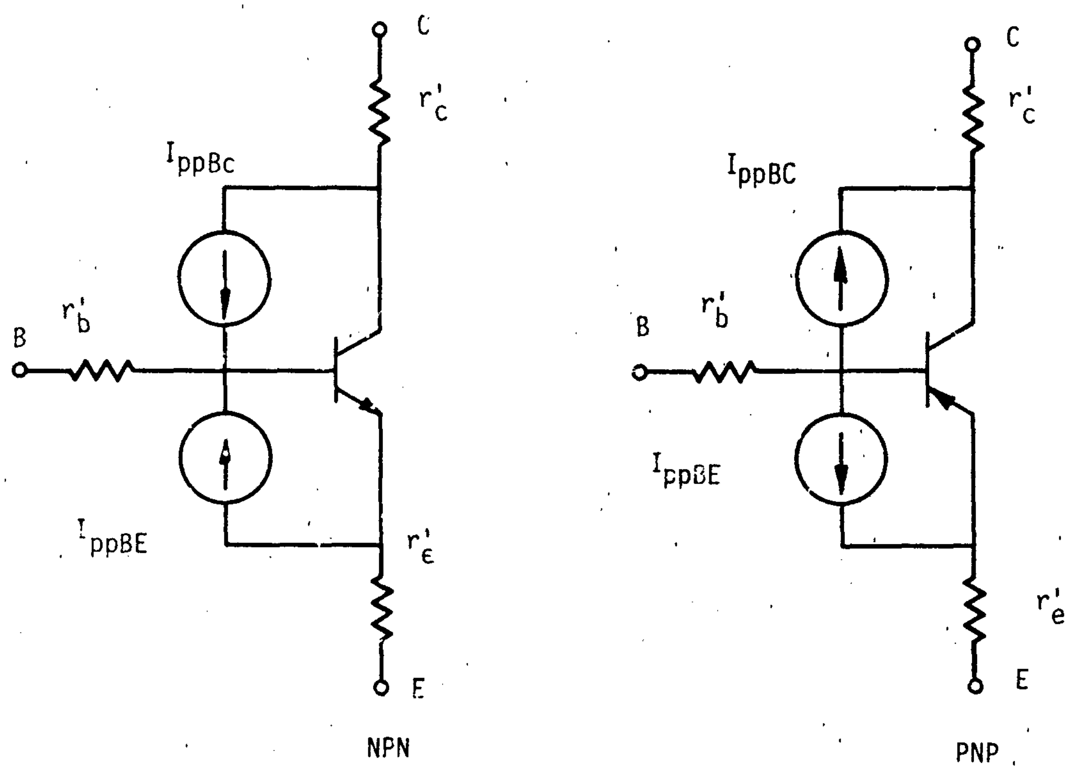


Figure III-62. Placement of Photocurrent Generators

e. Defining Equations

Notthoff's equations are listed in table III-11. The accuracy of prediction by Notthoff's equations is illustrated in figure III-63.

f. Parameterization

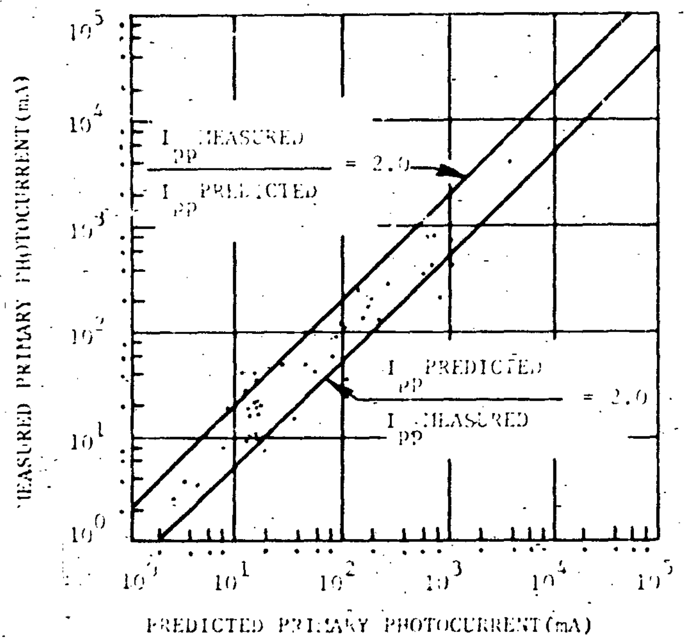
The 2N2222A is listed as a switching and amplifier transistor. Two of Notthoff's equations are applicable. The equation for switching transistors is the first applicable equation. From the data sheets shown in figure III-5, the equation may be parameterized as:

TABLE III-11. DEFINING EQUATIONS

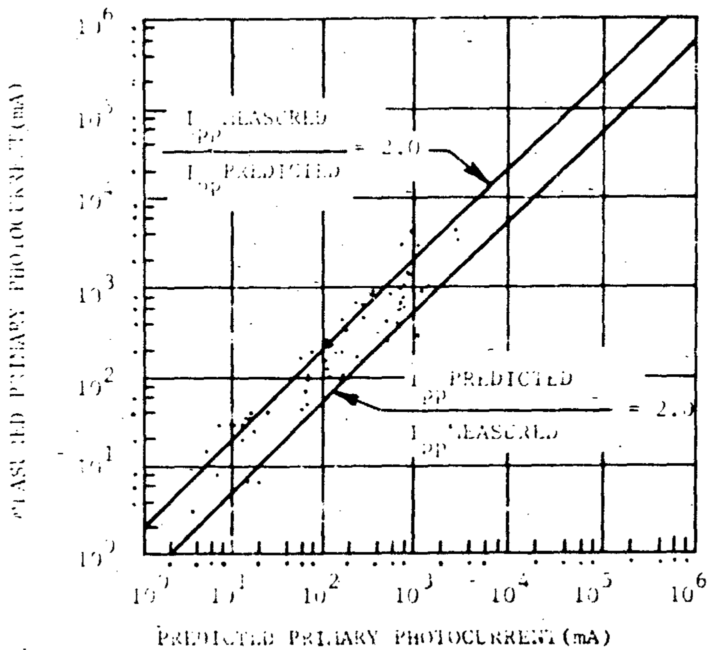
Polarity	P_D (Watts) (Note 1)	Type (Note 2)	Prediction Equation I_{pp} =	
NPN	to 0.6	SW	$\dot{\gamma} C_{CB1} V_{CB1}^{1/3} t_s^{1/2} \left(6.47 + V_{CB2}^{1/3}\right)$	6×10^{-12}
PNP	to 0.6	SW	Same as Above	9.5×10^{-12}
NPN	0.8 to 1.0	SW	Same as Above	1.7×10^{-11}
PNP	0.8 to 1.0	SW	Same as Above	2.6×10^{-11}
NPN	2.0 and over	SW	Same as Above	4×10^{-11}
PNP	2.0 and over	SW	Same as Above	6.3×10^{-11}
NPN	All	Amp	$\dot{\gamma} f_T^{-2/5} \; V_{CBO} \left(C_{CB1} V_{CB1}^{1/3} + 1.08\right) \left(21.6 + V_{CB2}^{1/3}\right)$	3.24×10^{-13}
PNP	All	Amp	Same as Above	4.8×10^{-13}

NOTES:

1. Power Dissipation at $T_A = 25°C$.
2. SW = Switching; Amp = Amplifier.
3. Units are mA, rad (Si)/s, pF, Volts, GHz, ns.
4. V_{CB1} is voltage at which C_{CB1} is specified.
5. V_{CB2} is voltage at which device is to be operated.



(a) Predicted vs Measured Primary Photocurrents in Silicon Switching Transistors at 10^{10} rad(Si)/s



(b) Predicted vs Measured Primary Photocurrents in Silicon Amplifier Transistors at 10^{10} rad(Si)/s

Figure III-63. Predicted Versus Measured Primary Photocurrents in Silicon Switching and Amplifier Transistors (After Notthoff, Reference III-2)

$$I_{pp} = \dot{\gamma}\ (8\ pF)(10\ V)^{1/3}\ (225\ ns)^{1/2}\ (6.47 + V_{CB2}^{1/3})\ \ 6 \times 10^{-12}$$

The equation for all NPN amplifiers yields:

$$I_{pp} = \dot{\gamma}\ (0.3\ GHz)^{-2/5}\ (75\ V) \left[(8\ pF)(10\ V)^{1/3} + 1.08 \right]$$

$$(21.6 + V_{CB2}^{1/3})\ (3.24 \times 10^{-13})$$

g. <u>Example - 2N2222A</u>

A simulation of a 2N2222A transient ionizing radiation test was made by application of Notthoff's equations. As an approximation, the photocurrent predicted by these equations was given a waveshape identical to the ionizing waveform discussed in the diode photocurrent example. From dosimetry, the peak ionizing dose rate was taken to be 1.16×10^{10} rad (Si)/sec.

The test circuit used for the actual test and the simulation is shown in figure III-64.

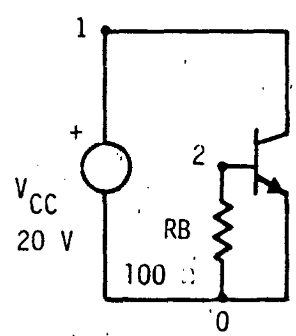


Figure III-64. Photocurrent Test Circuit

Notthoff's equations for these conditions (V_{CB2} = 20 V, $\dot{\gamma}$ = 1.16×10^{10}) yields the results.

$$I_{pp}\ (SW) = 165.26\ mA$$
$$I_{pp}\ (AMP) = 203.19\ mA$$

The results from the switching transistor equation were applied.

The results of the actual test are illustrated in figure III-65. The current probe used to monitor the test has a response of 5 mV/mA. The peak photoresponse is about 920 mA. The SPICE simulation circuit is listed in figure III-66. The simulation results are shown in figure III-67. The predicted peak photocurrent was 456 mA. The experimental waveform lasted roughly 300 ns. The predicted waveform lasted about 180 ns.

7. Neutron Effects

The two major effects of neutron damage, increased density of recombination centers and carrier removal, may produce serious degradation of the performance of the transistor.

The carrier removal effect will result in an effective counterdoping of all regions of the semiconductor. One effect of lighter doping is to increase junction breakdown. Experiments, however, indicate that this effect is relatively small for transistors. The change in BV_{CEO} will be significant due to the gain dependency of this parameter (see chapter III.B.2).

Another effect of counterdoping will be to increase the resistivity of the semiconductor. The increase in resistivity is especially pronounced in the lightly doped regions. Since the collector region is usually lightly doped in a planar process, an increase in the collector bulk resistance is expected.

The increased density of recombination centers will produce several effects, the most important being the degradation of transistor gain. Minority carriers which are injected into the base from the emitter must cross the base region to reach the collector as collector current.

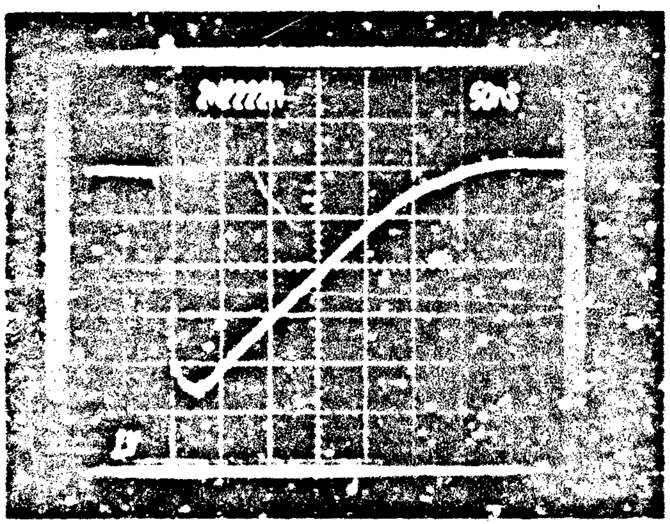


Figure III-[illegible] Secondary Photoresponse of [illegible]

```
••••• 03/03/78 •••••••• SPICE 20.2 (26SEP76) ••••••••• 09.43.09.

*SECONDARY PHOTORESPONSE TEST

     INPUT LISTING                          TEMPERATURE =   27.000 DEG C

••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••••

VCC 1 0 20.
RR  2 5 100.
V1 1 2 0 00
IPP 1 2 PWL(0 0 12.E-9 165.26E-3 15.E-9 165.26E-3 28.E-9 6
+ 92.E-9 0 100.E-9 0)
.MODEL Q0 NPN(BF=100 BR=30 IS=3.E-14 RB=100 RC=15 RE=0.25 VA=
+       C2=6.67E-2 NE=1.085 IK=192.E-3 IKR=18.2E-3 C4=6.57
+             TF=9.59E-10 TR=6.29E-8 CJE=23.12E-12 PE=0.5
+             CJC=12.36E-12 PC=0.6 MC=0.32 EG=1.11)
.TRAN 5NS 200NS
.PLOT TRAN I(VCC)
.END
```

Figure III-66. SPICE Simulation Listing

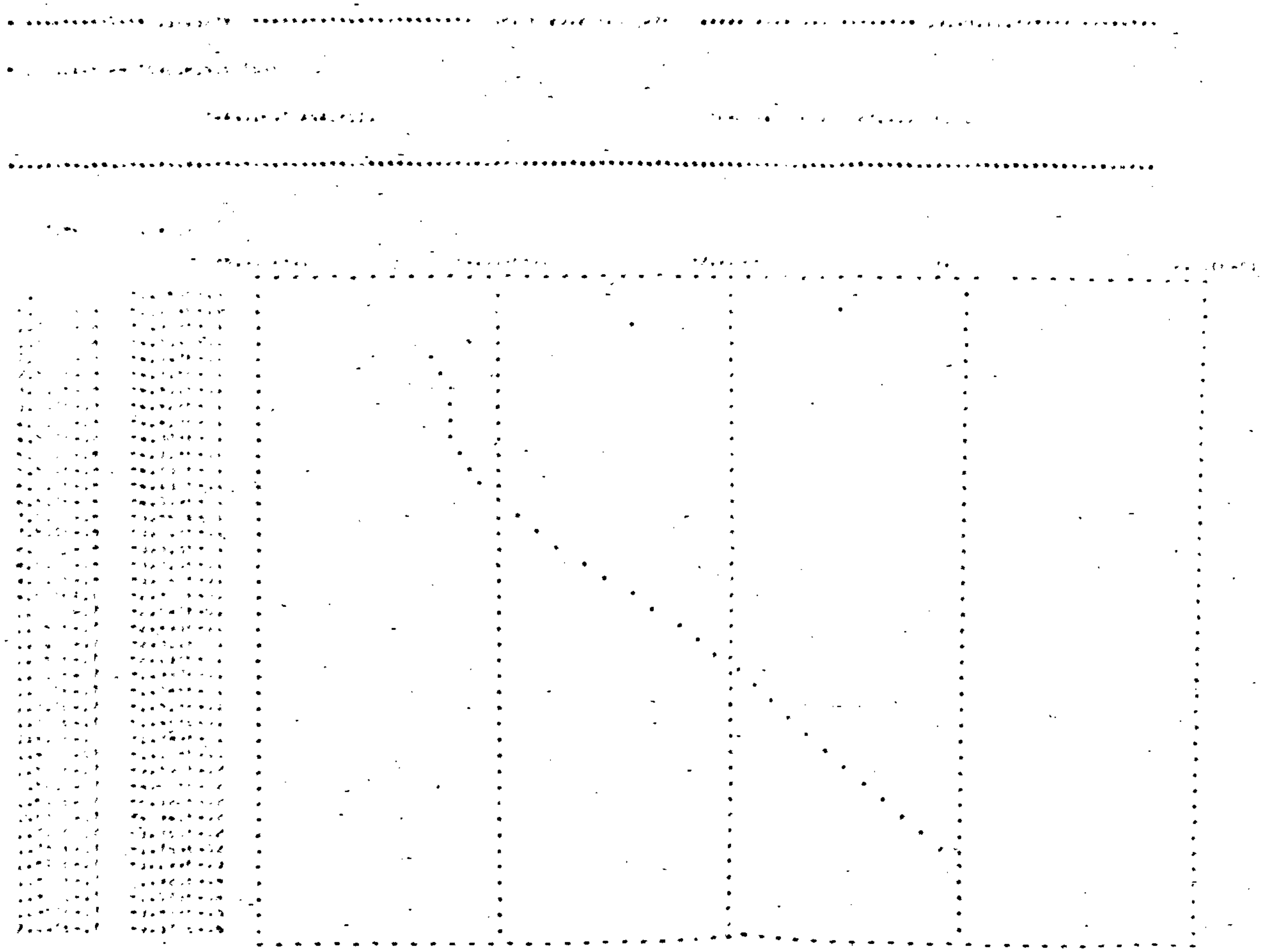


Figure III-67. Predicted Secondary Photoresponse

Carriers injected into the base are not at equilibrium and may recombine with the majority carriers in the region producing base current. The addition of recombination centers to the base will increase the recombination process producing more base current and less collector current. The net result is a loss of gain.

Very narrow base widths mean less time for base transit and therefore less chance for recombination, higher gain, and higher frequency performance. This is the basis for the Messenger-Spratt equation:

$$\frac{1}{\beta_\phi} - \frac{1}{\beta_0} = \frac{K\phi}{2\pi f_T}$$

where:

β_0 = the preirradiation β

β_ϕ = the postirradiation β

K = an empirical constant approximately equal to 10^{-6} cm^2/n-sec

ϕ = the neutron fluence in n/cm^2 in 1 MEV equivalents

Other effects of the increased recombination center density are increased junction leakage, decreased diffusion capacitance, and increased collector resistance.

It has now been stated that both the carrier removal effect and the increase in recombination center density will affect the collector bulk resistance. An increase in collector resistance coupled wth a decrease in beta may produce a serious change in the saturation characteristics of a transistor. First, the decrease in beta will require an increase in base current to bring a transistor into saturation. The increased collector resistance will produce a higher collector-emitter saturation voltage. The change in saturation voltage is frequently the most important radiation effect for switching transistors.

While the most important neutron radiation effect, gain degradation, may be estimated from terminal measurements or data sheet information, test data are the most reliable.

Test data may be obtained from such sources as the CRIC data base if experimental facilities are not available (see reference III-4).

All changes to a transistor, including those represented by complex interactions such as collector resistance, may be determined by simply remodeling the transistor from tests described in this chapter.

8. Total Dose Effects

Ionizing radiation alters the behavior of semiconductor surfaces. The major effects are the accumulation of positive charge in the passivating oxide and an increased density of surface states at the silicon-oxide interface. The net result will be an enhancement or depletion of the semiconductor surface.

The surface field may produce a loss in gain of silicon passivated transistors. Surface damage will produce an additional leakage component for the reverse biased collector base junction, and an additional base current component for the forward biased, base emitter junction. Transition capacitance may undergo an increase.

Unfortunately, the effect of ionizing radiation on the surface of transistors cannot be predicted from the physical characteristics of the transistor. The fact that damage appears to be bias dependent further complicates the problem.

At the present time, the effects of total ionizing dose are best modeled from information obtained through experiment.

9. Burnout

Electrical overstress or even extreme bias conditions may produce overheating and failure of the transistor. For EMP simulations, burnout will usually involve the breakdown of a transistor junction and the subsequent heating. The best technique currently available for failure prediction is to treat the two junctions of the transistor as two interrelated diodes each of which has associated failure constants, K. These diodes may be analyzed by the techniques discussed in Chapter II.B.10.

10. Linvill Lumped Model of the Transistor

a. Introduction

In chapter II.B.12, the concept of modeling the physical processes within a bipolar semiconductor device using lumped, linear network-like elements was discussed. These concepts may be applied directly to transistor models which will be discussed briefly in this section.

The Linvill "lump" represents an arbitrarily small slice or volume of semiconductor material. Each slice is made up of the Linvill elements which represent the physical behavior of minority charge carriers in the slice. The storance element represents charge storage, combinance represents charge recombination, diffusance represents charge diffusion, and driftance represents charge behavior in an electric field. The Linvill lumps are coupled with the Linvill P-N junction. The Linvill P-N junction models the "law of the junction" which defines minority carrier concentration at the junction edge as a function of the voltage across the junction.

The Linvill transistor model can now be seen as two Linvill P-N junctions separated by a region of either P- or N-type semiconductors. Obviously, the accuracy of the model will be a function of the number of lumps and the size (for example, 1/2 base width) of the lumps. As a general rule, however, only the smallest number of lumps that permits a sufficiently accurate model should be used.

The base region of a transistor is designed to be narrow compared to the minority carrier diffusion length. For this reason, a single π representation of two lumps is usually sufficient to model the behavior of the base region. Doping gradients, etc. may produce an electric field across the base so carrier movement in the base may be represented by the driftance element as well as the diffusance element. At this point, the simplest transistor model, the two-lump model, is defined. This model is shown in figure III-68. Relevant expressions for this model are:

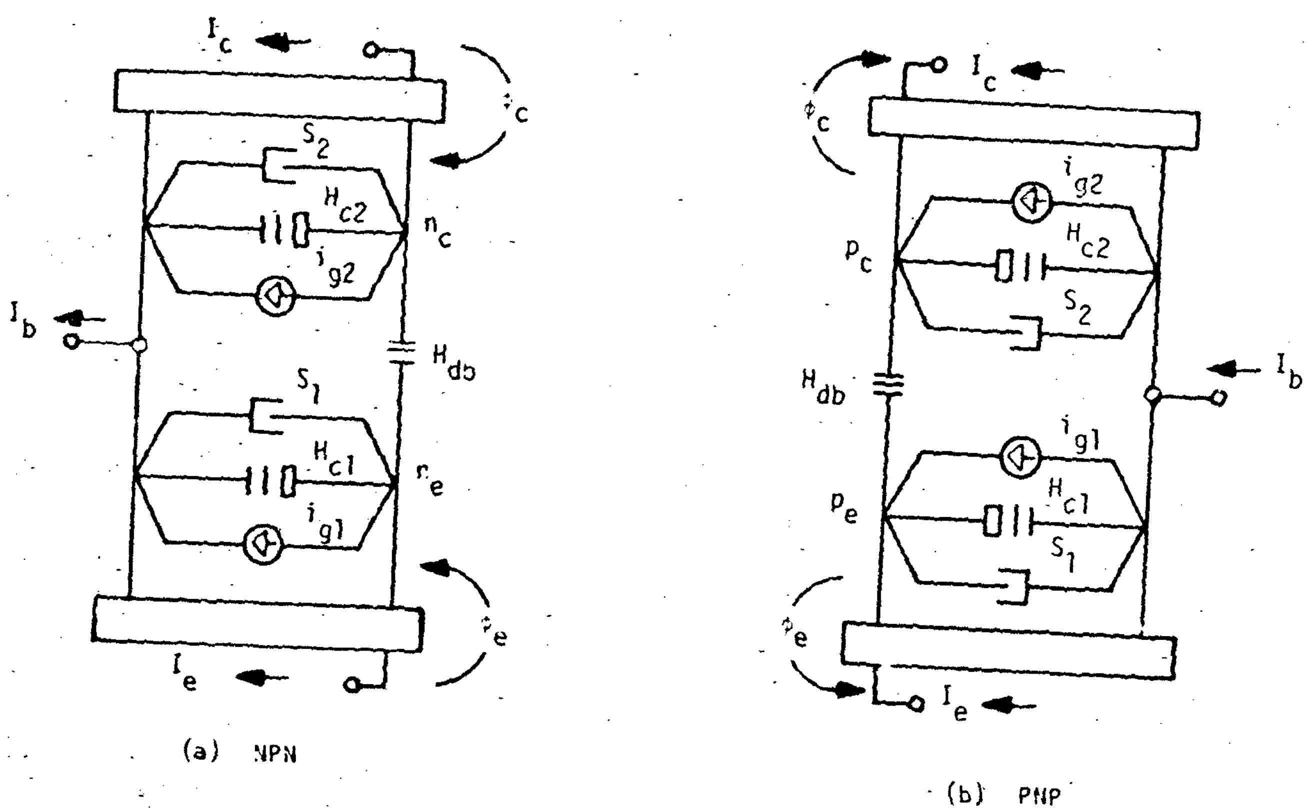


Figure III-63. Two Lump Transistor Models

$$m_o \ (H_{dB} + H_{C1}) = I_{ES}$$

$$m_o \ H_{dB} = \alpha_I \ I_{CS} = \alpha_F \ I_{ES}$$

$$m_o \ (H_{dB} + H_{C2}) = I_{CS}$$

where m_o is the base equilibrium minority carrier concentration.

$$\frac{S_1}{H_{dB}} \approx \tau_F$$

$$\frac{S_2}{H_{dB}} \approx \tau_R$$

The emitter is usually heavily doped and has little effect on the radiation response of the transistor. Physically, the importance of the emitter is in determining the current gain of the transistor through emitter efficiency. Normally, no lumps or only one lump is used to model the emitter region.

The lightly doped collector region will significantly affect the charge storage behavior and the photoresponse of the transistor. Because the length of the collector is generally long compared to the minority carrier diffusion length, a number of lumps modeling the collector region may be necessary.

Other regions, such as the substrate buried layer and isolation region and junction, may also be considered for modeling. If even higher accuracy is required, two dimensional Linvill structures may be built to simulate lateral effects.

Radiation effects for Linvill models are discussed in chapter II.B.12. For neutrons, the change in the combinance elements of the base will model transistor gain degradation as this element will reflect the increase in recombination centers produced by the impinging neutrons. If photocurrent predictions are desired, the collector region must be modeled. The two lump model will not predict the shape of the primary photocurrent waveform.

The values of the lumped elements cannot be easily determined by terminal measurements. As a consequence, the Linvill transistor model is better suited to research into device behavior than for practical nuclear hardness assessments. However, to demonstrate the implementation of a transistor model by a network analysis code, rough approximations were used to produce a two lump Linvill model of the 2N2222A.

b. Example of Two Lump Transistor Model

1) Description

The Linvill lumped model for the transistor represents the development of a symbolic model consisting of lumped, linear, network-like elements which represent physical events within the device. These elements represent actual physical processes occurring in transistors such as charge diffusion, recombination, generation, storage, and drift.

2) Advantages

The Linvill lumped model of the transistor gives the analyst greater insight into the physical processes occurring in the transistor.

3) Cautions

The principal disadvantage of the lumped model is that the lumped elements are not directly measurable. The number of codes adaptable to the Linvill formulation are also limited.

4) Characteristics

The concept of modeling using Linvill lumped elements is discussed in chapter II.B.12. One concept is that model accuracy improves with increasing number of lumps. For practical use, the model needs to be as simple as possible.

The simplest transistor model is a two lump subdivision of the base. The total excess charge stored in the base is then divided into two independent lumped components contained in these two lumps. Two lump models of transistors are illustrated in figure III-68.

5) <u>Defining Equations</u>

$$i_{g1} = P_{no} H_{C1} + \frac{qA_B W}{2} g_o \dot{\gamma} \quad \text{(if PNP)}$$

$$i_{g2} = P_{no} H_{C2} + \frac{qA\ W_B}{2} g_o \dot{\gamma} \quad \text{(if PNP)}$$

$$i_{g1} = n_{po} H_{C1} + \frac{qA_B W}{2} g_o \dot{\gamma} \quad \text{(if NPN)}$$

$$i_{g2} = n_{no} H_{C2} + \frac{qA\ W_B}{2} g_o \dot{\gamma} \quad \text{(if NPN)}$$

$$p_e = p_{po} \left[\exp \left(\frac{q\phi_e}{KT} \right) -1 \right]$$

$$p_c = p_{no} \left[\exp \left(\frac{q\phi_c}{KT} \right) -1 \right]$$

$$n_e = n_{po} \left[\exp \left(\frac{q\phi_e}{KT} \right) -1 \right]$$

$$n_c = n_{po} \left[\exp \left(\frac{q\phi_e}{KT} \right) -1 \right]$$

(assuming uniformly doped base)

$$\frac{S_1}{H_{dB}} \approx \tau_F$$

$$\frac{S_2}{H_{dB}} \approx \tau_R$$

6) <u>Parameter List</u>

S = the values of the storance elements

H_C = the value of the combinance elements

i_g = the value of the charge generation current generator
I_c = the collector current
I_b = the base current
I_e = the emitter current
n = the concentration of minority carrier electrons
p = the concentration of minority carrier holes
n_{po} = the equilibrium concentrations of minority carrier electrons
P_{no} = the equilibrium concentration of minority carrier holes
ϕ_e = the voltage potential across the emitter junction
ϕ_c = the voltage potential across the collector junction
W_B = base width
A = base area
$\dot{\gamma}$ = ionizing dose rate
g_o = generation rate

7) Parameters to be Found

n_{po}
P_{no}
S_2
H_{C2}
S_1
H_{C1}
H_{dB}

8) Parameterization

a) n_{po}, P_{no}

1 Definition

n_{po} and p_{no} are the equilibrium minority carrier concentrations in P- and N-type material, respectively. n_{po} is required for the base material if dealing with an NPN transistor. P_{no} is

required for the base region if a PNP transistor is being considered. An important assumption is that the transistor is abrupt and uniformly doped.

2 Typical Value

Values for n_{po} and p_{no} vary widely. A typical value is 1×10^4 carriers/cm^3.

3 Measurement

If the doping concentration of the base is known, a minority concentration m_o (n_{po} or p_{no}) can be calculated as:

$$m_o = \frac{n_i^2}{N_B}$$

where:

N_B = the doping concentration in the base

n_i = the intrinsic carrier concentration (1.45×10^{10} carriers/cm^3 for silicon at room temperature)

If the doping concentration is not known, an estimate of N_B can be obtained from BV_{EBO}, the base-emitter breakdown voltage as:

$$N_B = \left(\frac{V_{BD}}{2.72 \times 10^{12}}\right)^{-3/2}$$

assuming that the emitter is much more heavily doped than the base and that the emitter junction is planar.

b) H_{dB}

1 Definition

H_{dB} represents the diffusion of minority carriers through the base region.

2 Typical Value

A typical value for H_{dB} is 1×10^{-16} cm^3·A.

3 Measurement

H_{dB} can be determined from m_o (n_{po} or p_{no}) and I_S, which is described in chapter III.B.1 along with techniques to determine its value. H_{dB} can then be calculated to be:

$$H_{dB} = \frac{I_S}{I_o}$$

c) H_{C1}, H_{C2}

1 Definition

H_{C1} and H_{C2} are the values of the elements which represent the recombination of minority charge carriers in the base region.

2 Typical Values

Typical values for H_{C1} and H_{C2} are 1×10^{-18} and 1×10^{-16} $cm^3 \cdot A$, respectively.

H_{C1} and H_{C2} can be determined from m_o (n_{po} or p_{no}), I_S, H_{dB}, α_F, and α_R. I_S and α_R are parameters which are discussed in chapter III.B.1. From these parameters, H_{C1} and H_{C2} are found as:

$$H_{C1} = \frac{I_S/\alpha_F - m_o H_{dB}}{m_o}$$

$$H_{C2} = \frac{I_S/\alpha_R - m_o H_{dB}}{m_o}$$

d) S_1, S_2

1 Definition

S_1 and S_2 are the values of the two storance elements in the base region. S_1 and S_2 represent charge storage within the base.

2 Typical Values

Typical values for S_1 and S_2 are 1×10^{-24} $cm^3 \cdot C$ and 1×10^{-22} $cm^3 \cdot C$, respectively.

3 Measurement

S_1 and S_2 can be estimated from τ_F, τ_R, and H_{dB}. τ_F and τ_R are parameters developed in chapter V. S_1 and S_2 are estimated as:

$$S_1 = \tau_F H_{dB}$$

$$S_2 = \tau_R H_{dB}$$

9) Examples - 2N2222A

a) m_o

The doping concentration within the base is not directly available; therefore, the breakdown estimate will be made. Base-emitter breakdown voltage was measured at about 8 volts.

$$N_B = \left(\frac{8 \text{ V}}{2.72 \times 10^{12}}\right)^{-3/2} = 1.98 \times 10^{17} \text{ atoms/cm}^3$$

This implies an equilibrium electron concentration in the base of:

$$n_{po} = \frac{(1.45 \times 10^{10})^2}{1.98 \times 10^{17}} = 1.06 \times 10^3 \text{ electrons/cm}^3$$

b) H_{dB}

Choosing I_S from the basic transistor model, H_{dB} is:

$$H_{dB} = \frac{3.3 \times 10^{-14} \text{ A}}{1.06 \times 10^3 \text{ electrons/cm}} = 3.113 \times 10^{-17} \text{cm}^3 \cdot \text{A}$$

c) $\underline{H_{C1}, H_{C2}}$

Obtaining basic transistor model parameters:

$$H_{C1} = \frac{(3.3 \times 10^{-14} A)/(0.99567) - (1.06 \times 10^{3}/cm^{3})(3.113 \times 10^{-17} cm^{3} \cdot A)}{(1.06 \times 10^{3}/cm^{3})}$$

$$H_{C1} = 1.375 \times 10^{-19}\ A \cdot cm^{3}$$

$$H_{C2} = \frac{(3.3 \times 10^{-14} A)/(0.893) - (1.06 \times 10^{3}/cm^{3})(3.113 \times 10^{-17}\ cm^{3} \cdot A)}{(1.06 \times 10^{3}/cm^{3})}$$

$$H_{C2} = 3.538 \times 10^{-18}$$

d) $\underline{S_1, S_2}$

Applying the transit times from the charge storage model:

$$S_1 = (9.54 \times 10^{-10}\ \text{seconds})\ (3.113 \times 10^{-17}\ cm^{3} \cdot A)$$

$$= 2.97 \times 10^{-26}\ cm^{3} \cdot C$$

$$S_2 = (8.29 \times 10^{-8}\ \text{seconds})\ (3.113 \times 10^{-17}\ cm^{3} \cdot A)$$

$$= 2.58 \times 10^{-24}\ cm^{3} \cdot C$$

10) <u>Computer Simulation of the Linvill Transistor Model</u>

To demonstrate the implementation of the Linvill transistor model, the Linvill model was put through a simulated curve trace. The topology applied is demonstrated by figure III-69. The NET-2 input listing for this run is shown in figure III-70. The output for this run is shown in figure III-71

Some indication of the success of the Linvill transistor model can be found by checking the gain characteristic of the model. The

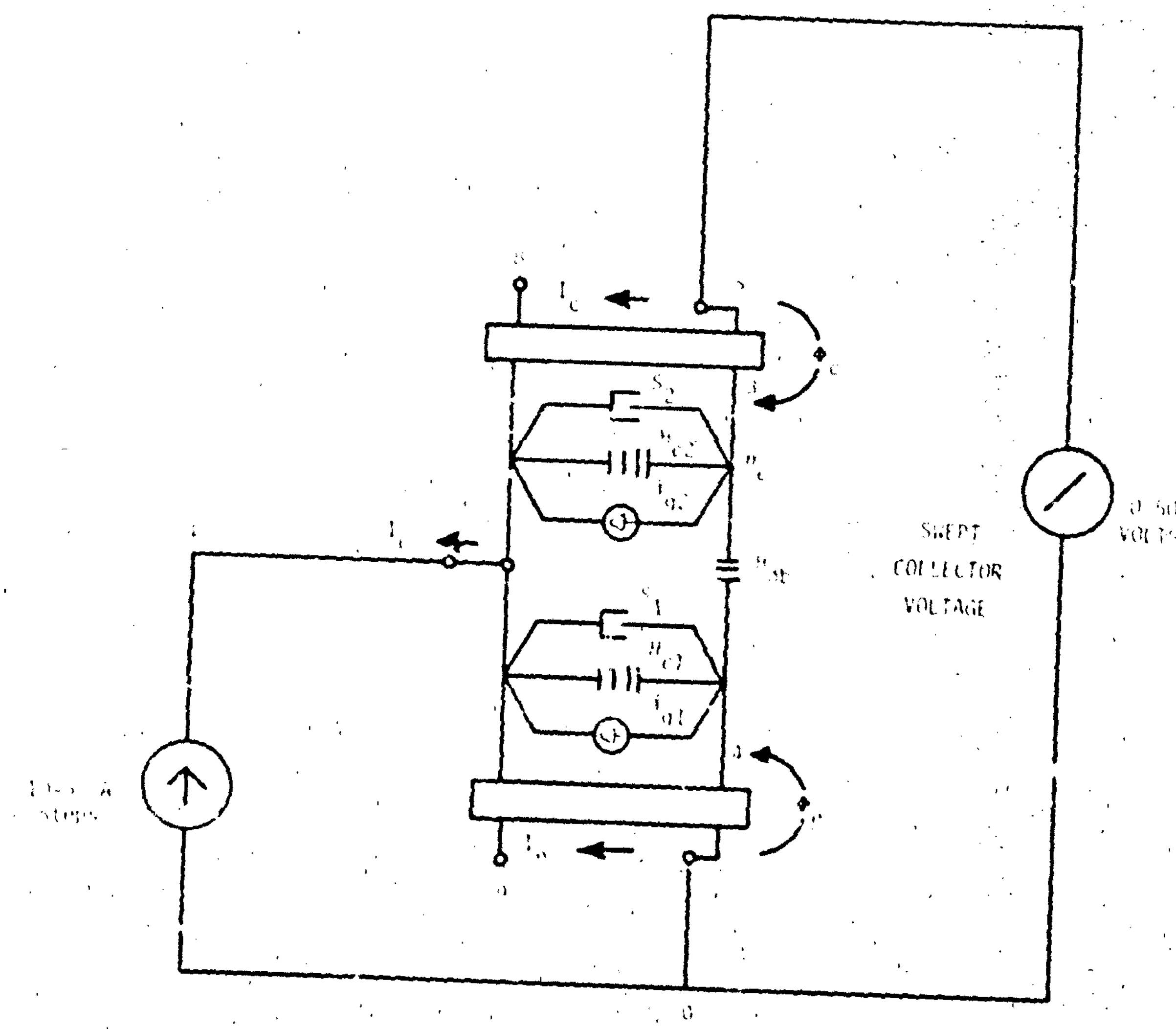


Figure III-69. Linvill Transistor Test Circuit 10-S A

```
NET-2 NETWORK ANALYSIS PROGRAM    RELEASE 9
03/22/78      16.30.45.

000000000111111111122222222223333333333444444444455555555556666666666777777777
123456789012345678901234567890123456789012345678901234567890123456789012345678
*LINVILL TRANSISTOR
PN1 1 2 3 3 CB
PN2 1 3 4 3 CE
ST2 1 3 2.35E-24
HC2 1 3 3.538E-18
I2 4 3 3.73E-15
ST1 1 4 2.47E-25
HC1 1 4 1.375E-19
I1 1 4 1.77E-15
HU1 4 3 3.113E-17
V1 0
V2 0
I3 3 0 P1
V1 2 0 P2
LIBRARY
    PN CB 9
        C 12.35E-12
        N 0.32
        VPO 1.0653
        PNO 0
        TM 35.5
        VZ 0.5
    PN CE 8
        C 23.12E-12
        N 0.342
        VPO 1.06E3
        PNO 0
        TM 35.5
        VZ 0.5
STATE1
    P2 0 (10) 1 (49) 50
    *P1 0 (10) 50.E-5
        PLOT I(V1) VS V(2)
END
```

Figure III-70. NET-2 Listing for Linvill Transistor

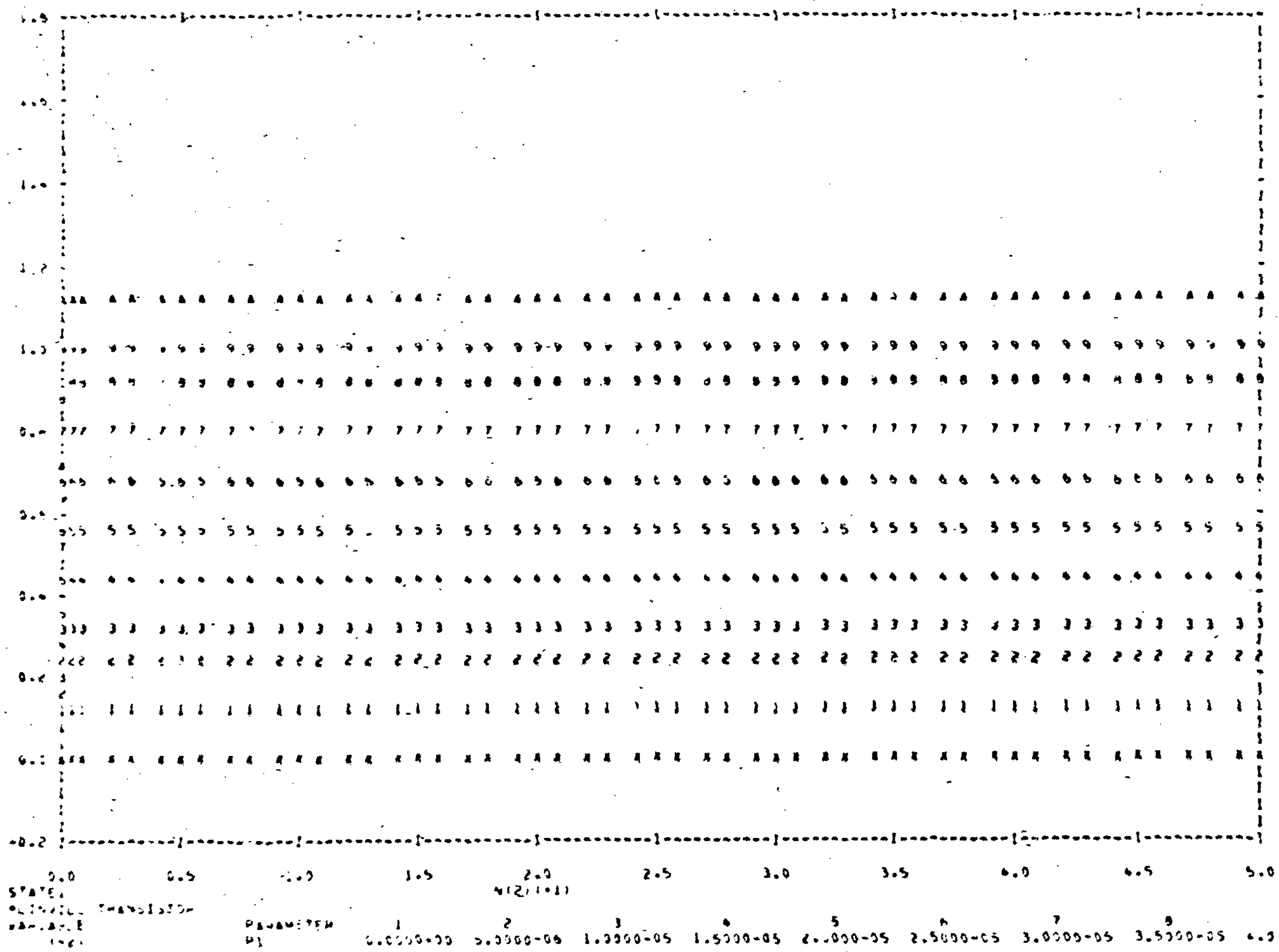


Figure III-71. Characteristic of Linvill Transistor

"A" points of figure III-69 represent the collector current produced by a base current of 50 microamperes. The collector current produced is about 11.2 mA. The model current gain is about 224. The actual gain is 230. The Linvill model used does produce the basic gain characteristics but should not be considered as representing physical reality because of the rough approximations made.

11. Code Implementation

Table III-12 is a set of conversion factors to allow the parameters obtained using this handbook to be applied by the more popular circuit analysis codes. A set of typical parameter values are given as default parameters in the event of incomplete characterization.

C. REFERENCES

III-1. "Semiconductor Data Library", Motorola Semiconductor Products Inc., 1974

III-2. Gretreu, I. Modeling The Bipolar Transistor, Tektronix, Inc., Beaverton, Oregon, 1976.

III-3. Notthoff, J. K. "Technique for Estimating Primary Photocurrents in Silicon Bipolar Transistors," IEEE Trans. Nuc. Sci., NS-16, no. 6, December 1969.

III-4. Radiation Effects on Semiconductor Devices, Harry Diamond Laboratories, HDL-DS-77-1, Adelphi, Maryland, May 1977.

TABLE III-12. CODE IMPLEMENTATION

MODELING HANDBOOK	CIRCUS 2	SCEPTRE*	NET-2	TRAC	SPICE	"SAFE" DEFAULT VALUES
r_b' (Ω)	RB (Ω)	RB (kΩ)	RBB (kΩ)	-	RB (Ω)	1×10^{-3} Ω
r_c' (Ω)	RC (Ω)	RC (kΩ)	RCC (kΩ)	-	RC (Ω)	1×10^{-4} Ω
r_e' (Ω)	-	-	-	-	RE (Ω)	1×10^{-5} F
C_{jeo} (F)	A1 (F)	COE (pF)	CE (pF)	CEO $(VEBI)^{1/2}$	CJE (F)	2×10^{-12} F
C_{jco} (F)	A2 (F)	COC (pF)	CC (pF)	CCO $(VCBI)^{1/2}$	CJC (F)	1×10^{-12} F
φ_E (V)	PHI1 (V)	ϕ_E (V)	VZE (V)	VEBI (V)	PE (V)	0.6 V
φ_C (V)	PHI2 (V)	ϕ_C (V)	VZC (V)	VCBI (V)	PC (V)	0.6 V
M_E	N1	N_E	NE	0.5	ME	0.5
M_C	N2	N_C	NC	0.5	MC	0.5
I_S (A)	-	-	-	-	IS (A)	1×10^{-14} A
I_{ES}	$\left[\frac{BN+1}{BN}\right]$ IES (A)	IES (mA)	IES/$\left[1-\frac{BN}{(BN+1)}\frac{BI}{(BI+1)}\right]$	IES (A)	-	1×10^{-9} A
I_{CS}	$\left[\frac{BI+1}{BI}\right]$ ICS (A)	IES (mA)	ICS/$\left[1-\frac{BN}{(BN+1)}\frac{BI}{(BI+1)}\right]$	ICS (A)	-	1×10^{-9} A
q/KT (V^{-1})	THETAN (V^{-1})	θ_E (V^{-1})	THE (V^{-1})	38.61/ME**	-	38.61 (V^{-1})
q/KT (V^{-1})	THETAI (V^{-1})	θ_C (V^{-1})	THC (V^{-1})	38.61/MC**	-	38.61 (V^{-1})
β_F	BN	$\alpha_N/(1-\alpha_N)$	BN	HFEN	BF	100
β_I	BI	$\alpha_I/(1-\alpha_I)$	BI	HFEI	BR	1
τ_F	$\left[\frac{BN}{BN+1}\right]$ TCN	T_E(ns)	1/WN (ns)	TN(S)	TF	0.1 ns
τ_R	$\left[\frac{BI}{BI+1}\right]$ TCI	T_S(ns)	1/WI (ns)	TI (S)	TR	10 ns
C2	-	-	-	-	C2	0
C4	-	-	-	-	C4	0
V_A	-	-	-	-	VA	200 V
V_B	-	-	-	-	VB	200 V
N_{EL}	-	-	-	-	NE	2.0
N_{CL}	-	-	-	-	NC	2.0

*not representative of examples in this modeling handbook

**room temperature

CHAPTER IV
MOS MODELING

CHAPTER IV

TABLE OF CONTENTS

CHAPTER IV

MOS MODELING

A. INTRODUCTION

The MOS (metal oxide semiconductor) transistor is a semiconductor device in which the current between two electrodes, the source and the drain, is modulated by a relatively small voltage applied to the gate electrode. The modulation is accomplished by attracting or repelling charge carriers to create a narrow, high conductivity channel near the surface of the semiconductor material. Since the gate electrode is separated from the semiconductor material by a high quality insulator, very little current flows between the gate and either the source or the drain. This produces an extremely high input impedance, which is the chief advantage of the device.

The construction and operation of the device can best be understood be referencing figure IV-1 (ref. IV-1). This figure represents an N-channel MOS transistor. The device is constructed by diffusing parallel N^+ source and drain regions into a lightly doped P-type substrate material. A thin layer of oxide is then grown over the region separating the source and drain. By depositing a layer of metallization (gate metallization) on top of the oxide and making electrical contacts to gate, source, drain, and substrate, a four terminal MOS transistor results.

For device operation, assume that the substrate and source are tied to ground and the drain is connected to a positive voltage. If a positive voltage is applied to the gate, electrons are attracted to the surface. At a sufficiently large gate voltage, the surface of the silicon will become N-type due to the presence of a large number of electrons. With this thin channel formed at the surface, current can flow from the drain to the source. Since the drain voltage is positive, a depletion

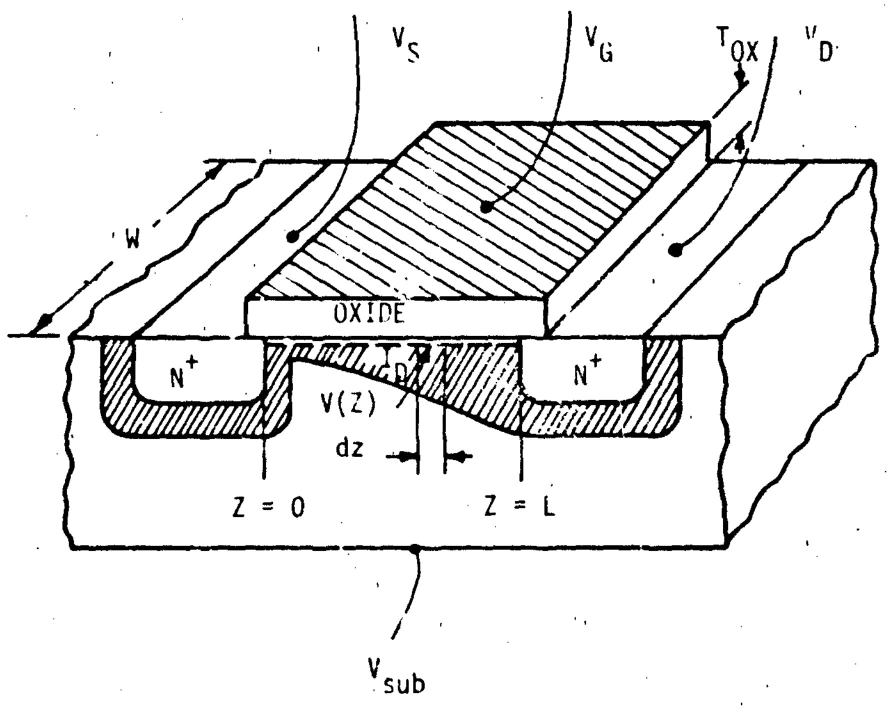


Figure IV-1. N-Channel MOS Transistor Diagram

region is formed around the N^+ P diode comprising the drain-to-substrate diode. As the drain voltage becomes increasingly positive, the depletion region expands until it eventually penetrates and pinches off the channel. Thus, once the channel is formed between source and drain, the current increases with increasing drain voltage until the pinchoff condition is reached and the current no longer increases with drain voltage.

Three regions of operation are of interest. The first region is "cutoff" in which no channel is formed between source and drain and no drain current flows. The second region of interest occurs once sufficient voltage has been applied between the gate and source to form a channel between drain and source. This is known as the triode region of operation and is characterized by increasing drain current with increasing drain voltage. The third region of interest is that of saturated operation in which the drain voltage has been increased until the channel is pinched off and drain current no longer increases with drain voltage.

MOS transistors can be fabricated so that they operate in either the enhancement mode or the depletion mode. The enhancement mode device has been generally described above. Without gate-to-source bias, a channel is not present between source and drain, and current will not flow. The carrier density near the surface must be "enhanced" in order for conduction to take place. For N-channel devices fabricated on P-type material, the gate voltage must be positive to form the channel. For P-channel devices fabricated on N-type material, the gate voltage must be negative to form the channel. The depletion mode device has a channel formed between the source and drain even without gate-to-source bias. Thus, the device is normally in an "on" condition. To turn the device "off," a gate voltage must be applied to drive carriers away from the surface and "deplete" the channel. For N-channel devices, the polarity of the depleting voltage will be negative. For P-channel devices, depleting voltage will be positive.

The ac performance of the MOS transistor is governed by parasitic capacitances which appear across:

(1) Gate to Substrate
(2) Gate to Source
(3) Gate to Drain
(4) Source to Substrate
(5) Drain to Substrate

The source-to-substrate and drain-to-substrate capacitances are depletion region capacitances normally associated with reverse bias PN junctions. Their values vary as a function of reverse biasing voltage as previously discussed in the chapter on bipolar diodes. The values of the gate capacitances vary as a function of gate voltages. Expressions describing the variation will be discussed in this chapter.

Note that MOS devices rely on majority carriers to transport current between the source and drain. As a result, variations in minority carrier lifetime have little affect on their performance. Consequently, minority carrier lifetime degradation induced by neutron irradiation is of little consequence for MOS devices. Some carrier removal effects associated with neutron irradiation may occur at high fluences ($\approx 10^{15}$ n/cm^2). Neutron damage to MOS devices will not be treated in this handbook.

Ionizing radiation produces hole electron pairs in the insulator (usually silicon dioxide, SiO_2) between the gate electrode and the channel as well as within the semiconductor material. Unfortunately, electrons have a higher mobility in SiO_2 than do holes. Therefore, electrons tend to be swept out of the oxide leaving trapped, positively charged holes behind. This positive charge tends to attract or repell carriers near the surface depending on whether the device is an N-channel or P-channel transistor. Ionizing radiation causes P-channel transistors to move toward enhancement mode operation, and N-channel transistors move toward depletion mode operation. In addition to oxide charge trapping, ionizing radiation increases the interface state density. This is reflected as a shift toward enhancement mode operation for both N-channel and P-channel devices. Thus, oxide charge trapping and interface state

density increases tend to be offsetting phenomena in N-channel devices and additive phenomena in P-channel devices. Both phenomena are a function of:

(1) Total Ionizing Dose Absorbed by the Device

(2) The Gate Voltage

(3) The Physical Properties of the Gate Insulator

The functional dependencies are complex and not thoroughly defined at this time.

Ionizing radiation also produces photocurrents in PN junctions associated with the source/substrate and drain/substrate diffusions. These photocurrents have the same functional dependencies as those discussed previously in the bipolar diode chapter. They are reviewed briefly in the models presented here. In CMOS (complementary symmetry MOS) technology, both N-channel and P-channel, transistors are fabricated on the same silicon chip. As a result, three and four layer parasitic structures can be formed. These can act like transistors and SCR's when triggered by a photocurrent pulse. If an SCR structure is triggered, it can remain in a conducting state after the termination of the radiation pulse. This is the condition known as "latch up." It may result in catastrophic failure of the device. These parasitic bipolar structures must be included in any transient photoresponse analyses of CMOS devices.

Electrical overstress pulses may damage MOS devices either by burning out PN diodes associated with source and drain diffusions or by rupturing the gate dielectric. The SiO_2 gate dielectric is extremely thin (700 Å - 1000 Å) and is subject to breakdown at voltages in the range of 70 - 100 V. Thus, the gate voltage must be monitored in an electrical overstress analysis as well as the power dissipated in PN junctions.

This chapter includes a discussion of the following areas:

(1) First Order Drain Current Model

(2) Parasitic Elements

(3) Radiation Effects Model

(4) Second Order Effects Model

Section B presents a first order model of the drain current generator which simulates the three operating regions. The analyst who is interested in simple simulation of discrete MOS transistors will find this model to be generally adequate. Section C expands the model topology to include parasitic capacitances and gives their appropriate functional form. It also provides information for modeling multilayer, parasitic bipolar structures. Section D describes methods for modeling radiation effects including total dose, photocurrent, and electrical overstress environments. The final section includes model variations for simulating second order effects including weak inversion, channel length modulation, two-dimensional effects on threshold voltage, variable mobility, and temperature. These effects can be extremely important for the analyst modeling MOS devices found in high density MSI and LSI circuits.

B. FIRST ORDER DRAIN CURRENT MODEL

1. Description

The first order drain current model is based on a simple simulation of the drain-to-source current in the three regions of operation. The boundaries of the three operating regions are determined by the following inequalities:

(1) Cutoff $V_{GS} < V_T$

(2) Triode $V_{GS} \geq V_T$ and $V_{DS} < V_P$

(3) Saturation $V_{GS} \geq V_T$ and $V_{DS} \geq V_P$

This model considers the MOS transistor to be a bilateral device. Therefore, provisions must be included for altering the direction of current flow when the source and drain are interchanged. The key concepts to be mastered in applying this model are threshold voltage, pinchoff voltage, and the functional relationships among V_{GS}, V_{DS}, V_T, V_P, and I_D.

2. Advantages

The first order MOS model is usually easy to implement in computer analysis codes. Its parameters lend themselves to straightforward empirical measurement. It can be quite accurate for discrete MOS transistors.

3. Cautions

Logical FORTRAN statements have often been used to switch from one functional dependence to another in modeling cutoff, triode, and saturated operation. These statements can create discontinuities in the derivatives of the model equations. This can lead to numerical difficulties in the codes.

Some analytical switching functions which help to eliminate this problem are presented in this chapter. They should be given careful attention by analysts using SCEPTRE or similar codes.

The accuracy of the first order drain current model is usually adequate for discrete MOS transistors but is usually not adequate for MOS transistors found in integrated circuits.

4. Characteristics

a. Topology

The topologies shown in figure IV-2 are conventions for N-channel and P-channel devices. The gate-to-source, gate-to-drain, source-to-substrate, and drain-to-substrate capacitances have been shown in the topology. In this section, these parasitic capacitances will be considered to have constant values. A more detailed treatment of their functional form will be presented in the next section. The voltages across the capacitors are used to determine the operating condition of the transistor.

b. Typical Electrical Response

The drain current characteristics of N-channel and P-channel transistors as simulated by the first order model are shown as a function of gate voltage in figures IV-3 and IV-4, respectively. Figures IV-5 and IV-6 show the drain current as a function of gate voltage for N-channel and P-channel devices simulated by the first order model.

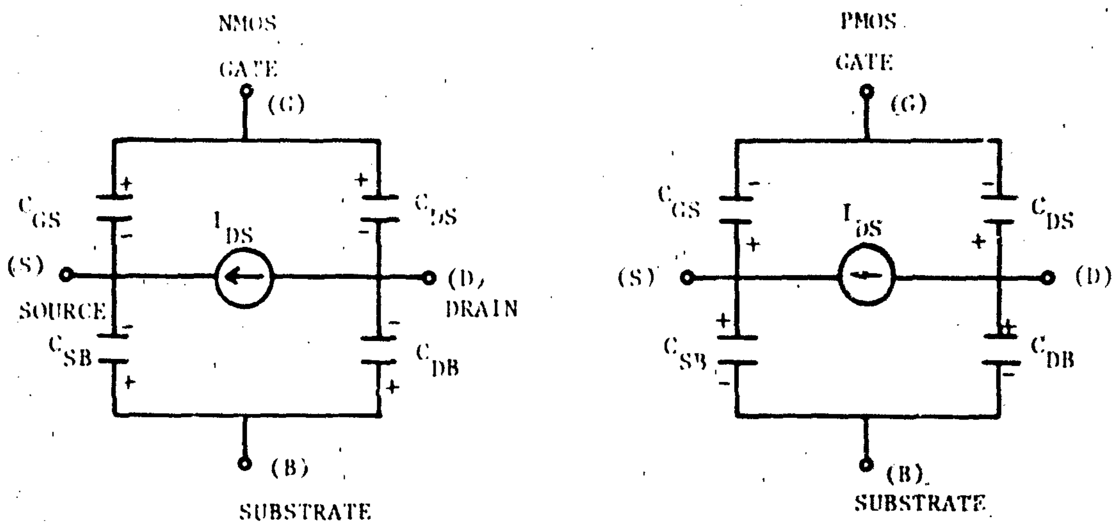


Figure IV-2. Topology Conventions for N-Channel and P-Channel Transistors

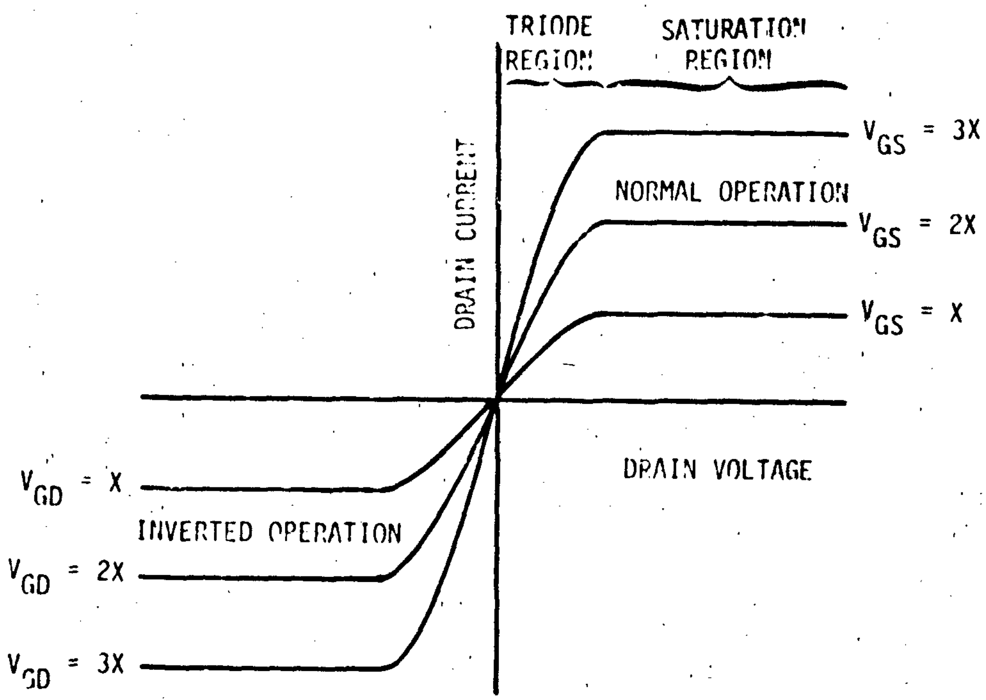


Figure IV-3. First Order Model Characteristics of Drain Current Versus Drain Voltage with Gate Voltage as a Parameter for an N-Channel Enhancement Mode Transistor

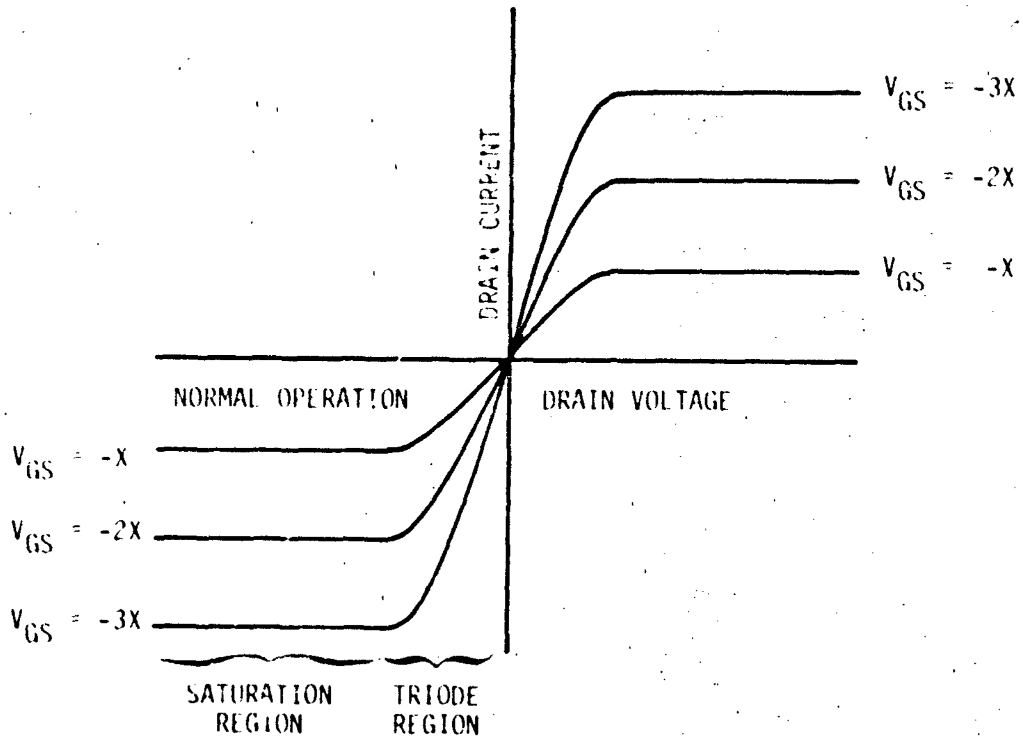


Figure IV-4. P-Channel Transistor Drain Current Characteristics

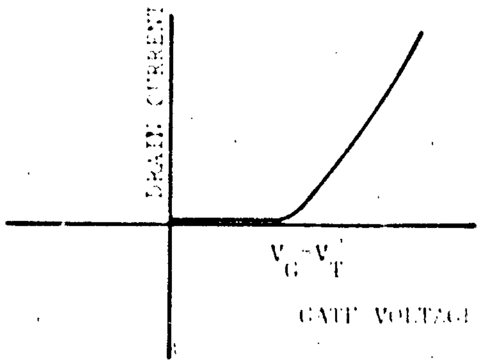


Figure IV-5. First Order Model Characteristic for Drain Current for an N-Channel Enhancement Mode Transistor

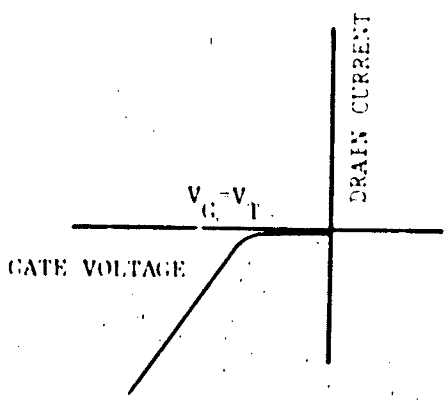


Figure IV-6. First Order Model Characteristic for Drain Current Versus Gate Voltage for a P-Channel Enhancement Mode Transistor

5. <u>Defining Equations</u>

If the source and substrate are always tied to the same potential (i.e., $V_{BS} = 0$), the first order dc characteristics of the MOS transistor can be described by the following equations for an N-channel device.

$$\text{NORMAL OPERATION} \begin{cases} V_{GS} < V_T \text{ or } V_{DS} = 0; \; I_{DS} = 0 \\ V_T \leq V_{GS} \text{ and } 0 < V_{DS} < V_P; \; I_{DS} = \beta\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2} V_{DS}^2\right] \\ V_T \leq V_{GS} \text{ and } 0 < V_P \leq V_{DS}; \; I_{DS} = (\frac{\beta}{2})(V_{GS} - V_T)^2 \end{cases}$$

$$\text{INVERTED OPERATION} \begin{cases} V_{GD} < V_T \text{ or } V_{DS} = 0; \; I_{DS} = 0 \\ V_T \leq V_{GD} \text{ and } -V_P < V_{DS} < 0; \; I_{DS} = -\beta\left[(V_{GD} - V_T)V_{DS} - \frac{1}{2} V_{DS}^2\right] \\ V_T \leq V_{GD} \text{ and } V_{DS} \leq -V_P < 0; \; I_{DS} = -(\frac{\beta}{2})(V_{GD} - V_T)^2 \end{cases}$$

For a P-channel device the equations become:

$$\text{NORMAL OPERATION} \begin{cases} V_{GS} > V_T \text{ or } V_{DS} = 0; \; I_{DS} = 0 \\ V_T \geq V_{GS} \text{ and } 0 > V_{DS} > V_P; \; I_{DS} = -\beta\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2} V_{DS}^2\right] \\ V_T \geq V_{GS} \text{ and } V_{DS} \leq V_p; \; I_{DS} = -(\frac{\beta}{2})(V_{GS} - V_T)^2 \end{cases}$$

$$\text{INVERTED OPERATION} \begin{cases} V_{GD} > V_T \text{ or } V_{DS} = 0; \; I_{DS} = 0 \\ V_T \geq V_{GD} \text{ and } 0 < V_{DS} < -V_p; \; I_{DS} = -\beta\left[(V_{GD} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2\right] \\ V_T \geq V_{GD} \text{ and } V_{DS} \geq -V_P; \; I_{DS} = -(\beta/2)(V_{GD} - V_T)^2 \end{cases}$$

6. <u>Parameter List</u>

$$\left.\begin{array}{lll} V_{GS} & = & \text{gate-to-source voltage} \\ V_{DS} & = & \text{drain-to-source voltage} \\ I_{DS} & = & \text{drain-to source current} \end{array}\right\} \text{Variables}$$

V_T = threshold voltage
V_P = pinchoff voltage $\left(V_{GS}-V_T\right)$ Model Parameters
β = transconductance factor

7. Parameterization

a. Threshold Voltage (V_T)

1) Description

The threshold voltage is the gate-to-source voltage required to form a channel and initiate conduction between drain and source. It is considered a constant in the first order approximation. Its value may be determined from measurements in either the triode or saturated regions of operation. In the triode region, the drain voltage is held at a low value (typically 10 - 50 mV) and the drain current is measured as a function of gate voltage. Figure IV-7 illustrates the experimental technique. Extrapolating the resulting plot to zero drain current yields the threshold voltage from the equation:

$$V_T = V_{GS} - \frac{1}{2} V_{DS}$$

For saturated region measurements, the gate and drain are tied together as shown in figure IV-8, and square root of the drain current is plotted as a function of gate voltage. At zero drain current, the value of applied gate voltage is equal to the threshold voltage as indicated by the equation:

$$V_{GS} - V_T = \sqrt{\frac{2I_{DS}}{\beta}} = 0$$

$$V_{GS} = V_T$$

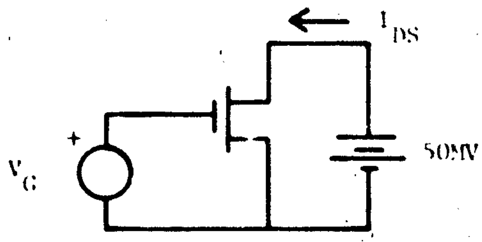


Figure IV-7. Triode Region Measurement for V_T

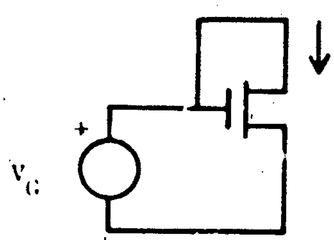


Figure IV-8. Saturated Region Measurement for V_T

2) Typical Value

Manufacturers can vary threshold voltage over a relatively wide range. This is especially true when both enhancement mode and depletion mode devices are considered. Table IV-1 gives reasonable signed values of threshold voltage for both N-channel and P-channel transistors. Voltages are referenced to the source.

TABLE IV-1. TYPICAL THRESHOLD VOLTAGES

	ENHANCEMENT MODE	DEPLETION MODE
N-channel	+1.5 V	-2.5 V
P-channel	-1.2 V	+2.5 V

3) Measurement Example

Figures IV-9 and IV-10 show the results of triode region measurements of threshold voltage of N-channel and P-channel transistors taken from an SSS 4007 integrated circuit. The N-channel devices show a threshold voltage of 1.65 volts, and the P-channel devices show a threshold voltage of 1.13 volts.

Figures IV-11 and IV-12 show the plot of the square root of the drain current of the same N- and P-channel transistor operating in the saturated region. The extrapolations to zero drain current show an N-channel threshold of 1.65 V and a P-channel threshold of 1.12 V. Note that both methods yield extremely close results.

Note that in both the triode region and saturated region measurements, the data begin to deviate from the expected behavior at higher gate voltages. This is due to variable mobility effects which are discussed in section E of this chapter.

b. Transconductance Factor (β)

1) Description

The transconductance factor can be thought of as the gain of the MOS transistor. It is determined by the mobility of the majority carriers in the channel, the oxide thickness, and the width to length ratio of the channel. In the first order model it is considered to be a constant. The data used to determine the threshold voltage in the previous subsection can also be used to determine the transconductance. For the triode region measurements, V_{DS} β is the slope of the plot of I_{DS} versus V_{GS}.

2) Typical Value

The transconductance factor is a function of the geometrical construction of the MOS transistor (i.e., it is directly proportional to the ratio of channel length to channel width). Therefore, suggesting a typical value could prove confusing.

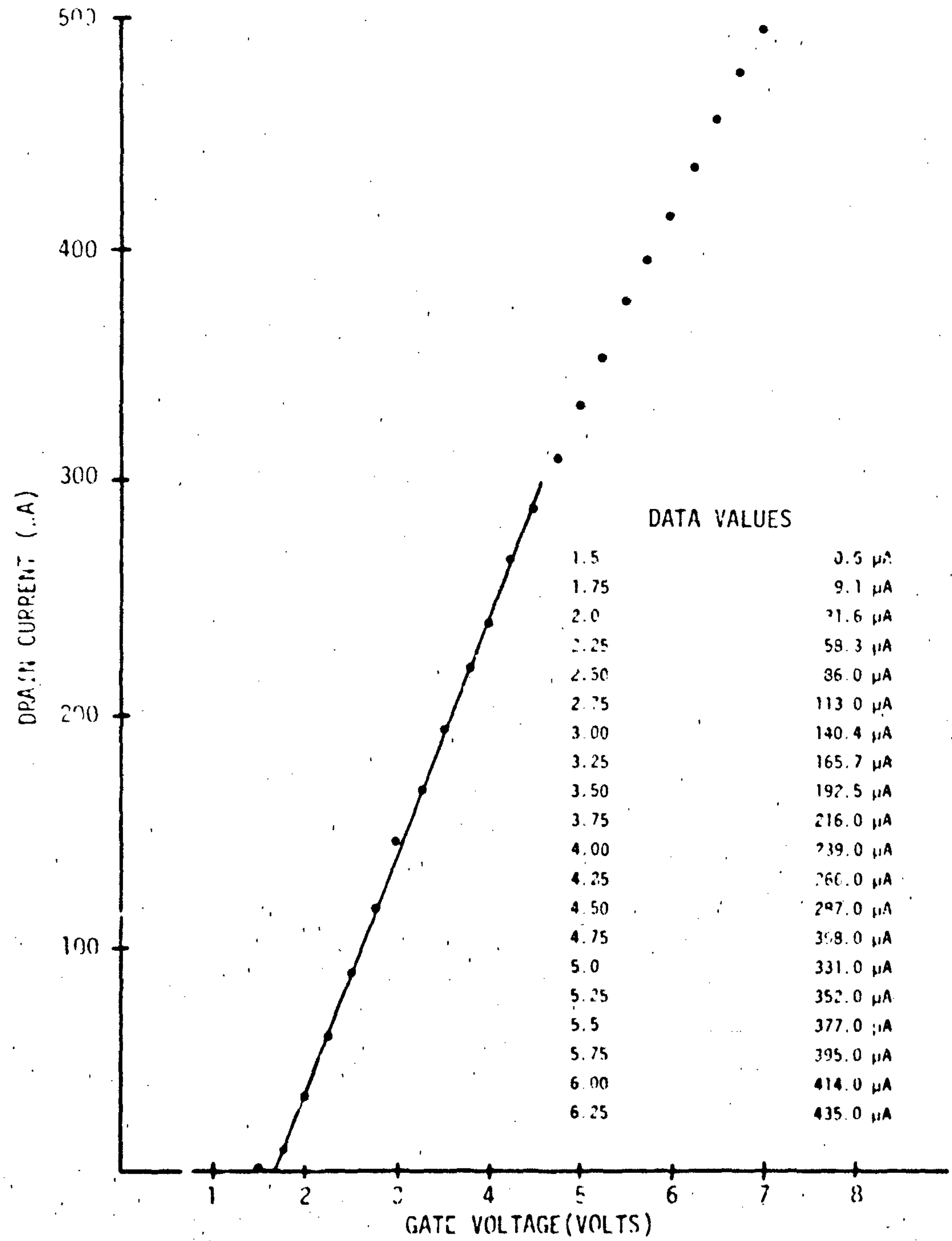


Figure IV-9. Threshold Voltage Determination from Triode Region Data for an N-Channel Enhancement Mode Transistor

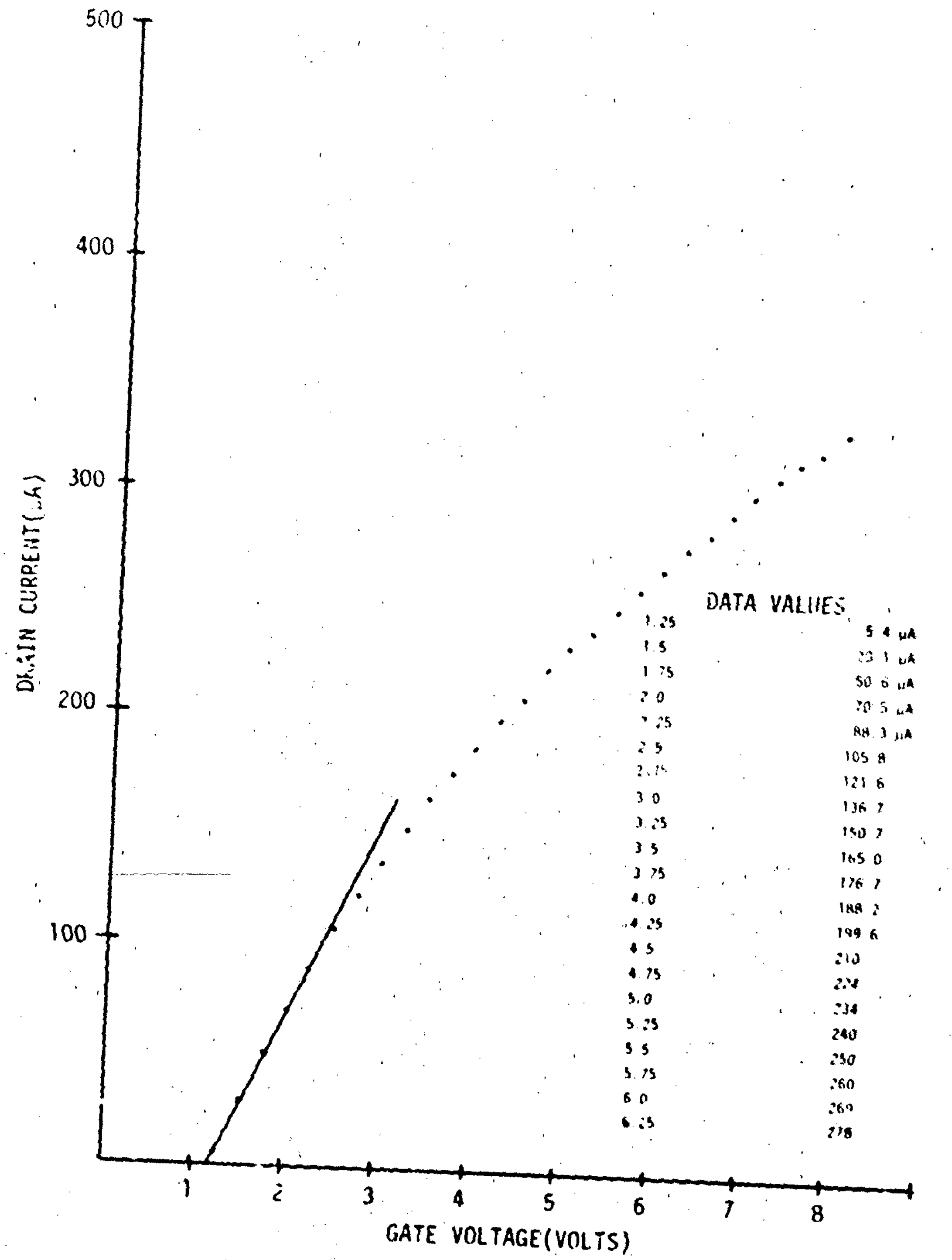


Figure IV-10. Threshold Voltage Determination from Triode Region Data for P-Channel Enhancement Mode Transistor

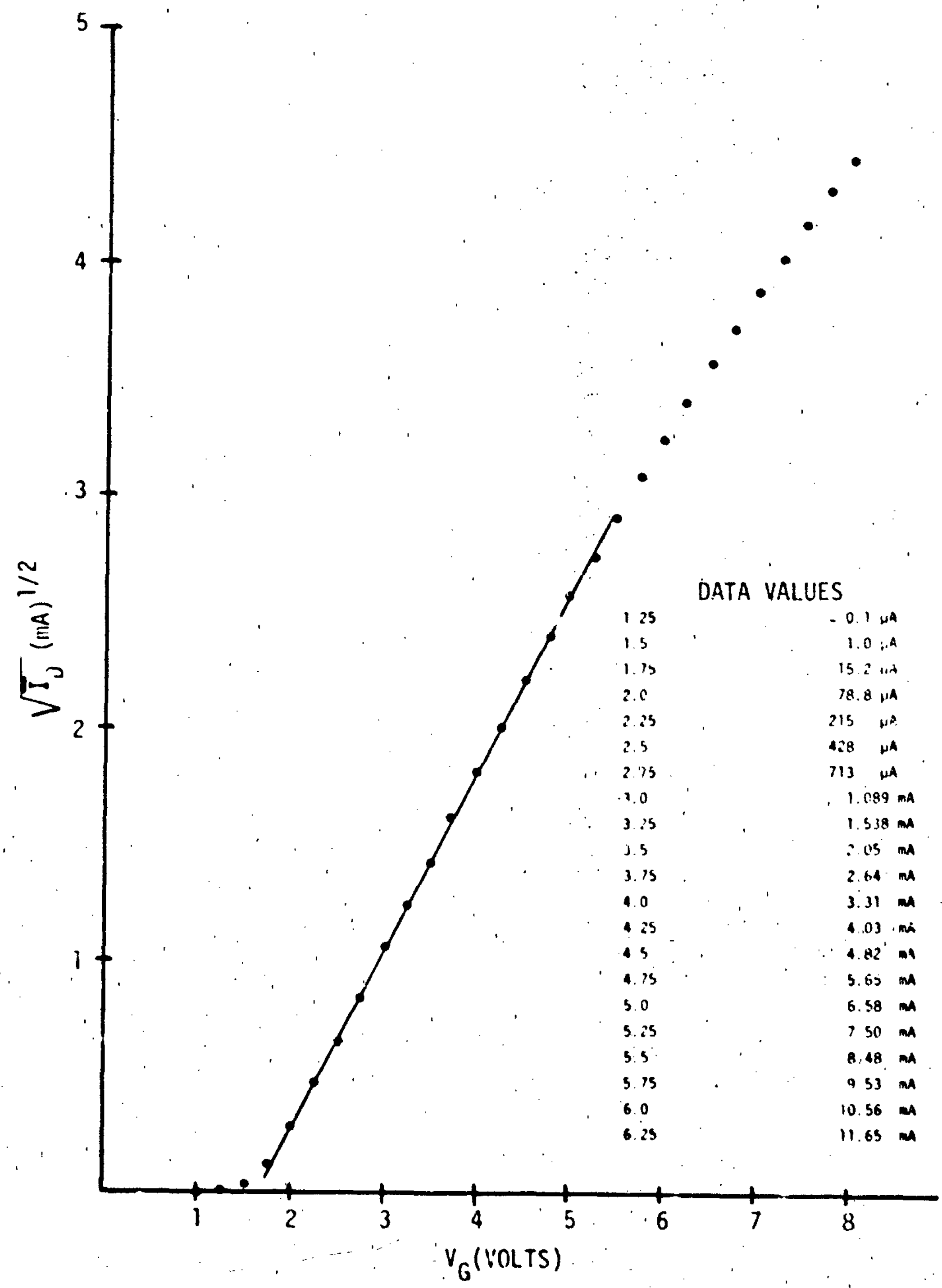


Figure IV-11. Threshold Voltage Determination from Saturated Region Data for an N-Channel Enhancement Mode Transistor

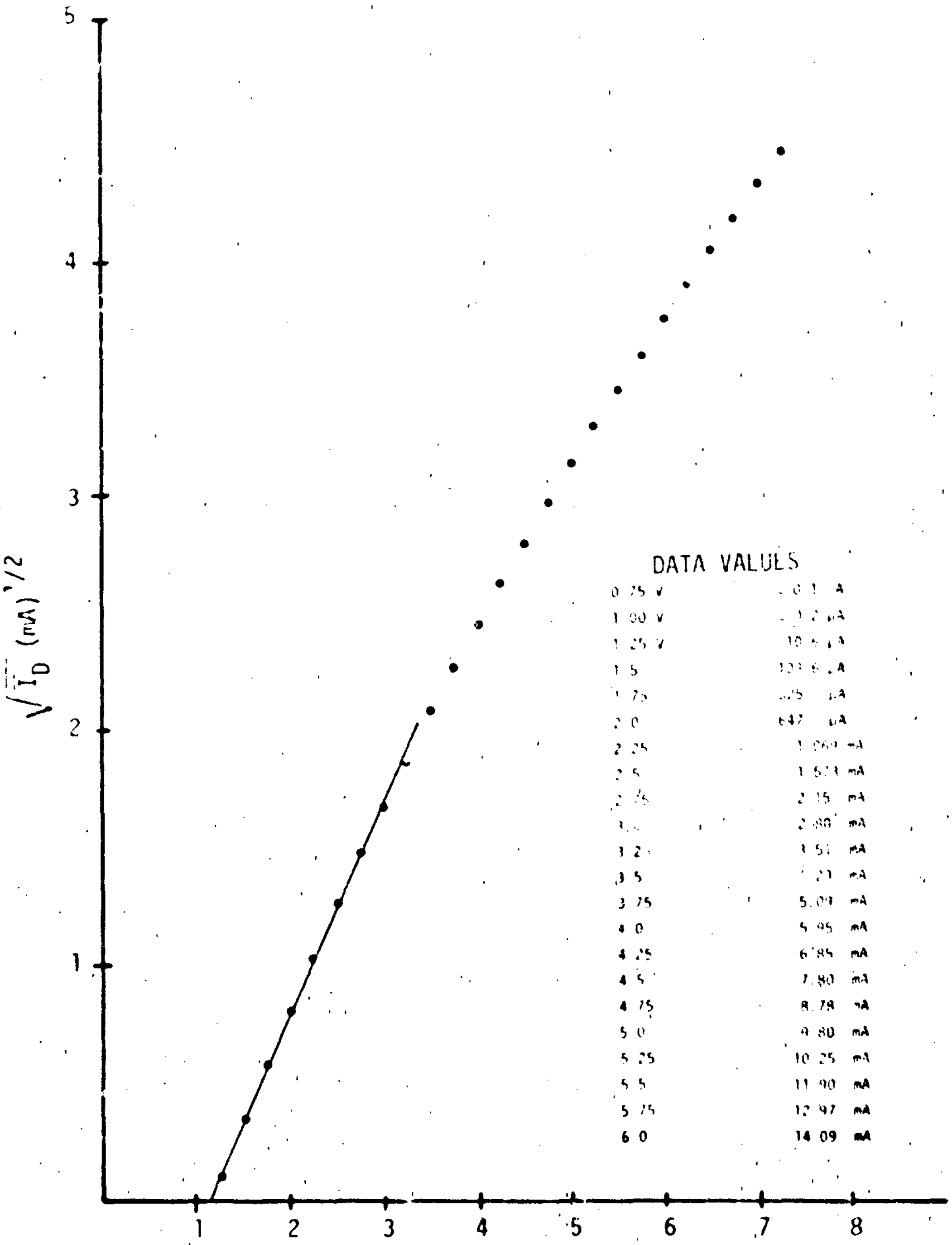


Figure IV-12. Threshold Voltage Determination from Saturated Region Data for P-Channel Enhancement Mode Transistor

3) Measurement Example

From the previous example of triode region data, the value of β for the N-channel transistor is 2.08 mA/V^2 and the value of β for the P-channel transistor is 1.61 mA/V^2.

c. Pinchoff Voltage

The pinchoff voltage marks the boundary between the triode and saturated region of operation. It may either be approximated by the expression $V_P = V_{GS} - V_T$ or measured as the locus of points satisfying the condition $\frac{\partial I_D}{\partial V_D} = 0$. The approximation is usually sufficient for the first order model and no attempt to directly parameterize V_P will be made here.

8. Code Implementation and Notes

Table IV-2 presents a listing of the parameters available for specifying a first order MOS transistor model in SCEPTRE, CIRCUS2, TRAC, NET-2, and SPICE2. Since SCEPTRE, CIRCUS2, and TRAC all require the MOS model to be included as a user-defined subroutine, only a single column has been assigned to them. A FORTRAN subroutine suitable for implementation with minor modifications in any of those three codes is given in figure IV-13. In figure IV-13, an analytical switching function of the form

$$f(X) = \frac{1}{1 + e^{S(R-X)}}$$

has been used, where:

X = independent variable
R = reference value at which switching is to take place
S = scale factor to determine the rate of transition (10 is a recommended value)
f(X) = value of the switch
= 1 for X > R
= 1/2 for X = R

TABLE IV-2. SCEPTRE, CIRCUS2, TRAC, NET-2, AND SPICE2 MODEL PARAMETERS REQUIRED FOR THE FIRST ORDER MOS MODEL

[illegible]				[illegible]				[illegible]			
CODE PARAMETER	DEFINITION	ENHANCEMENT NMOS VALUE	ENHANCEMENT PMOS VALUE	CODE PARAMETER	DEFINITION	ENHANCEMENT NMOS VALUE	ENHANCEMENT PMOS VALUE	CODE PARAMETER	DEFINITION	ENHANCEMENT NMOS VALUE	ENHANCEMENT PMOS VALUE
[illegible]	TYPE AND TRANSITION RATE FACTOR	[illegible]	[illegible]	[illegible]	POLARITY CONSTANT	[illegible]	[illegible]				
[illegible]	TRANSCONDUCTANCE FACTOR [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	INTRINSIC [illegible]	[illegible]	[illegible]
[illegible]	THRESHOLD VOLTAGE [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	THRESHOLD VOLTAGE	[illegible]	[illegible]
				[illegible]	[illegible]	[illegible]	[illegible]				
				[illegible]	[illegible]	[illegible]	[illegible]	GAMMA [illegible]	[illegible]	[illegible]	[illegible]
				[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
				[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
				[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
				[illegible]	[illegible]	[illegible]	[illegible]	LAMBDA	[illegible]	[illegible]	[illegible]

TABLE IV-2. SCEPTRE, CIRCUS2, TRAC, NET-2, AND SPICE2 MODEL PARAMETERS REQUIRED FOR THE FIRST ORDER MOS MODEL (Concluded)

SCEPTRE CIRCUS2 TRAC SUBROUTINE IMPLEMENTATION											
CODE PARAMETER	DEFINITION	ENHANCEMENT NMOS VALUE	ENHANCEMENT PMOS VALUE	CODE PARAMETER	DEFINITION	ENHANCEMENT NMOS VALUE	ENHANCEMENT PMOS VALUE	CODE PARAMETER	DEFINITION	ENHANCEMENT NMOS VALUE	ENHANCEMENT PMOS VALUE
				[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

*[illegible]

**[illegible]

***[illegible]

```
      FUNCTION FMOS(VG,VD,VBS,B,VT,S)
      FSWITCH(X,R,S)=1./(1.+EXP(AMIN1(100.,S*(R-X))))
      FA(VDA,VDE,VGE,B,VT)=B*SIGN(ABS(VDE)*ABS(VGE-VT-VDE/2.),VDA)
      FP(VGE,VT)=VGE-VT
      IF(VD*S.LT.0)GO TO 5
      VDE=VD
      VGE=VG
      VBE=VBS
      GO TO 10
    5 VDE=-VD
      VGE=VG-VD
      VBE=VBS-VD
   10 CONTINUE
      VMAX = 1.E3
      IF(ABS(VGE).GT.VMAX) GO TO 50
      IF(ABS(VDE).GT.VMAX) GO TO 50
      IF(ABS(VBE).GT.VMAX) GO TO 50
      AU=FA(VD,VDE,VGE,B,VT)
      VP=FP(VGE,VT)
      ADSS=FA(VD,VP,VGE,B,VT)
      F1=FSWITCH(VGE,VT,S)
      F2=FSWITCH(VDE,VP,S)
      FMOS=F1*F2*ADSS+F1*(1.-F2)*AU
      RETURN
   50 FMOS = 0.
      RETURN
      END
```

Figure IV-13. FORTRAN Subroutine Implementation of the First Order Drain Current Model for Incorporation into SCEPTRE, CIRCUS2, and TRAC

In using the switching function with the MOS model, a value of S equal to 10 was found to represent a good compromise between switching speed and computational efficiency.

To utilize the switching function with expressions for drain current for P- and N-channel devices in an MOS model, the boundaries of the regions of operation must be defined. Once the boundaries are defined, the appropriate switching functions can be derived to provide smooth transitions (continuous first derivatives) between regions. The operating regions to be considered include cutoff, normal and inverted triode operation, and normal and inverted saturation. Therefore, switches must be included for the following transitions:

(1) Transitions from cutoff to either normal or inverted triode operation.

(2) Transitions from normal triode operation to normal saturated operation.

(3) Transitions from inverted triode operation to inverted saturated operation.

Table IV-3 presents a set of switching functions which are adequate to model the required transitions. For the model, cutoff is defined as the region where either the gate-to-drain or gate-to-source voltage is too small to support conduction ($V_{GS} < V_T$, $V_{DS} = 0$). Two switches are required to bound cutoff. One compares gate-to-source voltage (V_{GS}) with V_T. The other compares gate-to-drain voltage (V_{GD}) with V_T. The switches (f_1, f_3) are defined such that f_1 is "true" for V_G greater than V_T. The switch f_3 is "true" for V_{GD} greater than V_T.

Saturated operation is defined as the region where drain-to-source or source-to-drain voltage exceeds pinchoff (V_P). Two switches were defined to determine transitions between triode and saturated operation. Switch f_2 is defined as "true" for the drain-to-source voltage (V_{DS}) greater than V_P. Switch f_4 is defined as "true" for source-to-drain voltage (V_{SD}) greater than V_P.

Since the signs of the quantities V_{GS}, V_{DS}, V_P, and V_{GD} are different for N- and P-channel devices, the inequality changes required

to retain the correct sign conventions for enhancement mode devices are given in table IV-3.

TABLE IV-3. ANALYTICAL SWITCH DEFINITIONS

SWITCH	N-CHANNEL	P-CHANNEL
f_1 = TRUE = 1	$V_{GS} > V_T$	$V_{GS} < V_T$
f_2 = TRUE = 1	$V_{DS} > V_P$	$V_{DS} < V_P$
f_3 = TRUE = 1	$V_{GD} = V_{GS} - V_{DS} > V_T$	$V_{GD} = V_{GS} - V_{DS} < V_T$
f_4 = TRUE = 1	$V_{SD} > V_P$	$V_{SD} < V_P$

The cutoff region is not specifically included above. However, cutoff is automatically defined by a "false" condition on each of the switches f_1, f_2, f_3, and f_4.

The switches f_3 and f_4 actually perform the same function as f_1 and f_2, respectively. Thus, they can be eliminated from the model by the appropriate redefinition of the source and drain terminals. In the implementation of the model, that redefinition is made and only two switching functions are required as will be shown later. The use of the analytical switching function will usually produce a more computationally stable model than will the use of a logical switching function having discontinous first derivatives.

The NET-2 MOS model has been built into the code and may be accessed through a model call and an appropriate parameter list in the device parameter library. The NET-2 model allows the user a great deal of flexibility in the selection of model equation coefficients. This is especially useful when there are sufficient experimental data available to allow curve fitting of the equations to measured values of drain current as a function of gate-to-source and drain-to-source voltage. The relationship of the NET-2 model parameters to the usual MOS characteristic equations is demonstrated below.

Triode Region:

$$I_{DS} = \beta \left[V_{DS} (V_{GS} - V_T) - \frac{1}{2} V_{DS}^2\right] = V_{DS}\left[-\beta V_T + \beta V_{GS} - \frac{1}{2} \beta V_{DS}\right]$$

NET-2 Model:

$$I_{DS} = V_{DS} \left[A_1 + A_4 V_{GS} + A_3 V_{DS} + A_2 \sqrt{V_{DS}} + A_5 V_{GS}^2\right]$$

Saturated Region:

$$I_{DS} = \beta \left[V_P (V_{GS} - V_T) - \frac{1}{2} V_P^2\right] = V_P \left(-\beta V_T + \beta V_{GS} - \frac{1}{2} \beta V_P\right)$$

NET-2 Model:

$$I_{DS} = (V_{DS} - V_P)(K_1 + K_2 V_{GS} + K_3 V_{GS}^2)$$

$$+ V_P \left(A_1 + A_4 V_{GS} + A_3 V_P + A_2 \sqrt{V_P} + A_5 V_{GS}^2\right)$$

For the first order model, parameters A_1, A_4, and A_3 are required. The remaining parameters are used to include second order effects which will be discussed in subsequent sections.

The SPICE2 MOS model is an extremely flexible built-in model. It was designed to be used in all phases of MOS integrated circuit design. Therefore, it can be parameterized from either measured electrical data or device physics data determined from fabrication procedures. The parameter values given in table IV-2 are based on the assumption that only measured electrical data will be used. If the first order SPICE2 model is desired, the analyst should be careful not to specify values for substrate doping concentration and should insure that all other values marked with an asterisk (*) are set to precisely the values indicated in table IV-2. Failure to do so will result in inconsistencies within the model and inaccurate results.

9. Computer Example

Listings of SCEPTRE programs used to produce "curve tracer" characteristics of an N-channel and P-channel transistor are presented in figures IV-14 and IV-15. Note that the zero valued current sources JB and JG are used to detect the gate and substrate bias with respect to the source. The results of exercising these programs for the measured parameters from the S^3 4007 are shown in figures IV-16 and IV-17. The figures display the drain current as a function of drain voltage for a variety of gate voltages. The listings of MEI-2 programs used to produce turn-on characteristic runs (I_D versus V_{GS}) for N-channel and P-channel devices are shown in figures IV-18 and IV-19. The results of the program solutions for measured parameters from the S^3 4007 are shown in figures IV-20 and IV-21.

C. PARASITIC INCLUSIVE MOS MODELS

1. Description

Parasitic elements associated with MOS transistors occur because of interactions between the gate electrode and the semiconductor material and because of PN junction effects resulting from source and drain diffusions into the semiconductor. These parasitics have a significant effect on the operation of MOS circuits. Accurate prediction of operating speed cannot be made without appending appropriate capacitive and resistive elements to the model. Parasitic diodes and other bipolar structures may be important for predicting power consumption and information storage time properties for MOS integrated circuits, and they are essential to predictions of transient radiation effects (see section D).

2. Advantages

The operation of digital MOS integrated circuits can generally be understood in terms of the charging and discharging of gate capacitors by nonlinear, voltage controlled, current sources. A reasonable estimate of capacitance can be coupled with basic drain current models to produce

Figure IV-14 SCEPTRE Listing of Curve Tracer Circuit for Displaying N-Channel Characteristics for the First Order Model

```
MODEL DESCRIPTION
MODEL NMOS (D-S-G-B)
    UNITS = R=OHM,V=VOLT,I=AMP,T=SEC,L=HENRY,C=FARAD
        ELEMENTS
            RD,D -DD = 1.00
            RS,SS -S = 1.00
            CGD,G -DD = 1.00E-12
            CGS,G -SS = 1.00E-12
            CBD,BD -DD = 5.00E-12
            CBS,BS -SS = 5.00E-12
            CBG,G -B = 1.00E-12
            JB,BS -SS = 0.
            J[illegible] -SS = 0.
            JD,[illegible] -SS = FMOS(VJG,VJD,VJB,2.0E-3,1.65,10.)
            JBD,BD -DD = DIODE Q(1.00E-11,38.5)
            JBS,BS -SS = DIODE Q(1.00E-11,38.5)
            J1,DD -B = 0.
            J2,SS -B = 0.
            R[illegible] -DD = 1.E12
            R[illegible],BS -SS = 1.E12
            R[illegible] -B = 5.
            R[illegible] -BS = 5.
        DEFINED PARAMETERS
            PEC = Q IV(VJ1,PE1)
            PES = Q IV(VJ2,PE1)
            PE1 = 100.
        FUNCTIONS
            Q IV(V,VMAX) = (ABS(V/VMAX))

CIRCUIT DESCRIPTION
CURVE TRACER [illegible]
    UNITS = [illegible] I=AMP,T=SEC,L=HENRY,C=FARAD
    ELEMENTS
        [illegible]  [illegible](TIME,[illegible])
        [illegible]  [illegible](TIME,[illegible],0.,[illegible],0.,18.)
            [illegible]
            [illegible]
        [illegible]
    DEFINED PARAMETERS
        [illegible] = 1.E-4
        [illegible]
    OUTPUTS
        [illegible]
            [illegible]
        V[illegible],PLOT
        [illegible],PLOT
        J[illegible],PLOT
    RUN CONTROLS
        [illegible] INITIAL CONDITIONS
        INTEGRATION ROUTINE = IMPLICIT
            MINIMUM STEP SIZE = 1.E-40
        MAXIMUM STEP SIZE = [illegible]
        MAXIMUM ITERATION PASSES = [illegible]
        [illegible]
        STOP TIME = [illegible]
            [illegible]
            [illegible]
END
```

Figure IV-14. SCEPTRE Listing of Curve Tracer Circuit for Displaying N-Channel Drain Characteristics for the First Order Model (Concluded)

```
SUBPROGRAM

      FUNCTION FMOS(VG,VD,VBS,HO,OH,C,E,U,G,VF,PHI,FEEF,S)
      FSWTCH(X,R,S) = 1./(1.+EXP(AMIN1(100.,S*(R-X))))
      FA(VDA,VDE,VGE,H,VX,APHI,AFE)= H*SIGN(ABS(VDE)*ABS(VGE-VX-VDE/2.)
     1  -2. APHI*((ABS(VDE)+AFE)**1.5-AFE**1.5)/3.,VDA)
      FP  (  VGE,ADE ,HEU,VX,PHI,APHI,VHE) =       VGE- ADE/HEU -VX +
     1 PHI*(APHI/2. -SQRT(ABS(VGE-ADE /HEU -VF-VHE+PHI*APHI/4.)))
      APHI = ABS(PHI)
      VX = VF + FEEF
      IF(VD*S.LT.0) GO TO 5
      VDE = VD
      VGE = VG
      VHE = VBS
      GO TO 10
    5 VDE = -VD
      VGE = VG - VD
      VHE = VBS - VD
   10 CONTINUE
      VMAX = 1.E3
      IF(ABS(VGE).GT.VMAX)  GO TO 50
      IF(ABS(VDE).GT.VMAX)  GO TO 50
      IF(ABS(VHE).GT.VMAX)  GO TO 50
      AFE = ABS(FEEF-VHE)
      VT = VX + PHI*SQRT(AFE)
      H = HO/(1.+OH*ABS(VGE-VT))
      HEU = H*E*U
      AU = FA(VD,VDE,VGE,H,VX,APHI,AFE)
   30 VP = FP    (VGE,0.,HEU,VX,PHI,APHI,VHE)
   31 ADSS =       FA(VD,VP,VGE,H,VX,APHI,AFE)
      ADE = SIGN(ADSS,VP)
   32 VP = FP     (VGE,ADE ,HEU,VX,PHI,APHI,VHE)
   33 ADSS = FA(VD,VP,VGE,H,VX,APHI,AFE)
      A = U*(1.+G*ABS(ADSS)) -E/C
      AA = SIGN(AMAX1(1.E-100,ABS(A)),A)
      P = (ABS(VDE-VP)+E*U)/C
      TEMP = P**2 +4.*AA*U*ABS(VDE-VP)/C
      IF (TEMP.LT.0.) PRINT 100
      DU = (-P + SQRT(ABS(TEMP)))/(2.*AA)
      F1 = FSWTCH(VGE,VT,S)
      F2 = FSWTCH(VDE,VP,S)
      FMOS = F1*F2*ADSS*U/(U-DU) +F1*(1.-F2)*AU
      RETURN
   50 FMOS = 0.
      RETURN
  100 FORMAT(5X,*NEGATIVE VALUE UNDER RADICAL IN DELTA U EQUATION *
     1  *CAUSED BY PARAMETER ERRORS IN FMOS REFERENCE.*)
      END

      FUNCTION FSTEP(T,TP,TO,TUP,VO,DV)
C        RESTRICTIONS
C        TP CAN NOT BE 0.
C        TUP MUST BE LESS THAN BUT NOT EQUAL TO 1.
      IF(T.GT.TO) GO TO 5
      FSTEP = VO
      IF(T.LT.TO/2.) FSTEP = VO*T*2./TO
      RETURN
5     TN = (T-TO)/TP
      N = 0
6     IF(TN.LT.1.) GO TO 10
      TN = TN - 1.
      N = N + 1
      GO TO 6
10    FSTEP = VO+N*DV
      IF(TN.GE.TUP) FSTEP = VO+DV*(N+(TN-TUP)/(1.-TUP))
      RETURN
      END
```

Figure IV-15. SCEPTRE Listing of Curve Tracer Circuit for Displaying P-Channel Drain Characteristic for First Order Model

```
MODEL DESCRIPTION
    MODEL PMOS (G-S-D-B)
    UNITS = R=OHM,V=VOLT,I=AMP,T=SEC,L=HENRY,C=FARAD
        ELEMENTS
            RD,L -DL = 1.00
            RS,SS -S = 1.00
            CGD,G -GD = 1.00E-12
            CGS,G -SS = 1.00E-12
            CBD,BD -DL =5.00E-12
            CBS,BS -SS = 5.00E-12
            CBG,G -B = 1.00E-12
            JB,BS -SS = 0.
            JG,G -SS = 0.
            JD,DL -SS = PMOS(VGS,VDS,VBS,2.61E-3,-1.13,-10.)
            JSD,DL -BD = DIODE Q(1.00E-11,38.5)
            JSS,SS -BS = DIODE Q(1.00E-11,38.5)
            J1,DL -G = 0.
            J2,SS -G = 0.
            R3,BD -DL = 1.E12
            R4,BS -SS = 1.E12
            R5,B -BD = 5.
            R6,B -BS = 5.
        DEFINED PARAMETERS
            PFD = Q IV(V01,PF1)
            PFS = Q IV(V02,PF1)
            PF1 = 100.
        FUNCTIONS
            Q IV(V,VMAX) = (ABS(V/VMAX))

CIRCUIT DESCRIPTION
CURVE TRACER PROGRAM
    UNITS = R=OHM,V=VOLT,I=AMP,T=SEC,L=HENRY,C=FARAD
    ELEMENTS
        EG,S-G=     STEP(TIME,PTP,PTO,.5,-2.0,-2.0)
        ED,S-DR=  SWEEP(TIME,PTP,PTO,.5,0,1.0,0,-10.)
            RD,DR-D = 50.
            RG,GR-G =   1.E3
        T1,G-S-D-S = MODEL PMOS
    DEFINED PARAMETERS
        PTP = 1.E-3
        PTO = 0.
    OUTPUTS
        IRDX1,PLOT(ED)
            IRDX1,PLOT
        VDGX1,PLOT
        ED,PLOT
        JDX1,PLOT
    RUN CONTROLS
        RUN INITIAL CONDITIONS
        INTEGRATION ROUTINE   IMPLICIT
            MINIMUM STEP SIZE = 1.E-10
        MAXIMUM STEP SIZE = 5.E-6
        MAXIMUM INTEGRATION PASSES = 2.E5
        NO OVERFLOW PRINTOUT
        STOP TIME =  5.E-3
            TERMINATE IF(PFSX1.GT.1.)
            TERMINATE IF(PFDX1.GT.1.)
END
```

Figure IV-15. SCEPTRE Listing of Curve Tracer Circuit for Displaying P-Channel Drain Characteristic for First Order Model (Concluded)

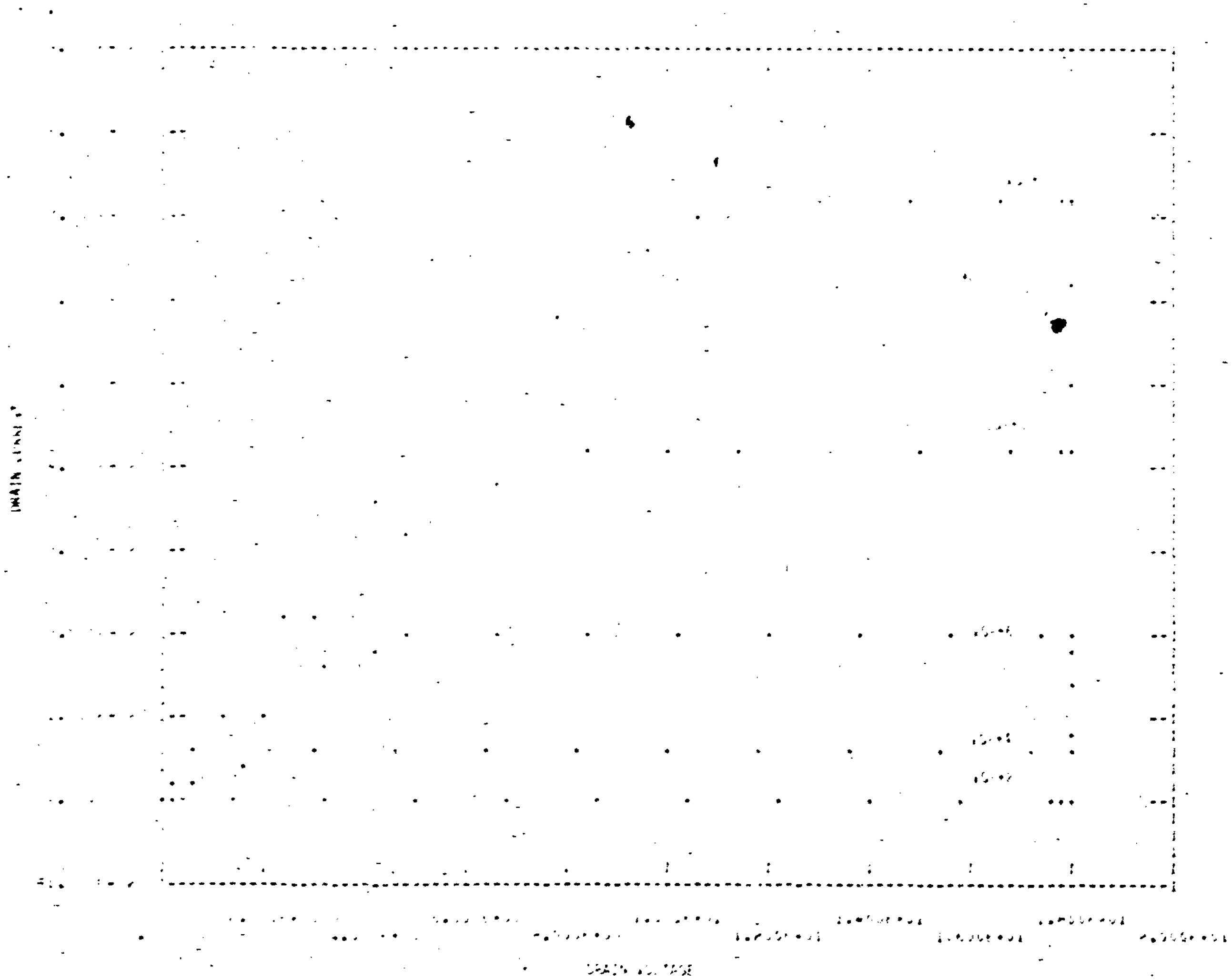


Figure IV-16. SCEPTRE First Order Model . ain Characteristics for an N-Channel MOS Transistor

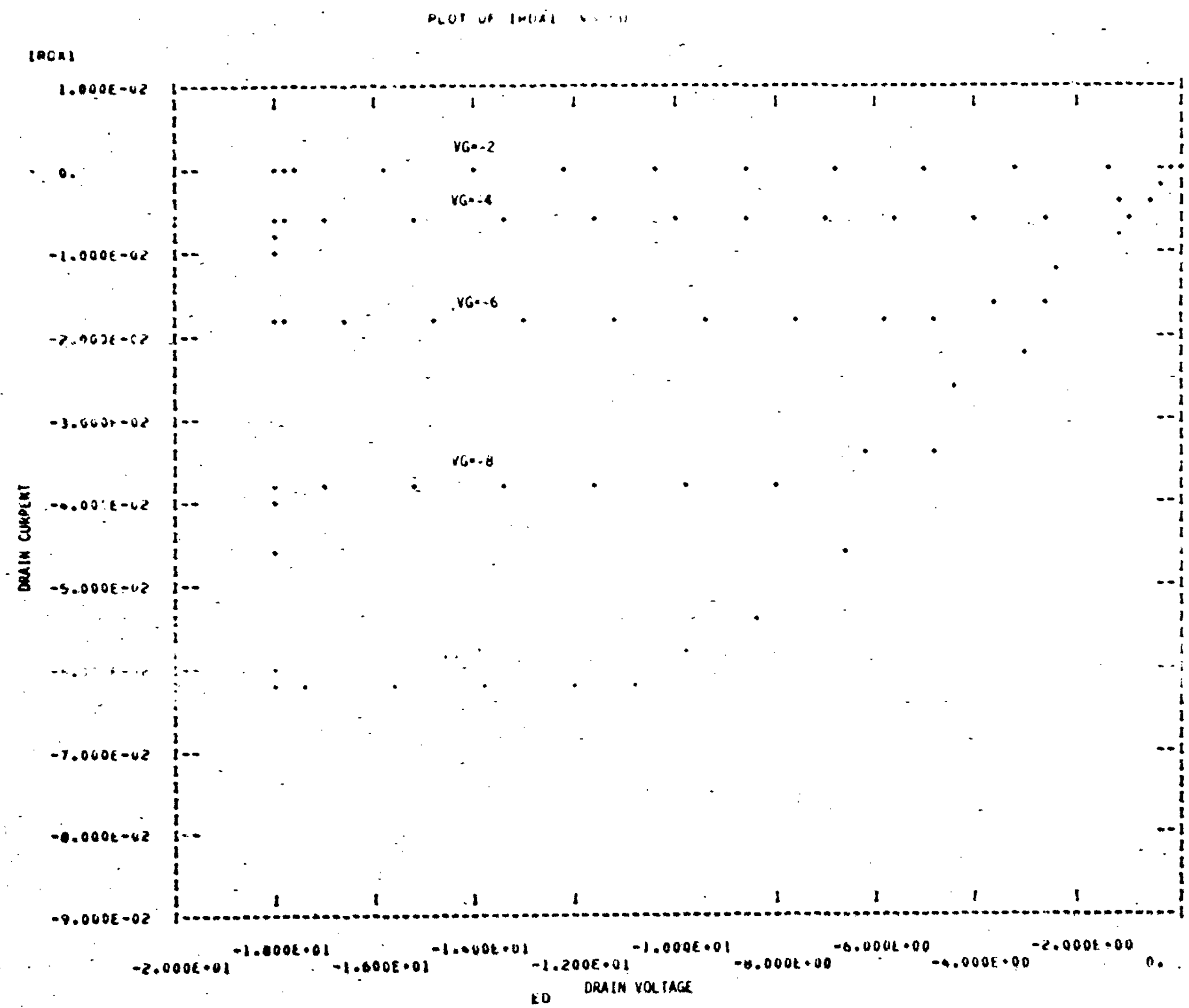


Figure IV-17. SCEPTRE First Order Model Drain Characteristics for P-Channel Transistor

```
NET-2 NETWORK ANALYSIS PROGRAM    RELEASE 9
05/03/74     09.29.03.

        000000000111111111122222222223333333333444444444455555555556666666666777777777778
        12345678901234567890123456789012345678901234567890123456789012345678901234567890
        * GATE CHARACTERISTICS OF NET2 FIRST ORDER MODEL--N-CHANNEL/ENHANCEMENT
        LIBRARY
             MEET NMOS 5
                  A1 -1.72
                  A2 0.
                  A3 -.52
                  A4 1.04
                  A5 0.
                  C71 5.
                  C02 5.
                  CGD1 1.
                  CGS1 1.
                  IS1 1.0E-9
                  IS2 1.EE-9
                  K1 [illegible].
                  K2 [illegible].
                  K3 [illegible].
                  N1 .5
                  N2 .5
                  [illegible] .1
                  T 1000.
                  TH1 20.
                  TH2 30.
                  VB1 1.
                  VB2 1.
                  VGO1 1.
                  VGO2 1.
                  VZ1 1.
                  VZ2 1.
                  R1 .1
                  R2 .1
        MEET1 G 1 2 0 NMOS
        V1 1 0 P1
        V2 2 0 P2
        P1 0
        P2 0
        STATE1
             P1 C (20) 2 [illegible] 15
             *P2 0 (7) 1.
             PLOT I(V2) VS N(2)
             PLOT I(V2) VS N(1)
        END
```

Figure IV-18. NET-2 Listing for Curve Tracer Circuit Displaying N-Channel Turn on Characteristics for the First Order Model

```
NET-2 NETWORK ANALYSIS PROGRAM    RELEASE 9
 05/03/78      09.30.57.

        00000000011111111112222222222333333333344444444445555555555666666666677777777778
        12345678901234567890123456789012345678901234567890123456789012345678901234567890
        * GATE CHARACTERISTICS OF NET2 FIRST ORDER MODEL--P-CHANNEL/ENHANCEMENT
        LIBRARY
                MFET PMOS 5
                        A1 -.92
                        A2 0.
                        A3 -.40
                        A4 .01
                        A5 0.
                        CG1 5.
                        CG2 5.
                        CGS1 1.
                        CDS1 1.
                        IS1 1.0E-9
                        IS2 1.0E-9
                        R1 0.
                        R2 0.
                        R3 0.
                        N1 .5
                        N2 .5
                        S -1
                        T 150.
                        TH1 30.
                        TH2 30.
                        VM1 1.
                        VM2 1.
                        VG1 1.
                        VG2 1.
                        VZ1 1.
                        VZ2 1.
                        W1 .1
                        W2 .1
        MFET1 0 1 2 0 PMOS
        V1 1 0 R1
        V2 2 0 R2
        R1 0
        R2 0
        STATE1
                R1 0 (20) -2 (25) -15
                *R2 0 (7) -14
                PLOT I(V2) VS R(2)
                PLOT I(V2) VS R(1)
        END
```

Figure IV-19. NET-2 Listing for Curve Tracer Circuit Displaying P-Channel Turn on Characteristics for the First Order Model

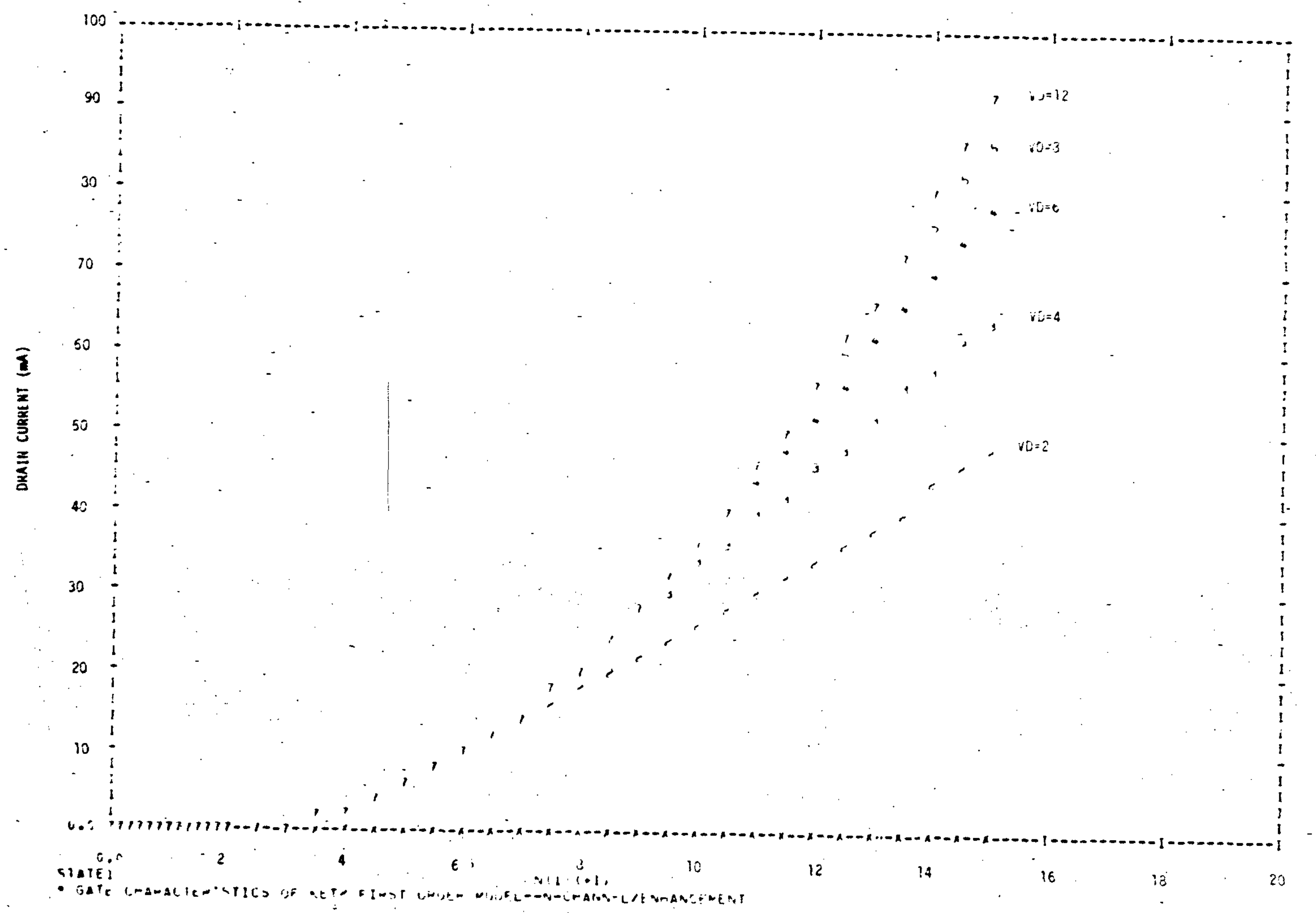


Figure IV-20. NET-2 First Order Model Turn on Characteristics for an N-Channel MOS Transistor

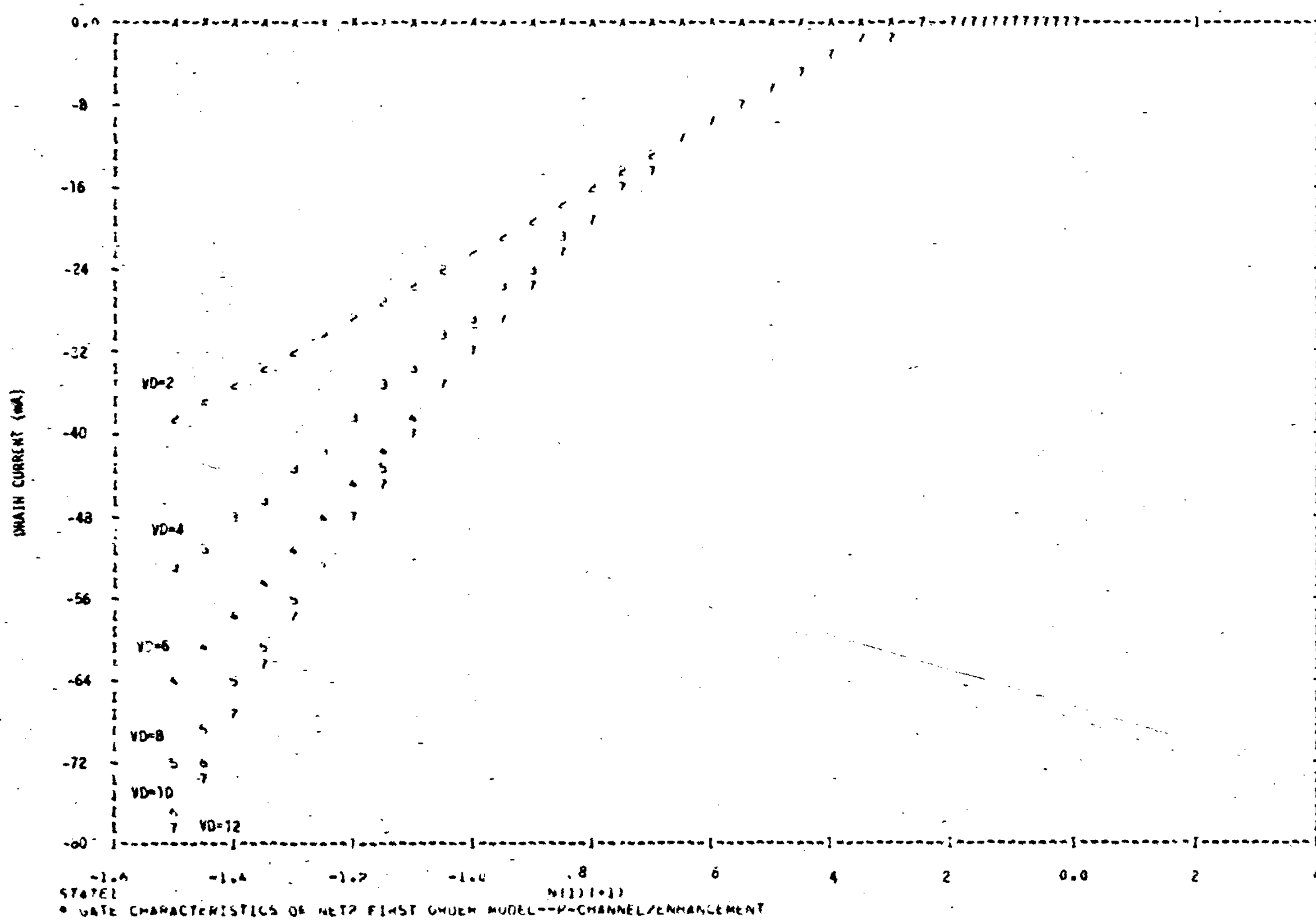


Figure IV-21. NET-2 First Order Model Turn on Characteristics for a P-Channel MOS Transistor

very acceptable predictions of propagation delay, risetime, and falltime. The ability to directly scale both capacitance and current capability of MOS devices with transistor geometry often makes the analysis task much simpler for MOS circuits than for bipolar circuits.

3. Cautions

An MOS model which contains full parasitics requires a large number of elements. For example, a complete model of a CMOS inverter containing an N-channel and P-channel transistor with full parasitics can require 37 individual resistors, capacitors, and current sources. The analyst must use his judgment in determining which of these elements are really necessary for an accurate solution. The parasitic elements described in the following material can be appended to either the first order model discussed in section B or the second order model discussed in section D.

4. Characteristics

A CMOS integrated circuit structure as shown in the cross section of figure IV-22 will be used to illustrate the relationship of the parasitic elements to the MOS drain current model. In figure IV-23, the CMOS structure has been redrawn schematically in terms of active and passive circuit elements. Figure IV-24 shows the MOS model topologies for the N-channel and P-channel transistors with the required parasitic elements. The N-channel transistor is shown in the top half of figure IV-24. Its drain current is modeled by the current source JC2. The P-channel device is in the lower half of the figure. Its drain current is modeled by the JC9 current source. For each MOS transistor, three capacitors are associated with the gate/semiconductor interactions. These are CGNS, CGND, and CGNB for the N-channel and CGPS, CGPD, and CGPB for the P-channel. Each of these capacitors has a fixed component and a voltage variable component. Two capacitors for each transistor are associated with the source and drain diffusions. These are CNS and CND for the N-channel and CPS and CPD for the P-channel. These represent a combination of the depletion region capacitance and diffusion capacitance

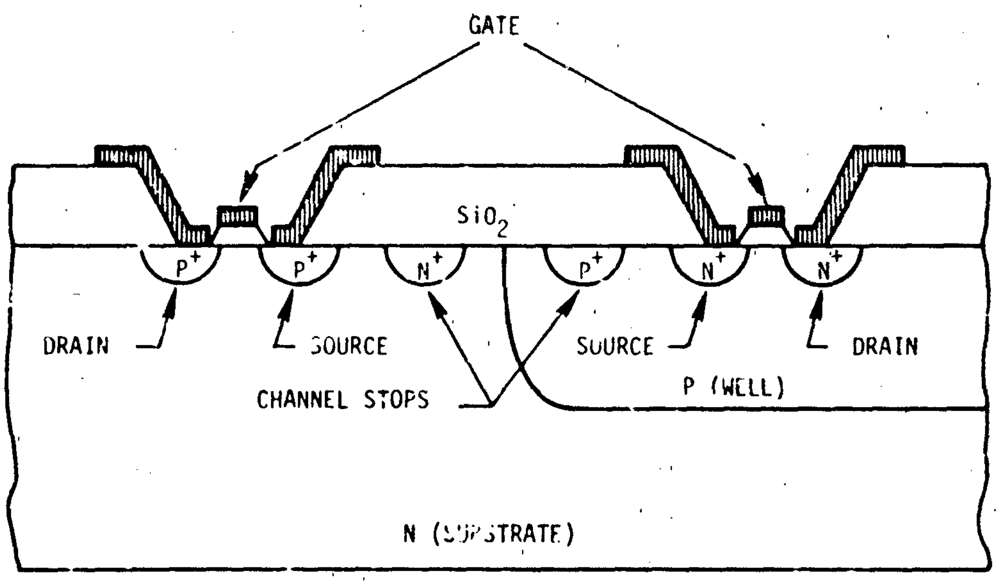


Figure IV-22. CMOS Inverter Cross Section

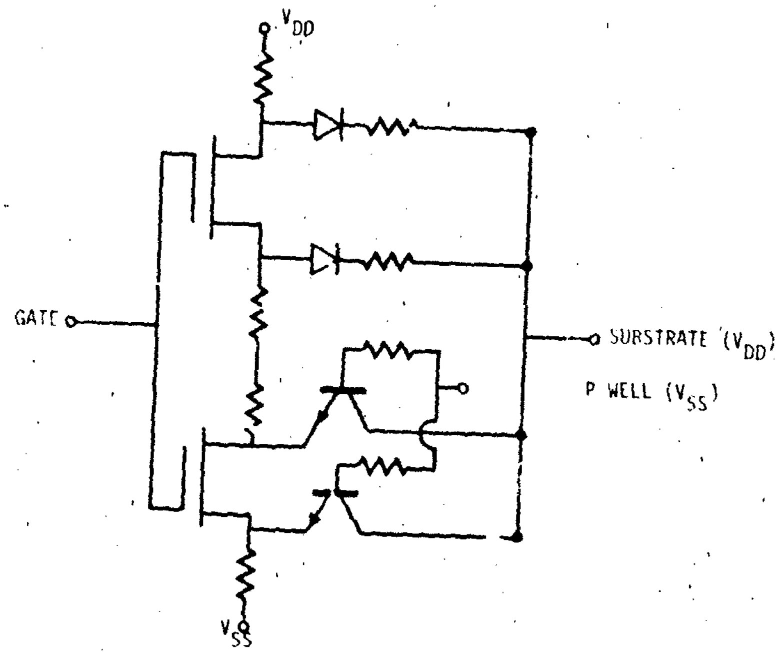


Figure IV-23. Parasitic Inclusive Schematic of CMOS Inverter

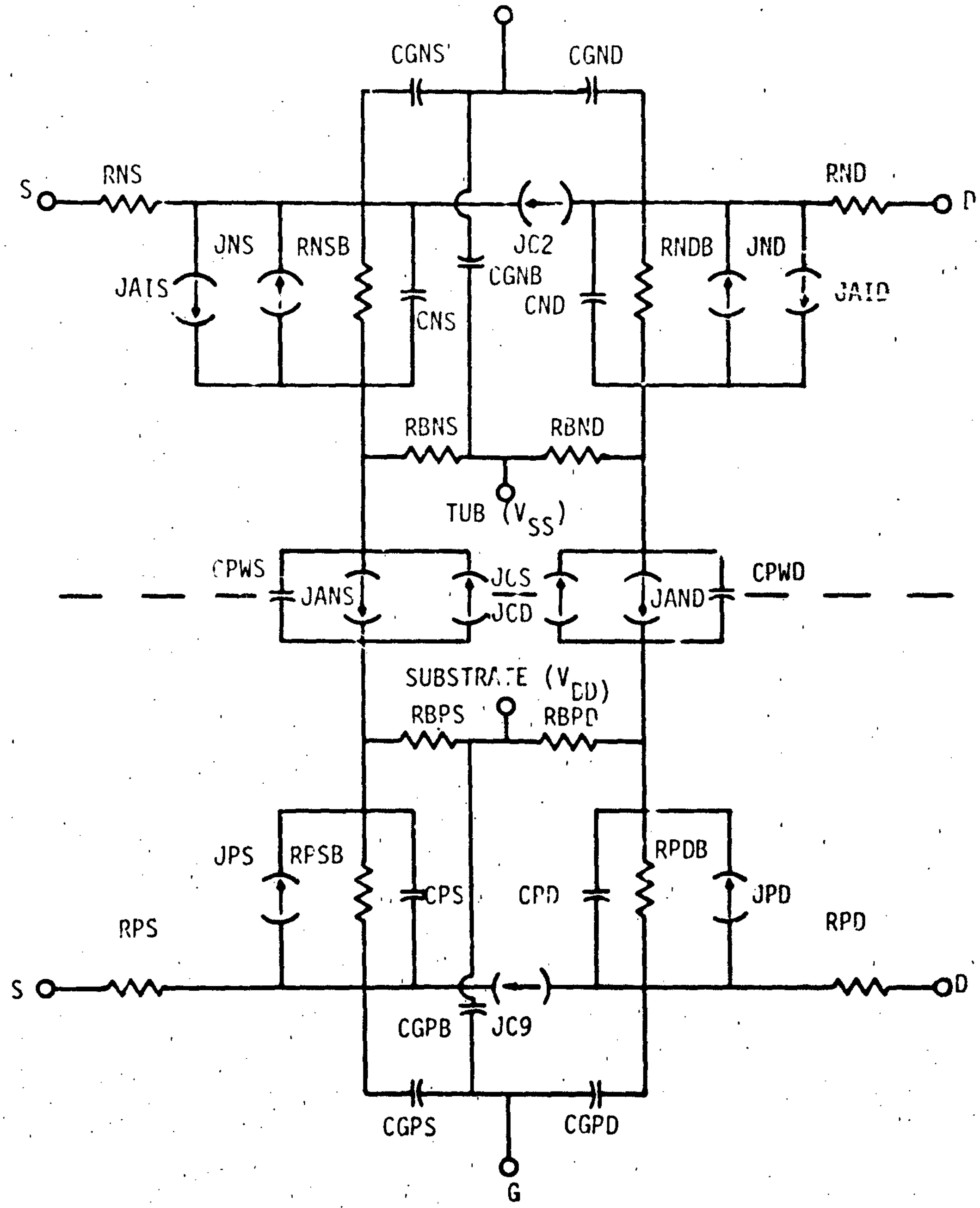


Figure IV-24. Model Topology for CMOS Pair

terms developed for bipolar diodes in chapter II. During normal operation, the source and drain junctions should remain reverse biased and only the depletion capacitance term should be required. Source and drain resistances are included for both the N- and P-channel transistors as RNS, RND, RPS, and RPD, respectively.

The remaining resistors, capacitors, and current sources in figure IV-24 are included to model the parasitic bipolar diodes and transistors associated with the CMOS inverter. Each source and drain is represented by a diode equation current generator (JNS, JND, JPS, JPD). Since these junctions are normally reverse biased, only the reverse saturation current is important for most applications. The resistors RNSB, RNDB, RPSB, and RPDB represent that portion of the leakage current that is voltage dependent. The resistors RBNS, RBND, RBPS, and RBPD represent the bulk resistances due to the semiconductor material between the metallurgical junctions and the ohmic contacts to the power supplies.

In bulk CMOS technologies, there is an additional PN junction between the P-well and the N-substrate. This junction is represented by the diode current generators JCS and JCD. Capacitors CPWS and CPWD represent the depletion region and diffusion capacitance associated with the junction. Since the three layer structure composed of the N-channel source (or drain), the P-well, and the N-substrate is an NPN bipolar transistor, the dependent current sources JANS, JAND, JAIS, and JAID have been added to model the required transistor action. The dependencies are as follows:

$$JANS = N1 * JNS$$
$$JAND = N2 * JND$$
$$JAIS = I1 * JCS$$
$$JAID = I1 * JCD$$

These are the same as discussed for the bipolar transistor models in chapter III. Since all the diode junctions are normally reverse biased, the parasitic transistor is turned off for standard operating conditions. However, it can become extremely important in modeling ionizing radiation effects.

5. Defining Equations

Only the gate-to-semiconductor capacitances are described by equations which have not been discussed previously.

For $V_{GS} \geq V_T$ or $V_{GD} \geq V_T$,

$$CGS = \frac{2}{3} WL\, C_{OX} \left\{ \frac{(V_{GS} - V_T)\left[3(V_{GS} - V_T) - 2(V_{GS} - V_{GD})\right]}{(V_{GS} - V_T + V_{GD} - V_T)^2} \right\} + CGSO$$

$$CGD = \frac{2}{3} WL\, C_{OX} \left\{ \frac{\left[2(V_{GS} - V_T) + (V_{GD} - V_T)\right](V_{GD} - V_T)}{(V_{GS} - V_T + V_{GD} - V_T)^2} \right\} + CGDO$$

$$CGB = CGBO$$

For $V_{GS} < V_T$ and $V_{GD} < V_T$,

$$CGB = WL\, C_{OX} + CGBO$$
$$CGS = CGSO$$
$$CGD = CGDO$$

Note the following cases of interest:

(1) At $V_{GS} = V_T$ or $V_{GD} = V_T$ and $V_{DS} = 0$, the equations above reduce to

$$CGS = \frac{1}{2} WL\, C_{OX} + CGSO$$

$$CGD = \frac{1}{2} WL\, C_{OX} + CGDO$$

(2) At saturation in normal mode, $V_{GS} - V_{GD} = V_{GS} - V_T$

$$CGS = \frac{2}{3} WL\, C_{OX} + CGSO$$

$$CGD = 0$$

The equations for parasitics associated with the diffusions are given below. They have been treated in chapters II and III. The reader is referred to these chapters for more detailed discussions.

$$RS = \frac{\rho_S\, \ell_S}{A_S} = \rho_{\square S} \frac{\ell_S}{W_S}$$

$$RD = \frac{\rho_D\, \ell_D}{A_D} = \rho_{\square D} \frac{\ell_D}{W_D}$$

$$JS = A_S J_0 \left(e^{\theta V_{SB}} - 1 \right)$$

$$JD = A_D J_0 \left(e^{\theta V_{DB}} - 1 \right)$$

$$CS = \frac{C_0\, A_S}{\left(1 - \frac{\phi}{V_{SB}}\right)^n}$$

$$CD = \frac{C_0\, A_D}{\left(1 - \frac{\phi}{V_{DB}}\right)^n}$$

$$JANS = \alpha_{N1} * JNS$$

$$JAND = \alpha_{N2} * JND$$

$$JAIS = \alpha_{I1} * JCS$$

$$JAID = \alpha_{I2} * JCD$$

6. Parameter List

ρ = material resistivity

$\rho_{\square}$ = sheet resistivity (ohms per square)

ℓ = length

W = width

J_0 = reverse saturation current density

A = area

ϕ = contact potential

n = junction grade constant

α_N = normal common base current gain

α_I = inverse common base current gain

CGS total gate-to-source capacitance = $f(V_{GS}, V_{GD})$

CGSO gate-to-source capacitance due to gate overlap of the source = a constant

CGD total gate-to-drain capacitance = $f(V_{GS}, V_{GD})$

CGDO gate-to-drain capacitance due to gate overlap of the drain = a constant

CGB total gate-to-substrate capacitance = $f(V_{GS})$

CGBO gate-to-substrate capacitance due to gate overlap of the substate

RNS & RPS = source resistance

RND & RPD = drain resistance

RNSB & RPSB = source-to-substrate leakage resistance

RNDB & RPDB = drain-to-substrate leakage resistance

RBNS & RBND = P-well resistances

PBPS & RBPD = substrate resistances

JNS & JPS = source diode current generator

JND & JPD = drain diode current generator

JCS & JCD = P-well-to-substrate diode current generator

JANS & JAND = parasitic collector dependent current sources

JAIS & JAI = parasitic emitter dependent current sources

7. Parameterization

Values for parasitic parameters are typically difficult to measure for several reasons. First, the capacitive terms are often masked by the packaging capacitance, and measured gate capacitance data cannot be easily separated into package capacitance, gate-to-source gate-to-drain, and gate-to-substrate depletion capacitances. Furthermore, the gate electrodes of almost all MOS integrated circuits and many discrete MOS transistors are protected by networks which protect the gate from electrical overstress transients. The capacitance of these protection networks usually completely masks the gate capacitance. They also clamp the voltages which can be applied to the gate to levels below those necessary to separate source and drain resistance effects from variable mobility effects.

Usually the best approach for estimating parasitics is to use typical values for the MOS process being analyzed and scale the values by the appropriate geometrical dimensions of the device. The following discussion provides a list of typical values and techniques to be used for estimating model parameters from them. The typical values are most applicable to CMOS/Metal gate technology with gate oxide thicknesses of approximately 700 Å. Figure IV-25 shows the topological layout of rows of N-channel and P-channel devices similar to those found in CMOS technology. It will be used as the principal reference in the examples.

a. Gate Capacitances (C_{OX}, CGSO, CGDO, CGBO)

The key parameter to be determined in establishing the values of gate capacitances is C_{OX}. This is the capacitance per unit area of the gate-thin oxide semiconductor structure. Its value can be estimated from the permittivity of the gate insulator divided by the insulator thickness.

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$$

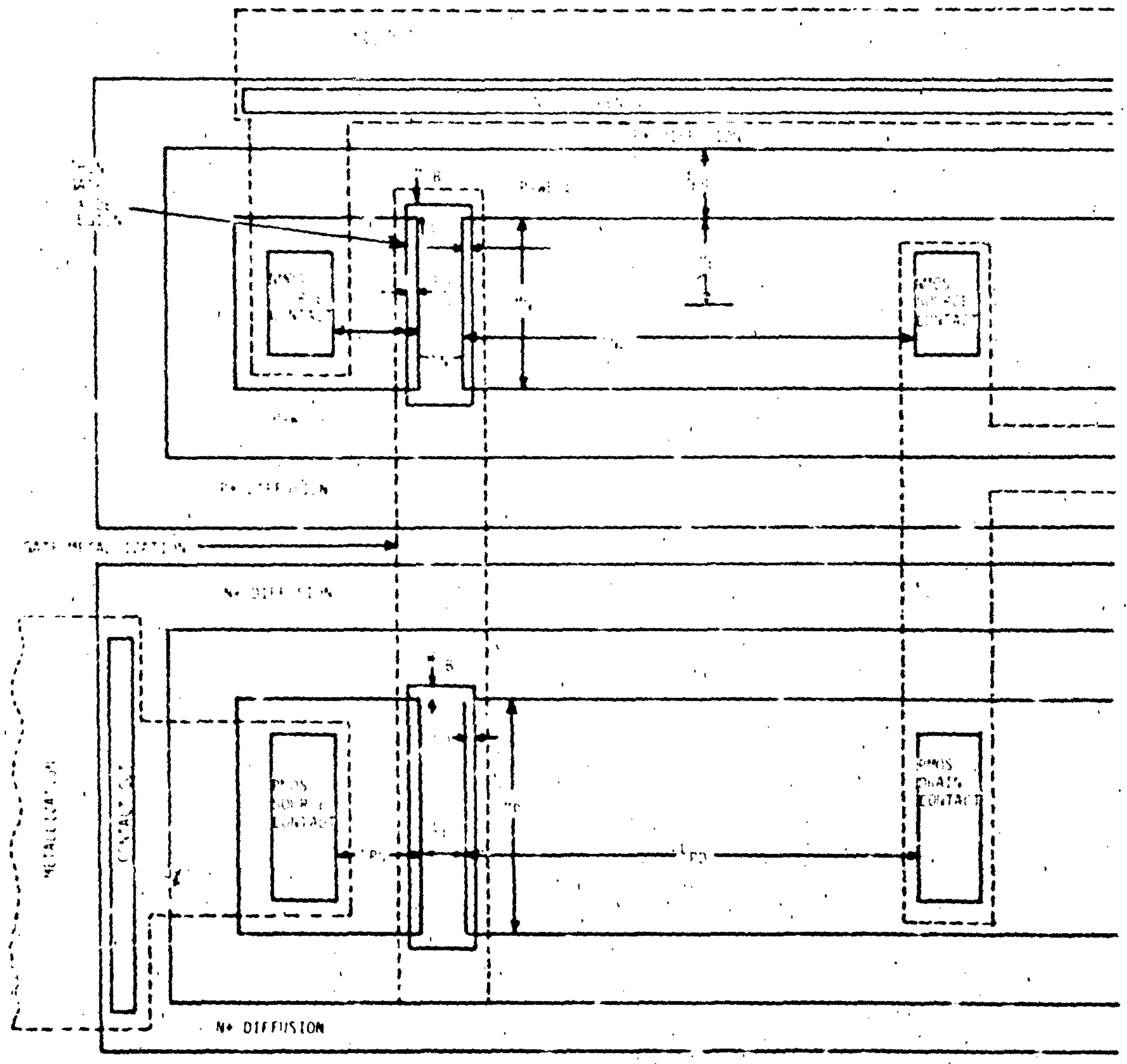


Figure IV-25. Typical CMOS Topology

Typical values for SiO_2 technologies are:

$$\varepsilon_{OX} = 3.54 \times 10^{-13} \frac{F}{cm}$$

$$t_{OX} = 8 \times 10^{-6} \text{ cm}$$

$$C_{OX} = 5.06 \times 10^{-8} \frac{F}{cm^2}$$

This value can be used with the equations presented in section C.5 of this chapter to predict CGS, CGD, and CGB as a function of voltage.

In addition to the voltage variable components of these capacitances, there are fixed capacitance values noted as CGSO, CGDO, and CGBO. These are overlap capacitances which are due to the metal gate extending over the source, drain, and substrate, respectively. The values of these capacitances can be estimated as follows:

	N-Channel	P-Channel
CGSO =	$C_{OX} * L_0 * W_N$	$C_{OX} * L_0 * W_p$
CGDO =	$C_{OX} * L_0 * W_N$	$C_{OX} * L_0 * W_p$
CGBO =	$C_{OX} * (L_N + 2L_0) * W_{OB}$	$C_{OX} * (L_p + 2L_0) * W_{OB}$

Typical Values

$L_N = L_p = 5 \times 10^{-4}$ cm (channel length)

$L_0 = 2 \times 10^{-4}$ cm

$W_{OB} = 15 \times 10^{-4}$ cm

W_p & W_N = proportional to the current capability of the MOS transistors (channel width)

b Diode Capacitances

The depletion and diffusion capacitances associated with the source and drain diodes follow the same functional relationships as those discussed in chapter II. Since they are difficult to measure

directly, they can be estimated from a capacitance per unit area and from the forward diode current.

Depletion Capacitance:

$$\frac{C}{A} = \sqrt{\frac{q\varepsilon_{si} N_B}{2(\phi - V_A)}}$$

Typical Values	NMOS	PMOS
q (charge)	1.6×10^{-19} coul	1.6×10^{-19} coul
ε_{si} (permittivity)	1.05×10^{-12} F/cm	1.05×10^{-12} F/cm
N_B (substrate doping)	2×10^{16} cm^{-3}	2×10^{15} cm^{-3}
ϕ (contact potential)	.9 V	.9 V
C/A	4.30×10^{-8} F/cm^2	1.37×10^{-8} F/cm^2
C_D	$4.30 \times 10^{-8} * W_N * L_{ND}$	$1.37 \times 10^{-8} * W_P * L_{PD}$
C_S	$4.30 \times 10^{-8} * W_N * L_{NS}$	$1.37 \times 10^{-8} * W_P * L_{PS}$

Diffusion Capacitance:

$$C = \frac{\tau\theta\, I_D}{2\pi}$$

Typical Values

$$\theta = \frac{1}{.026\text{ V}}$$

τ minority carrier lifetime $= 1 \times 10^{-6}$ sec

$$C/I_D = 6.13 \times 10^{-6} \frac{\text{F}}{\text{amp}}$$

c. <u>Diode Current Parameters</u>

The bipolar diodes associated with the source and drain may be modeled with reasonable accuracy by the first order diode equation.

$$I_D = I_0 \left(e^{\theta V} - 1\right)$$

$$\frac{I_0}{A} = qn_i^2 \left[\frac{D_n}{N_A L_n}\right] \quad \text{N-channel}$$

$$\frac{I_0}{A} = qn_i^2 \left[\frac{D_p}{N_D L_p}\right] \quad \text{P-Channel}$$

Typical Values	N-Channel	P-Channel
q (charge)	1.6×10^{-19} coul	1.6×10^{-19} coul
Ni^2 (intrinsic carrier concentration)	1.96×10^{20} cm^{-6}	1.96×10^{20} cm^{-6}
D (diffusion constant)	39 cm^2/s	15.6 cm^2/s
N_D (doping concentration)	2×10^{16} cm^{-3}	2×10^{15} cm^{-3}
L (diffusion length)	6.25×10^{-3} cm	3.95×10^{-3} cm
$\frac{I_0}{A}$	9.80×10^{-12} A/cm^2	6.20×10^{-11} A/cm^2
θ	38.5	38.5
I_{OD}	$9.80 \times 10^{-12} * W_N * L_{ND}$	$6.20 \times 10^{-11} * W_P * L_{PD}$
I_{OS}	$9.80 \times 10^{-12} * W_N * L_{NS}$	$6.20 \times 10^{-11} * W_P * L_{PS}$

d <u>Drain and Source Resistance</u>

The drain and source resistances may be estimated from values of sheet resistivity and the geometry of the source and drain diffusion.

$$R = \rho_{\square} * \frac{L}{W}$$

Typical Values	N-Channel	P-Channel
$\rho_{\square}$ (sheet resistivity)	10 ohm/square	40 ohm/square
R_S	$10 * \frac{L_{NS}}{W_N}$	$40 * \frac{L_{PS}}{W_P}$
R_D	$10 * \frac{L_{ND}}{W_N}$	$40 * \frac{L_{PD}}{W_P}$

e. P-Well Resistance

The P-well resistance associated with the base of the parasitic transistors can be estimated from knowledge of the P-well sheet resistivity under the drain and source and the P-well sheet resistivity in the open tub. In the structure shown in figure IV-25, the P^+ diffusion around the P-well produces a low resistivity path to V_{SS} on each side of the drain. This has the effect of paralleling two resistors and making the effective resistance one-half of the value.

$$R_2 = \frac{1}{2} \frac{\rho_{\square D}}{6} \frac{W_E}{L_{ND}} + \frac{1}{2} \frac{\rho_{\square 0} d_{EB}}{L_{ND}}$$

Typical Values

$\rho_{\square 0}$ (open P-well sheet resistivity) 100 Ω per square

$\rho_{\square D}$ (P-well sheet resistivity under the drain) 12,000 Ω per square

$$R_2 = \frac{1000\, W_E}{L_{ND}} + \frac{500\, d_{EB}}{L_{ND}}$$

Note that R_1, the P-well resistor associated with the source, has not been parameterized here. The source of the N-channel which is also the emitter of the parasitic NPN transistor is tied directly to V_{SS} as is the P-well. Thus, it is unlikely that there will ever be a sufficient voltage drop across the base emitter to turn on the parasitic transistor.

f. Substrate Resistance

Substrate resistances are extremely difficult to estimate because of the distributed nature of the substrate and the uncertainty associated with current flow patterns. If the analyst considers these resistances to be important, he must usually select them by a trial and error procedure where results are compared with experimental data which he believes to be influenced by substrate resistance. This is likely to be an expensive procedure and will result only in a simulation of experimental data.

8. Code Implementation

Table IV-4 provides values for parasitic elements as they would be implemented in each of the three models. SCEPTRE, CIRCUS, and TRAC models are lumped together since they implement the MOS model through a user defined subroutine. Similar parameters in each of the codes are placed on the same horizontal lines since the parasitic parameters are based on topological layout of the MOS transistor. The following dimensions have been used to determine the parameter values in the table. The reader should reference figure IV-25 for an explanation of the dimensions.

	N-Channel	P-Channel
Channel length	$L_N = 5 \times 10^{-4}$ cm (.197 mil)	$LP = 5 \times 10^{-4}$ cm (.197 mil)
Channel width	$W_N = 94 \times 10^{-4}$ cm (3.7 mil)	$W_p = 145 \times 10^{-4}$ cm (5.7 mil)
Gate overlap of drain/source	$L_0 = 2 \times 10^{-4}$ cm (7.8×10^{-2} mil)	$L_0 = 2 \times 10^{-4}$ (7.8×10^{-2} mil)
Gate overlap of substrate	$W_{OB} = 15 \times 10^{-4}$ cm (.6 mil)	$W_{OB} = 15 \times 10^{-4}$ (.6 mil)

TABLE IV-4. SCEPTRE, CIRCUS2, TRAC, NET-2, AND SPICE2 MODEL PARAMETERS REQUIRED FOR PARASITIC INCLUSIVE MOS MODEL

SCEPTRE CIRCUS 2 TRAC (SUBROUTINE IMPLEMENTATION)				NET-2 BUILT-IN MODEL				SPICE 2 BUILT-IN MODEL			
CODE PARAMETER	DEFINITION	NMOS VALUE	PMOS VALUE	CODE PARAMETER	DEFINITION	NMOS VALUE	PMOS VALUE	CODE PARAMETER	DEFINITION	NMOS VALUE	PMOS VALUE
S	Type & Transition Factor	+10	-10	S	Polarity Constant	+1	-1	-	-	-	-
B	Transconductance Factor (β)	2.06E-4 A/V^2	1.67E-4 A/V^2	A4	Transconductance Factor	[illegible]	[illegible]	KP	Intrinsic Transconductance	[illegible].67E-4 A/V^2	2.44-4 A/V^2
VT	Threshold Voltage	+1.69 V	-1.[illegible]3 V	A1	$\frac{-E}{2} V_T$	-.343 mA	[illegible]	VTO	Threshold Voltage	+1.65 V	[illegible]3
				A3	[illegible] 4β	[illegible]	[illegible]				
				A2	**	0*	0*	GAMMA	**	0*	0*
				A5	**	0*	0*	UO	**	0*	0*
								UCRIT	**	0*	0*
								UEXP	**	0*	0*
								UTRA	**	0*	0*
CBD	Substrate-Drain Depletion Capacitance	[illegible] F	5.06E-13 F	C1	Substrate-Drain	[illegible] pF	[illegible] pF	CBD	Substrate-Drain	3.[illegible] F/cm^2	9.62E-9 F/cm^2
CBS	Substrate-Source Depletion Capacitance	9.50E-13 F	5.05E-13 F	C12	Substrate-Source Depletion Capacitance	.950 pF	.505 pF	CBS	Substrate-Source Depletion Capacitance	3.[illegible] F/cm^2	9.62E-9 F/cm^2
CGB	Gate-Substrate Overlap Capacitance	1.68E-15 F	1.68E-15 F					CGB	Gate-Substrate Overlap Capacitance	6.65E-13 F/cm	6.65E-13 F/cm

TABLE IV-4. SCEPTRE, CIRCUS2, TRAC. NET-2, AND SPICE2 MODEL PARAMETERS REQUIRED FOR PARASITIC INCLUSIVE MOS MODEL (Continued)

SCEPTRE CIRCUS 2 TRAC (SUBROUTINE IMPLEMENTATION)				NET-2 FUNCTION MODEL				SPICE 2 FUNCTION MODEL			
CODE PARAMETER	DEFINITION	NMOS VALUE	PMOS VALUE	CODE PARAMETER	DEFINITION	NMOS VALUE	PMOS VALUE	CODE PARAMETER	DEFINITION	NMOS VALUE	PMOS VALUE
CGD	Fixed Value Gate-Drain Capacitance [illegible]	1.54E-13 F	2.44E-13 F	CGD	Low Level Gate-Drain Capacitance	[illegible]	[illegible]	[illegible]	Gate-Drain Overlap Capacitance [illegible]	[illegible]	[illegible]
CGS	Fixed Value Gate-Drain Capacitance [illegible]	1.54E-13 F	2.44E-13 F	CGS	Low Level Gate-Source Capacitance [illegible]	[illegible]	[illegible]		Gate-Source Overlap Capacitance [illegible]	[illegible]	[illegible]
				IP1	**	0*	0*				
				IP12	**	0*	0*				
				IP21	**	0*	0*				
				IP22	**	0*	0*				
ISS	Substrate-Source Saturation Current	[illegible] A	[illegible] A		Substrate-Source Saturation Current	[illegible]	[illegible]		Saturation Current Density	[illegible] $\frac{A}{m^2}$	[illegible] $\frac{A}{m^2}$
ISD	Substrate-Drain Saturation	[illegible] A	2.31E-15 A	IS2	Substrate-Drain Saturation Current	[illegible]	[illegible]				
				M	**	0*	0*	[illegible]	**	0*	0*
				M2	**	0*	0*				
				M3	**	0*	0*				
				[illegible]	**	0*	0*				
				[illegible]	**	0*	0*				
				[illegible]	**	0*	0*				
				[illegible]	**	0*	0*				
				[illegible]	**	0*	0*				
				[illegible]	**	0*	0*				

TABLE IV-4. SCEPTRE, CIRCUS2, TRAC, NET-2, AND SPICE2 MODEL PARAMETERS REQUIRED FOR PARASITIC INCLUSIVE MOS MODEL (Continued)

[illegible]	DEFINITION	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	Substrate to [illegible] Constant	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	Diode [illegible] Constant	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	Substrate [illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

TABLE IV-4. SCEPTRE, CIRCUS2, TRAC, NET-2, AND SPICE2 MODEL PARAMETERS REQUIRED FOR PARASITIC INCLUSIVE MOS MODEL (Concluded)

SCEPTRE/CIRCUS 2/TRAC (SUBROUTINE IMPLEMENTATION)				NET-2 BUILT-IN MODEL				SPICE 2 BUILT-IN MODEL			
CODE PARAMETER	DEFINITION	NMOS VALUE	PMOS VALUE	CODE PARAMETER	DEFINITION	NMOS VALUE	PMOS VALUE	CODE PARAMETER	DEFINITION	NMOS VALUE	PMOS VALUE
				VGD1	V_{GD} Voltage (Saturated Region Transition)	4.[illegible] V	[illegible]				
				VGD2	V_{GD} Voltage Parameter (Linear Region Transition)	[illegible]	[illegible]				
ΦBS	Substrate Source Contact Potential	.9 V	.9 V	Φ2	Substrate Source Contact Potential	.9 V	.9 V	PB	Bulk Junction Contact Potential	.9 V	.9 V
ΦBD	Substrate Drain Contact Potential	.9 V	.9 V	Φ2	Substrate Drain Contact Potential	.9 V	.9 V				
C_{BS}	Substrate Source Diffusion Capacitance Factor	6.12E-6 F/A	6.12E F/A	Φ1	Substrate Source Diffusion Capacitance Constant	6.2[illegible]E-3 [illegible]	6.2[illegible]E-3 [illegible]				
C_{BD}	Substrate Drain Diffusion Capacitance Factor	6.12E6 F/A	6.12E-6 F/A	Φ2	Substrate Drain Diffusion Capacitance Constant	[illegible]E-3 [illegible]	6.2[illegible]E-3 [illegible]				
								PHI	**	[illegible]	[illegible]
RD	Total Drain	3.46 Ω	7.06 Ω					RD	Intrinsic Transistor Drain Resistance	[illegible]	[illegible]
RS	Total Source	2.5[illegible] Ω	7.06 Ω					RS	Intrinsic [illegible]	[illegible]	[illegible]
								TOX	**	Do Not Specify	Do Not Specify
								NSUB	**	[illegible]	[illegible]
								NSS	**	[illegible]	[illegible]
								NFS	**	[illegible]	[illegible]
R1	P-well Resistance Source	NA	NA					XJ	**	[illegible]	[illegible]
R2*	P-well Resistance Drain	3502	NA					[illegible]	**	Do Not Specify	Do Not Specify
								[illegible]	**	[illegible]	[illegible]

*Must always be set to indicated value for consistent first order model.
**Discussed in subsequent sections.

	N-Channel	P-Channel
Drain length	$L_{ND} = 32.5 \times 10^{-4}$ cm (1.28 mil)	$L_{PD} = 25.6 \times 10^{-4}$ cm (1.01 mil)
Source length	$L_{NS} = 23.5 \times 10^{-4}$ (.93 mil)	$L_{PS} = 25.6 \times 10^{-4}$ (1.01 mil)
P-well length separating N^+ and P^+	$d_{EB} = 45 \times 10^{-4}$ cm (1.77 mil)	NA
	$V_T = 1.65$	$V_T = -1.10$
	β = 7.67E-4 (KP = 4.07E-5)	β = 2.44E-4(KP = 8.46E-6)

In SCEPTRE, CIRCUS, and TRAC, the parasitic elements are included by attaching the appropriate resistor, capacitor, and diode elements to the nodes of the drain current source as shown in figure IV-24. This technique will be familiar to the SCEPTRE user who is aware of the necessity for constructing his own model. It may be less familiar to the TRAC or CIRCUS user who uses the "built-in" bipolar device models. Table IV-4 includes the values for the elements to be attached to the drain current generator in order to achieve a model topology for a CMOS inverter similar to that of figure IV-24 with one exception. The dependent current sources required to model the parasitic transistor associated with the N-channel device have not been included. Their incorporation is a straightforward application of bipolar transistor modeling concepts discussed in chapter III Thus, only the source-substrate and drain-substrate diodes and the P-well resistance values are given for N-channel parasitics in table IV-4.

The reader should note that fixed value capacitances have been used for C_{BD}, C_{GS}, and C_{GD} in the SCEPTRE, CIRCUS, TRAC models. The tabulated values include the overlap capacitance and half of the channel capacitance in the gate-source and gate-drain capacitors, and only the overlap capacitance in the gate-substrate capacitor. If the analyst knows that the transistor is going to be operated primarily in the saturated, triode, or cutoff mode, he may wish to apportion the capacitance values differently.

The NET-2 model incorporates some parasitic elements within the MOS model parameter list. Only those elements so included are listed in table IV-4. Certainly other parasitics could be included as discrete elements attached to the appropriate node. Specifically, the gate-to-substrate capacitance, source and drain resistances, and the NPN parasitic bipolar transistor are not included. NET-2 does include voltage variable gate-to-source and gate-to-drain capacitances in the model. However, caution is required to use them properly. Their defining equations are presented below.

$$C_{GS} = C_{GSI} \quad \text{for } V_{GS} < V_{G1} \quad \text{(cutoff region)}$$

$$C_{GS} = \frac{\sqrt{2}\ \ C_{GSI}}{\sqrt{1 + \frac{V_{GS}}{V_{G1}}}} \quad \text{for } V_{G1} \le V_{GS} \le V_{G2} \quad \text{(saturation region)}$$

$$C_{GS} = \frac{\sqrt{2}\ \ C_{GSI}}{\sqrt{1 + \frac{V_{G2}}{V_{G1}}}} \quad \text{for } V_{GS} > V_{G2} \quad \text{(triode region)}$$

$$C_{GD} = C_{GD1} \quad \text{for } V_{GD} < V_{GD1} \quad \text{(cutoff region)}$$

$$C_{GD} = \frac{\sqrt{2}\ \ C_{GD1}}{\sqrt{1 + \frac{V_{GD}}{V_{GD1}}}} \quad \text{for } V_{GD1} \le V_{GD} < V_{GD2} \quad \text{(inverted saturation region)}$$

$$C_{GD} = \frac{\sqrt{2}\ \ C_{GD1}}{\sqrt{1 + \frac{V_{GD2}}{V_{GD1}}}} \quad \text{for } V_{GD2} < V_{GD} \quad \text{(inverted triode region)}$$

If the analyst associates V_{C1} with the threshold voltage and requires the value of capacitance in saturation to be two-thirds of its cutoff value

(see chapter IV.E), then V_{G1} equals 2/7 V_T. Similarly, if V_{G2} is associated with the transition to triode operation and the value of capacitance in that region is one-half of its cutoff value, then

$$V_{G2} = 7\ V_{G1} = 2\ V_T$$

Similar arguments hold for C_{GD}. In reality, the gate capacitance in cutoff should be apportioned to C_{GB} with only the overlap capacitances being associated with C_{GS} and C_{GD}. However, if the substrate is electrically tied to the source, as is often the case, the gate capacitance in cutoff can all be apportioned to C_{GS}. As long as the transistor operates in the normal mode (source acts as the source and drain acts as the drain), the above equations give approximately correct behavior of the gate capacitance. In this case, C_{GS1} should be the total channel capacitance ($C_{OX}*W_N*L_N$ or $C_{OX}*W_P*L_P$) and C_{GD1} should be the fixed gate-drain overlap capacitance. The gate-source overlap capacitance should be included as a fixed value capacitance external to the model. However, if the transistor may operate in both normal and inverted modes (e.g., a transmission gate), both overlap capacitances should be included as external fixed value capacitors, and half of the channel capacitance should be apportioned to C_{GS1} and C_{GD1}. The values in the table IV-4 reflect the assumption that the transistor will always operate in the normal mode.

The SPICE2 MOS model also incorporates a large number of parasitic elements as integral parts of the model. The SPICE2 model was designed primarily to assist integrated circuit designers in analyzing new circuits. Therefore, a number of features have been included for their convenience. The analyst must be aware of these features in applying the model. He should consider the model to represent the intrinsic MOS transistor. The intrinsic transistor is that portion of the device that lies under the gate metallization. It includes the channel and the

drain and source overlap regions. All parasitic elements are assumed to be continued to this region. The values of C_{GB}, C_{GS}, and C_{GD} in the parameter list should be given in units of F/cm. They are determined as follows:

$$C_{GB} = C_{OX} * W_{OB}$$

$$C_{GS} = C_{OX} * L_0$$

$$C_{GD} = C_{OX} * L_0$$

SPICE2 takes these values and multiplies them by the appropriate dimensions ($C_{GB}*L_N$ or $C_{GB}*L_P$; $C_{GS}*W_N$ or $C_{GS}*W_P$; $C_{GD}*W_N$ or $C_{GD}*W_P$) to determine actual capacitance values. The value of channel capacitance is calculated automatically and attributed to the gate-substrate, gate-source, or gate-drain depending on the region of operation. The equations governing the transitions are given in figure IV-26 which also shows a qualitative representation of the capacitance values in the three operating regions.

The depletion region capacitance and reverse saturation current are in units of F/cm^2 and A/cm^2, respectively. These values are multiplied by the source and drain areas provided in the model call to determine actual values. The diffusion capacitance is not included as part of the SPICE2 MOS model.

Fixed value source and drain resistors are included in the SPICE2 parameter list. In table IV-4, these values have been calculated for the intrinsic transistor only. They were determined as follows:

$$R = \rho_{DP} \frac{L_0}{W_P} \quad \text{or} \quad \rho_{DP} \frac{L_0}{W_N}$$

Thus, the resistance associated with the source and drain outside the overlap regions were not included in the model, but they may be included with external elements.

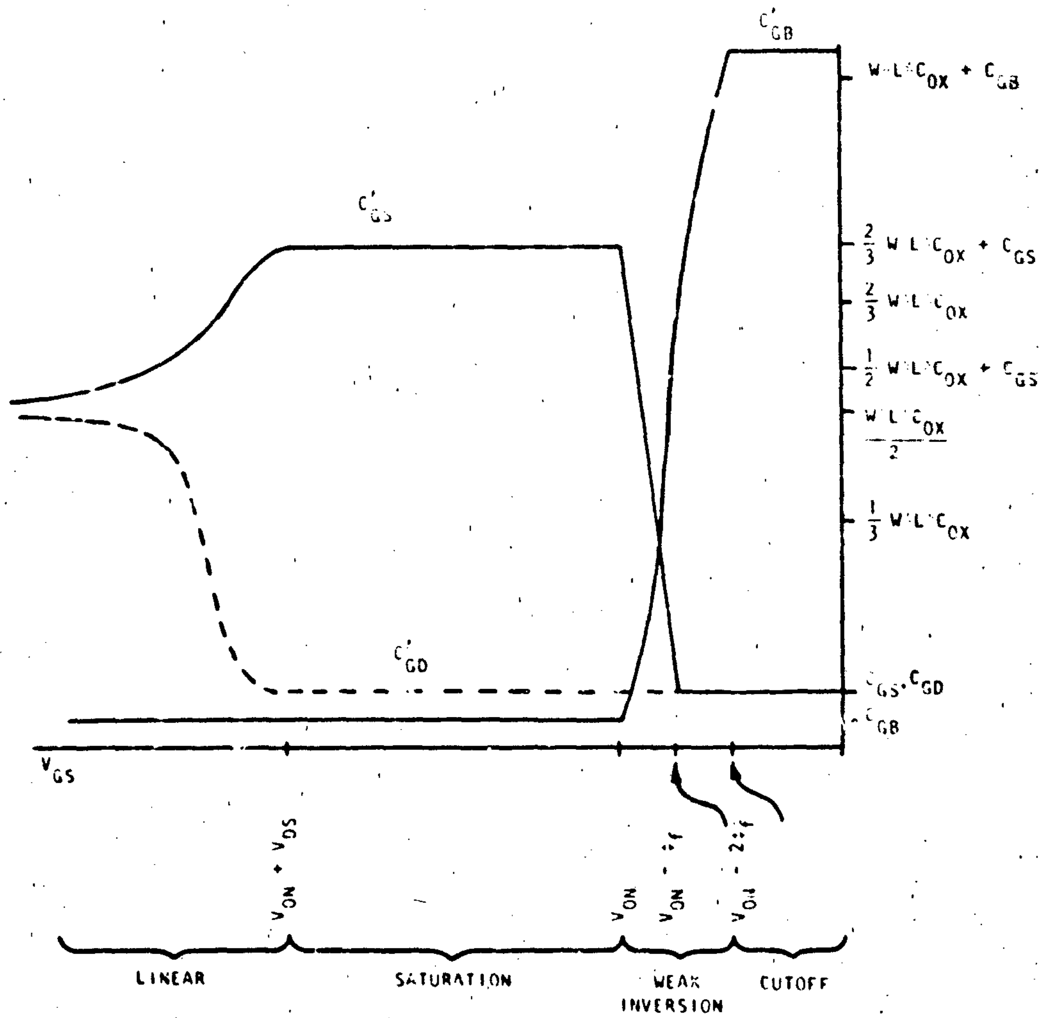


Figure IV-26. Gate Capacitances as a Function of Gate Voltage as Modeled by SPICE2

9. Computer Example

Figure IV-27 shows the model schematic for a CMOS inverter. It includes full parasitics for both an N-channel and P-channel device. Note that the resistance associated with the source and drain diffusions, but outside the intrinsic transistor, has to be modeled with two series resistances (e.g., RPDP11 and RPDP12). The parasitic diode or bipolar transistor has been connected to the common node of these resistors (e.g., DPDP1). The SPICE2 coding for the model is shown in figure IV-28 and the results of exercising the model with a 1 ms pulse are shown in figure IV-29.

D. RADIATION EFFECT INCLUSIVE MOS MODELS

1. Description

In modeling the response of MOS transistors to radiation exposure, the analyst is primarily concerned with ionizing radiation and electrical overstress pulses resulting from EMP. Since MOS transistors are majority carrier devices, their performance is not significantly affected by minority carrier lifetime degradation caused by neutron damage. Also, the effects of neutron damage are very difficult to separate from the damage caused by the ionizing radiation accompanying the neutron fluence. As a result, there is no reliable parameterizing data available for neutron effect modeling. The NET-2 MOS model contains neutron damage modeling parameters for modifying parasitic elements such as the reverse saturation current and the diffusion capacitance. However, these are identical to the model modifications treated under bipolar diodes and transistors. They will not be discussed again here. The interested reader is referred to the radiation effect sections of chapters II and III.

Ionizing radiation produces both permanent damage and transient photocurrents in MOS devices. The degree of permanent damage is proportional to the total accumulated dose. Ionizing radiation produces hole-electron pairs in the gate insulator. In SiO_2, the electrons have a

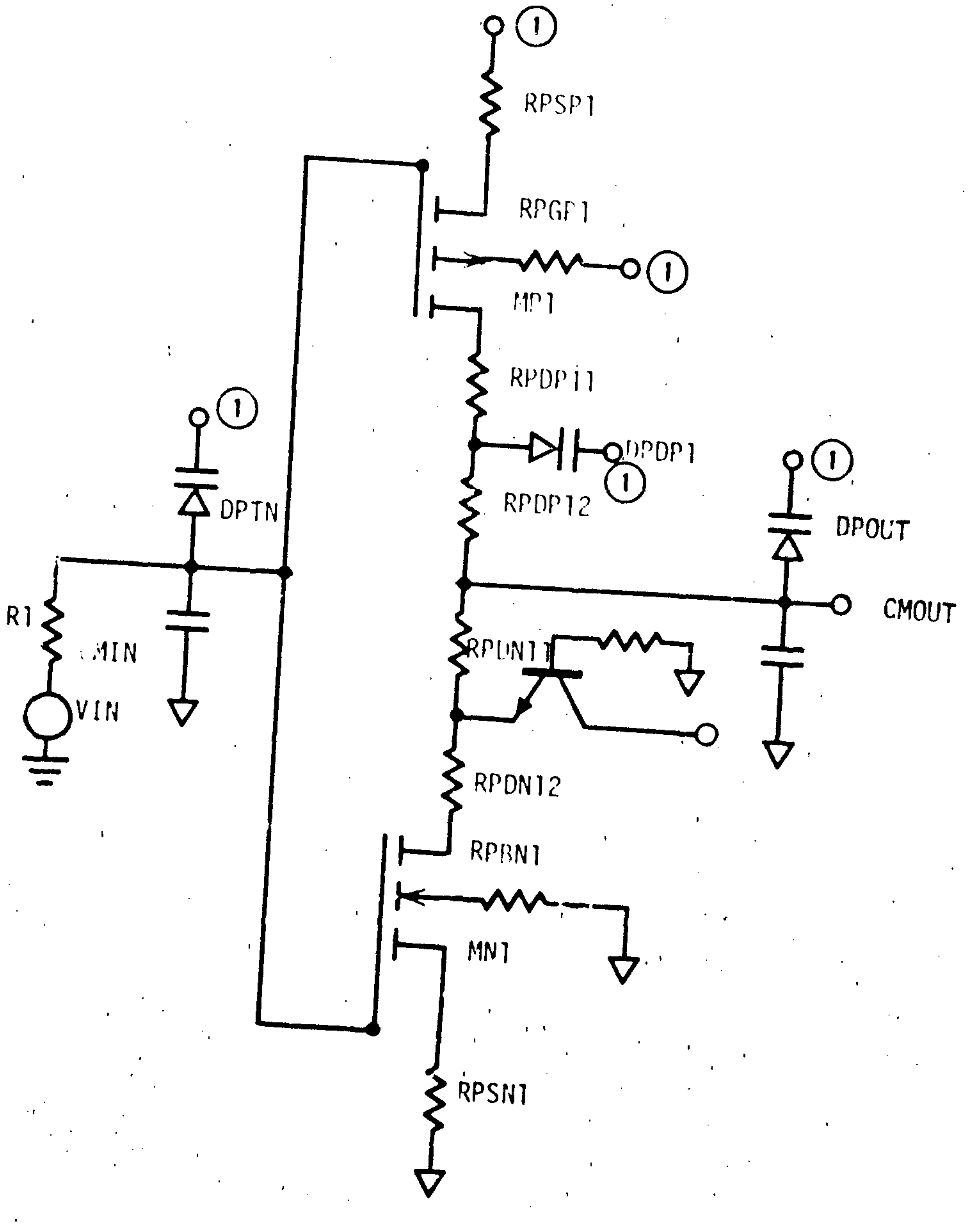


Figure IV-27. Inverter Example

```
     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

***********************************************************************

.MODEL NCHNL1 NMOS(VTO 1.65       KP 4..7E-5      RD .21
+                  RS .21         CBD 3.04E-8     CBS 3.04E-6
+                  CGB 6.65E-13   CGD 8.86E-12    CGS 8.86E-12
+                  JS 9.81E-12    PB .9)
.MODEL PCHNL1 PMOS(VTO -1.13      KP 8.4E-5       RD .55
+                  RS .55         CBD 9.62E-9     CBS 9.62E-9
+                  CGB 6.65E-13   CGD 8.86E-12    CGS 8.86E-12
+                  JS 6.2E-11     PB .9)
.MODEL DIODPPN D(CJO 9.62E-9 PB .5)
.MODEL DIODNPW D(CJO 3..4E-8 PB .5)
.MODEL BPXSTR NPN(BF 10..     BR 1..     IS 9.8E-12     CJE 3.04E-8
+                  PE .9      CJC 2..E-8 PC .7     MC .333)
.SUBCKT INVRTR 1 2 3
MP1  4  2  6  5 PCHNL1 W=3.69MIL L=.197MIL AD=2.89E-6 AS=2.89E-6
IPPPR 1 700 EXP(0. 8.98E-5 100.NS 8.NS 124.NS 333.NS)
VPPPR 700 7 DC
MN1  9  2 11 11 NCHNL1 W=3.71MIL L=.197MIL AD=1.39E-6 AS=2.69E-6
QDDN1 1 8.0 8 BPXSTR AREA=2.87E-5
IPPNEF 8 801 EXP(0. 7.28E-5 100.NS 8.NS 124.NS 333.NS)
VPPNEF 801 80  DC
IPPNCR 1 802 EXP(0. 4.46E-5 100.NS 8.NS 124.NS 333.NS)
VPPNCR 812 8 DC
RZDN1 0 80  3332
FDPIN 1 2 VPPPR .21
FDPOUT 1 3 VPPPR .21
DPIN    2 1 DIODPPN AREA=4.93E-6
DPOUT   3 1 DIODPPN AREA=4.93E-6
DPDP1   7 1 DIODPPN AREA=3.42E-5
CMIN    2  0 .33PF
CMOUT   3  0 .04PF
RPSP1   1  4 6.51
RPBP1   1  5 .1
RPDP11  6  7 3.26
RPDP12  7  3 3.26
RPDN11  3  8 1.63
RPDN12  8  9 1.63
RPBN1   10    .1
RPSN1   11    2.29
.ENDS
X1 2 4 5      INVRTR
VDD 1 0 DC 10
RDD 1 2 1
VIN 3 0 PULSE(0..10..25.NS.25.NS.500.NS.1.5US)
RIN 3 4 2K
CO 5 0 2PF
.TRAN 4NS 4..0US
.PLOT TRAN V(5)
.END
```

Figure IV-28. SPICE2 Coding for Parasitic Inclusive CMOS Inverter Model

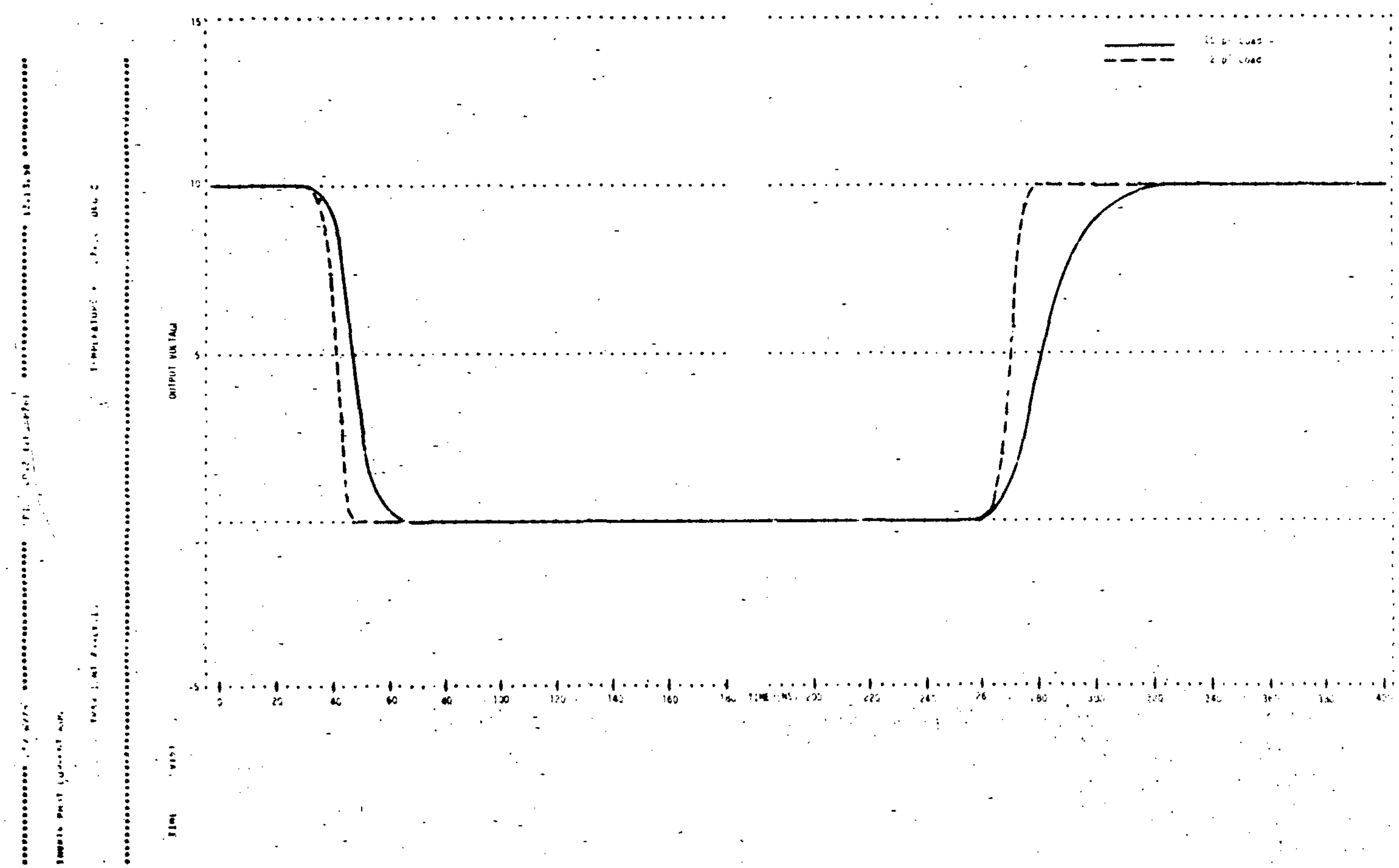


Figure IV-29. Pulse Response of CMOS Inverter Model With Full Parasitics as Exercised on SPICE2

higher mobility than holes. Therefore, they tend to be removed from the insulator. This leaves positively charged holes trapped there. This positive charge attracts electrons to the semiconductor surface and repels holes. The net effect is a shift in the threshold voltage of the device. The amount of threshold shift for a given dose is determined by oxide properties and the polarity and amplitude of gate bias. The physical understanding of charge trapping in the oxide is incomplete at this time. Therefore, no predictive models exist for estimating the degree of threshold voltage shift from physical properties of the device. The analyst must rely on experimental data for parameterization information. He should use extreme caution in extrapolating data on radiation induced threshold voltage shifts to dose levels outside the range of measurements and to devices taken from other manufacturing lots.

In addition to oxide charge trapping, total dose radiation increases the number of surface states, which tends to drive both N-channel and P-channel devices toward enhancement mode operation. In N-channel devices this counteracts the oxide charge trapping effects. In P-channel devices, it adds to oxide trapping effects. Physical mechanisms underlying surface state increase as a function of total dose are not well understood. The analyst should exercise the same caution in utilizing experimental data for threshold voltage shifts caused by surface state density increases. Typically, oxide charge trapping effects tend to dominate threshold voltage shifts below 10^5 rad (Si) and surface state density increases tend to dominate above 10^6 rad (Si). Figure IV-30 shows the effect total dose irradiation has on threshold voltage for sample N-channel and P-channel devices under different gate bias conditions.

Ionizing radiation also produces hole electron pairs in the silicon material of the MOS transistor. As a result, photocurrents appear across the junctions of source-substrate, drain-substrate, P-well-substrate, and any other diodes associated with the MOS device. These photocurrents may charge or discharge circuit nodes and result in

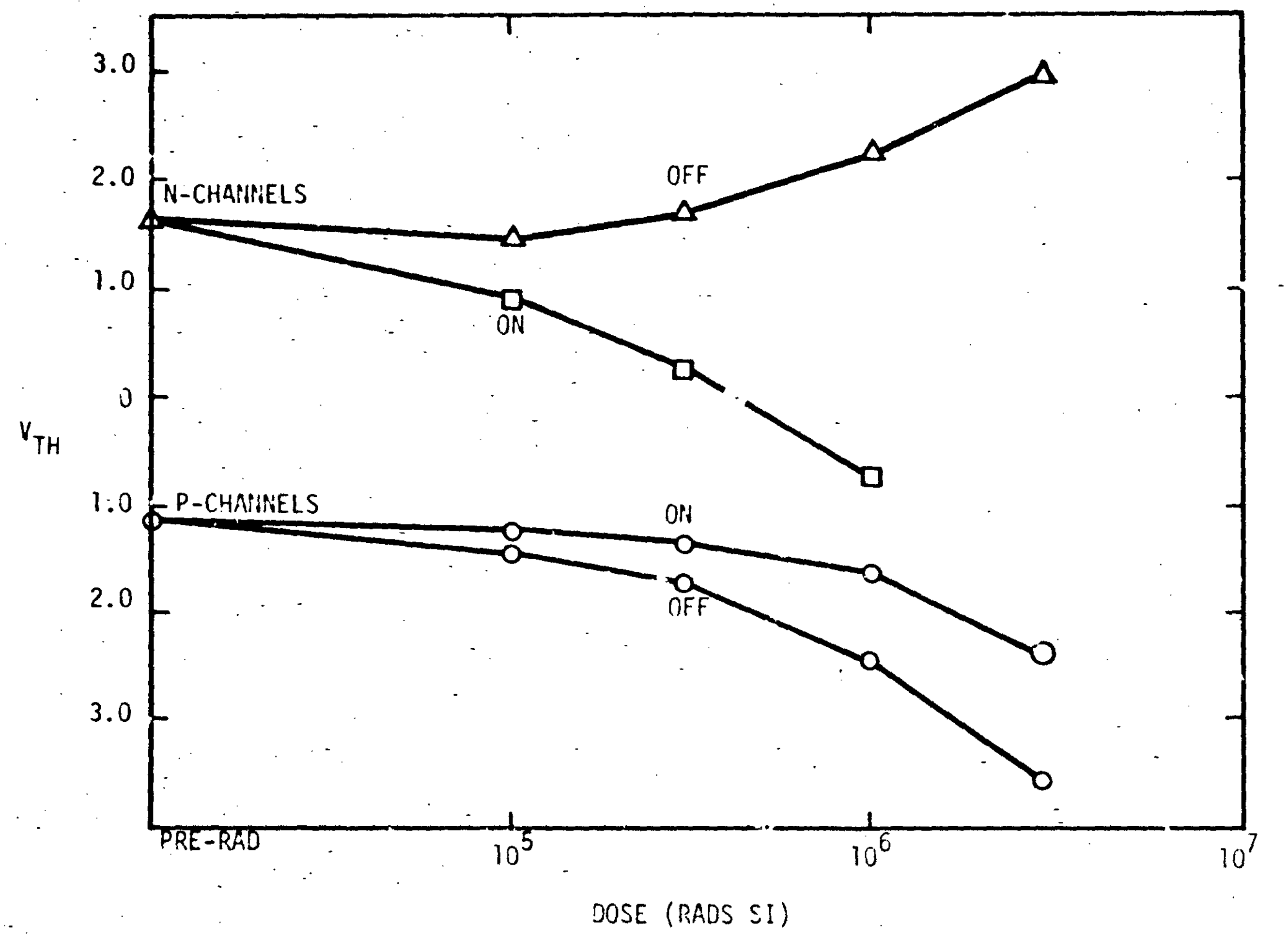


Figure IV-30. Illustration of the Effects of Co^{60} Irradiation on Threshold Voltages

signal transients or state changes in MOS circuits. The parasitic NPN transistors formed in CMOS technology may amplify the primary photocurrents and produce secondary photocurrents; these are particularly effective in changing node voltages. The same techniques for predicting and implementing photocurrents discussed in chapters II and III are effective in predicting photocurrents in MOS devices. They will not be repeated in detail in this chapter. The reader is referred to the radiation effects section of those chapters for supporting information.

Ionizing radiation can produce increased leakage between the gate electrode and the semiconductor material during the radiation pulse. This is due to ionization in the gate dielectric. NET-2 contains provisions for modeling this transient increase in leakage with current generators from gate to source and gate to drain. Transient ionization of the gate dielectric is generally a second order effect in determining the photoresponse of an MOS device. Furthermore, the current generators simulating dielectric ionization generators are extremely difficult to parameterize accurately. Use of the generators is not recommended and will not be treated in this handbook.

Electrical overstress pulses can result from EMP, photocurrents, electrostatic discharge, or normal system turn-on transients These pulses can damage MOS devices by rupturing the gate dielectric. The dielectric strength of SiO_2 is quite high (7×10^6 V/cm); however, the gate oxide is extremely thin (700-1000 Å). Only 50 to 70 volts are required to damage the oxide. Such voltages can be generated by electrostatic discharges encountered in packaging, shipping, and assembly. Therefore, manufacturers provide terminal protection networks on inputs and outputs of MOS IC's and discretes. These are typically combinations of diffused resistors and shunt diodes which clamp transients below the level required for breakdown of the dielectric. For high amplitude, fast risetime transients, the terminal protection network and terminal metallization may be damaged or the bulk resistance associated with the diodes may be sufficiently high to allow the terminal voltage to rise above the gate dielectric breakdown voltage. These effects can be modeled by using the

techniques discussed in chapters II and III for EMP effects on diodes and transistors. In addition, the gate voltage must be monitored to insure that it does not exceed the dielectric breakdown.

2. Advantages

Radiation effect modeling for MOS devices can be of significant benefit when combined with a good experimental program for determining parameter values. Circuit states can be easily set and the effects of threshold voltage changes on propagation delays and fanout capability can be readily determined. For transient effects, the voltages at internal nodes can be monitored and the effects of drain and source dimension changes on photoresponse can be economically evaluated. For electrical overstress effects, trade-offs between terminal protection network design and protective efficiency can be investigated.

3. Cautions

There are no reliable procedures currently available for predicting threshold voltage shift as a function of total dose. Seemingly minor variations in processing have produced major changes in threshold voltage shift as a function of total dose. The analyst should never extrapolate data beyond the range of total dose, gate bias, or processing technology for which they were measured. Even when the same processing technology from the same manufacturer is used, significant variations in threshold voltage shift can be expected from lot to lot The best approach is to try to bound the limits of threshold voltage variations and to perform analyses based on those bounds. The results should then be reported as a range of values (e.g., "For threshold voltage shifts between 1 and 2 volts the propogation delay of circuit X was found to vary from 100-200 µs.").

For photoresponse analyses, the parasitic networks are extremely important. In CMOS circuits the NPN transistors associated with the N-channel devices should be carefully modeled. The analyst should also look for potential PNP devices which can be coupled with the NPN parasitics to form an SCR structure. If such a structure is triggered, it may latch in a conducting state and remain conducting even after the radiation

stimulus is removed. The minority carrier lifetimes in the silicon material used for the substrates of MOS devices tends to be quite long. Therefore, the analyst should include the diffusion component of the photocurrent in any photoresponse calculation.

EMP modeling should carefully consider all possible current paths and accurately model all parasitic diode junctions associated with them. This usually results in a reasonable effort for input terminals, but may be unreasonably difficult for outputs and power supply terminals. Analysis results should be verified by test data.

4. Characteristics

a. Topology

Figure IV-31 shows a schematic representation of a CMOS inverter with an input protection network and all photocurrent generators drawn between appropriate nodes. Figure IV-32 shows the model topology required for a photoresponse analysis of the inverter. Note that no topology variations are required to implement threshold voltage variations with total dose. Only a parameter change in the drain current model is required.

b. Typical Effects

Figure IV-33 shows experimental data for the variation in saturated drain current as a function of gate voltage and total dose levels.

5. Defining Equations

a. Total Dose Effects

The threshold voltage can be written as:

$$V_T = \phi_{ms} - \frac{Q_{SS}}{C_{OX}} + 2\phi_f - \frac{2\varepsilon_s q N_B}{C_{OX}} \; 2\phi_f - V_{BS} + \frac{KT}{q}\left[1 + \frac{qN_{FS}}{C_{OX}} + \frac{2\varepsilon_s q N_B}{2C_{OX}\left(2\phi_f - V_{BS}\right)}\right]$$

Section E gives a complete description of this equation and its implementation in second order effect inclusive MOS models. The interested reader is referred to that section. The point to be made here is that both the

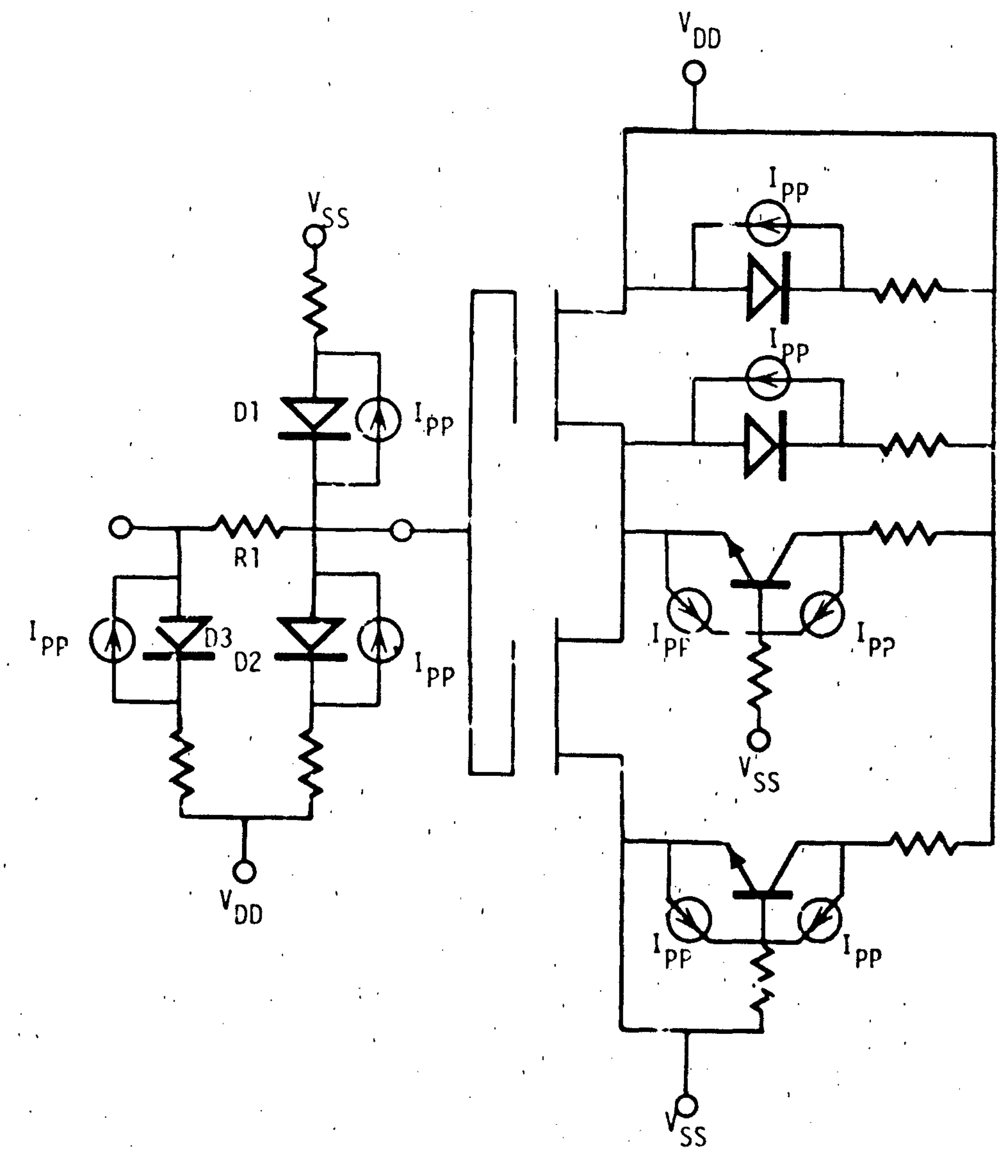


Figure IV-31. CMOS Inverter with Photocurrent Generators Model Topology Required for a Photoresponse Analysis of the Inverter

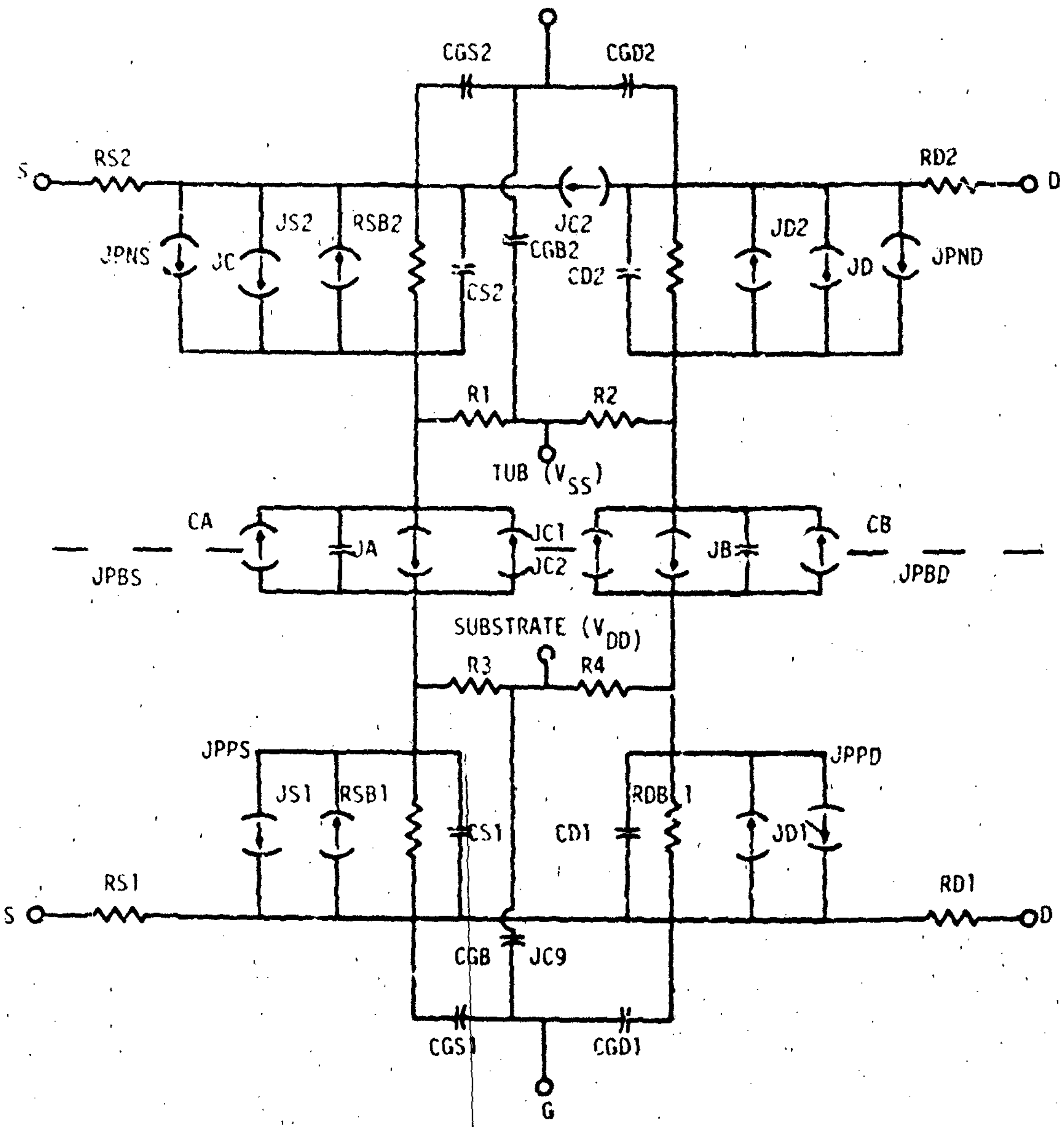


Figure IV-32. Model Topology for CMOS Inverter Photoresponse Analysis

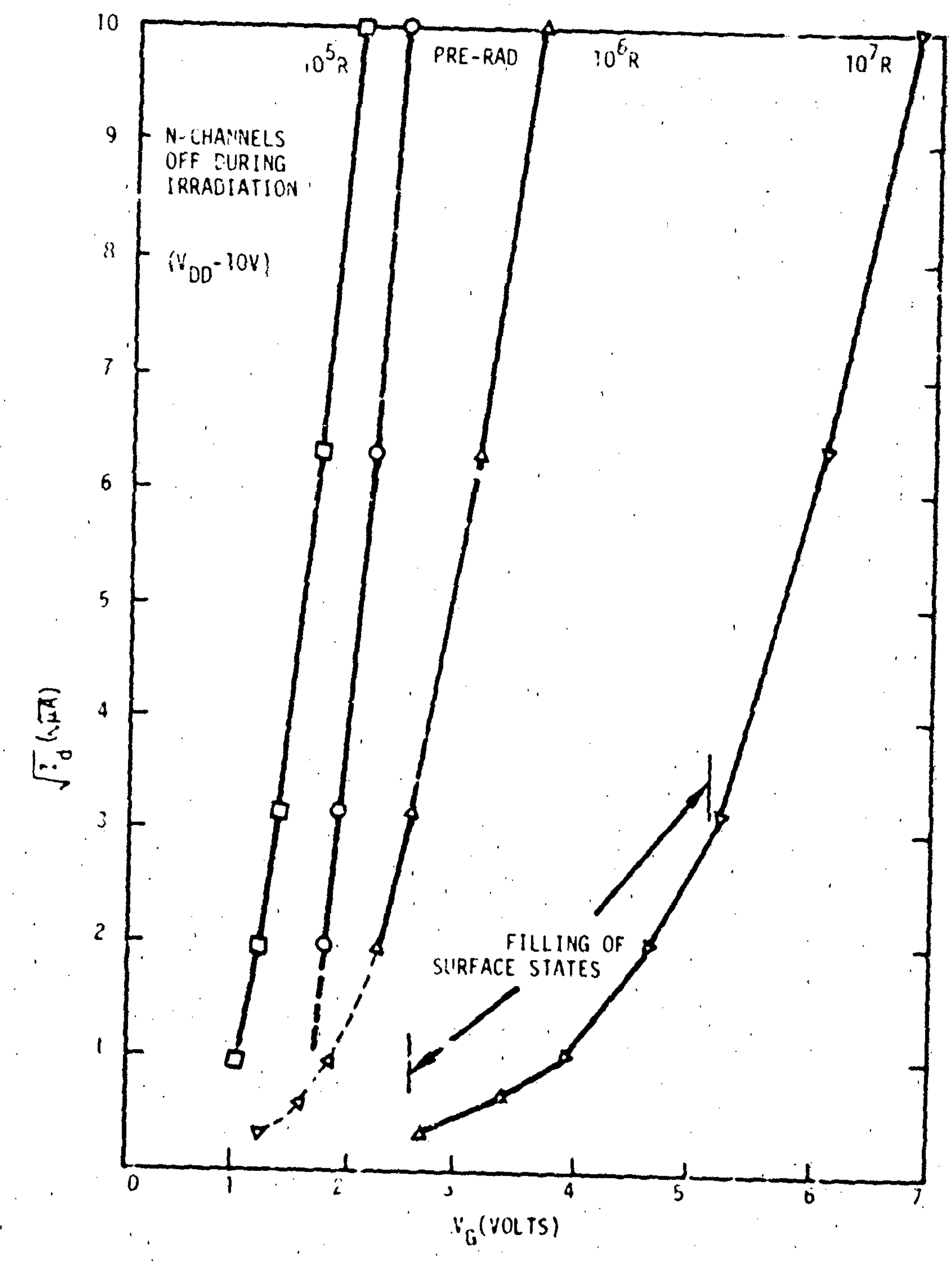


Figure IV-33. The Square Root of Drain Current Versus Gate Voltage for N-Channels Biased OFF During Irradiation

oxide charge (Q_{SS}) and the number of surface states (N_{FS}) directly influence the value of the threshold voltage (V_T). Therefore, threshold voltage shifts resulting from either effect can be modeled by incrementing or decrementing the value of V_T. Thus, total dose effects can be successfully implemented in either first order or second order effect models. In this section, the radiation effects are included with the first order model. In the next section, appropriate discussions are included with the second order model to guide the user in any special requirements for including radiation effects. The presentation here is not meant to imply that the analyst should avoid the use of the second order model with radiation effects. It simply reflects that the presentation of the radiation effects modeling is simpler if the first order model is used.

b. Photocurrent Effects

Any of the defining equations and implementations of photocurrent generators discussed previously with bipolar diodes can be used with the parasitic diodes and transistors in MOS devices. Since the minority carrier lifetimes are quite long in MOS substrates, the diffusion component of the photocurrent should be considered in whichever implementation is chosen. The reader is referred to the radiation effects section of chapters II and III for a more complete discussion. In this section, a douple exponential will be used to simulate the primary photocurrent.

$$I_p = I_{pp} \left(\exp \left\{ \frac{-\text{AMAX1}\left[(t - t_{DF}),\ 0\right]}{\tau_F} \right\} - \exp \left\{ \frac{-\text{AMAX1}\left[(t - t_{DR}),\ 0\right]}{\tau_R} \right\} \right)$$

c. Electrical Overstress Effects

As noted above, electrical overstress pulses can result in damage to either terminal protection networks (D_1, D_2, D_3, and R1 in figure IV-31) or to the gate dielectric. The diode damage in the protection network is a function of the applied power as expressed by the equation

$$P_F = Kt^{-1/2} = I_F V_{BD} + I_F^2 R_B$$

This equation is useful for pulse widths between 100 ns and 100 μs. The value of the damage constant can be estimated from the diode junction area from the empirical equation

$$K = 23.9 A^{.62}$$

The gate voltage must also be monitored to insure that the condition

$$V_g \leq t_{OX} * 7 \times 10^6 \text{ V/cm}$$

is never exceeded.

6. Parameter List

a. Total Dose Effects

ΔV_T - Change in threshold voltage. The parameter may be either positive or negative. The value should be determined from experimental data. The postirradiation threshold voltage becomes

$$V_{T_{Postrad}} = V_{T_{Prerad}} + \Delta V_T$$

b. Photocurrent Response

I_{pp} = peak photocurrent

t_{DR} = time delay between the beginning of the computer solution and the onset of the radiation pulse

τ_R = time constant of the photocurrent leading edge

t_{DF} = time delay between the beginning of the computer solution and the beginning of the photocurrent decay

τ_F = time constant of the photocurrent trailing edge

Figure IV-34 illustrates the primary photocurrent waveform.

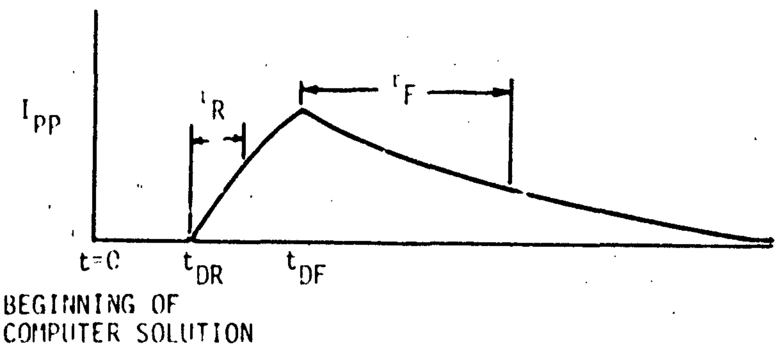


Figure IV-34. Primary Photocurrent Waveform

c. Electrical Overstress

K = damage constant for the diode

P_F = failure power

t = elapsed time from the onset of the electrical overstress pulse

R_B = bulk resistance intimately associated with the junction and contributing to junction heating

7. Parameterization

a. Total Dose Effects - ΔV_T

(1) Typical value - No typical change in threshold voltage shift as a function of total dose can be given because of the large variations resulting from different manufacturing techniques.

(2) Measurement - Figure IV-35 shows the extrapolation of saturated drain current measurements to yield values of threshold voltage shifts for an off N-channel device. Table IV-5 gives the values of ΔV_T which will be used for N-channel and P-channel devices irradiated under two different bias conditions in the following examples.

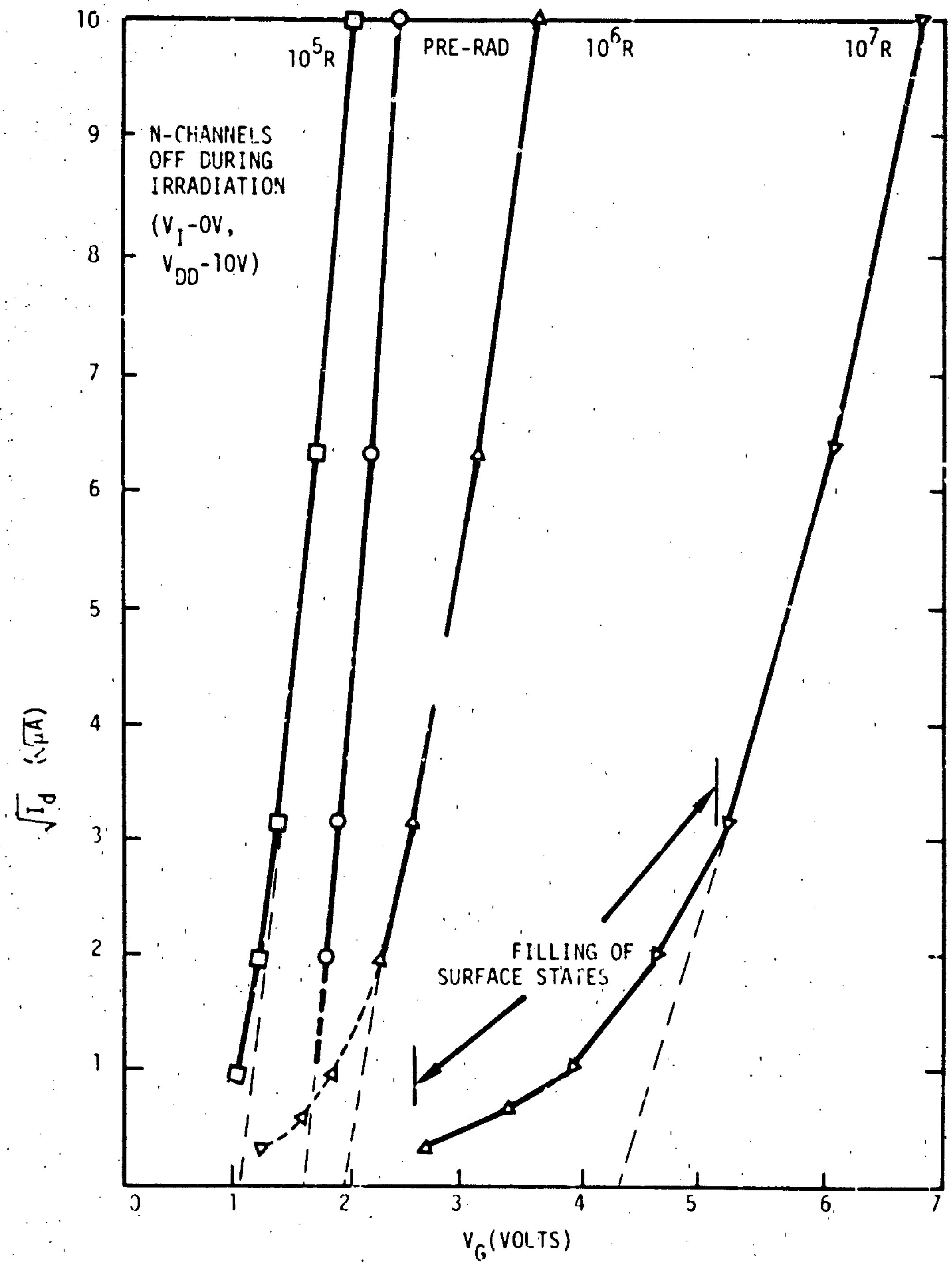


Figure IV-35. Determination of Threshold Voltage Shifts from Postirradiation Saturated Drain Current Measurements

TABLE IV-5. THRESHOLD VOLTAGE SHIFTS INDUCED BY TOTAL IONIZING DOSE

	0 V_T	1×10^5(rad) ΔV_T	2×10^5(rad) ΔV_T	5×10^5(rad) ΔV_T
N-channel (on)	+1.65 V	-1.47 V	-2.20 V	-3.60 V
N-channel (off)	+1.65	- .50	+ .20	+ .40
P-channel (on)	-1.13	- .15	- .15	- .30
P-channel (off)	-1.13	- .27	- .47	- .82

Note that in figure IV-35 the slope of the I_D versus V_G curve changes significantly at higher doses. Also, significant currents flow below the threshold voltage at doses greater than 10^6. Variations in slope can be accounted for by modifying the β parameter in the first order model. Current flow below the threshold voltage will be treated in the next chapter (see weak inversion effect in section IV-E). The analyst must use his judgment and the requirements of his analysis to decide when these effects become important.

b. Photocurrent Effects

(1) I_{pp} - Peak photocurrent. Typical value - peak values of primary photocurrent may be estimated using the following equation:

$$\frac{I_{pp}}{cm^2} = 6.4 \times 10^{-6} * \dot{\gamma} \left[W + L \operatorname{erf}\left(\frac{t_{DF} - t_{DR}}{\tau}\right)\right]$$

$$W = \text{depletion layer width} = \sqrt{\frac{2\varepsilon_s (\psi - V_T)}{q N_B}}$$

$W = 7.69 \times 10^{-5}$ cm for $N_B = 2 \times 10^{15}$ (P^+N diode) at $V_j = 0$ V

$= 2.68 \times 10^{-4}$ at $V_j = 10$

$W = 2.43 \times 10^{-5}$ cm for $N_B = 2 \times 10^{16}$ (N^+P diode) at $V_j = 0$

$= 8.46 \times 10^{-5}$ at $V_j = 10$

L - diffusion length $= \sqrt{D\tau} = \sqrt{\frac{Kt}{q}\,\mu\tau}$

$L = 3.95 \times 10^{-3}$ cm for $N_B = 2 \times 10^{15}$, P^+N

$L = 5.10 \times 10^{-3}$ cm for $N_B = 2 \times 10^{16}$, N^+P

erf .025 = .028

erf .100 = .112

erf .5 = .521

erf 1 = .843

For a 25-ns pulse width and material with a 1-μs minority carrier lifetime, the following can be considered typical values of I_{pp} for a dose rate of 10^9 rad (Si)/s:

	0 V	10 V
N^+P diode	1.07 A/cm^2	1.46 A/cm^2
N^+P diode	1.2 A/cm^2	2.42 A/cm^2

(2) τ_R - Time constant for leading edge at the pulse. Typical value - approximately one-third of the time between the onset of the radiation pulse and the maximum photocurrent. For a radiation pulse with a pulse width of 25 ns, τ_R = 8 ns.

(3) τ_T - Time constant for trailing edge of the pulse. Typical value - approximately one-third of the minority carrier lifetime assumed for the material. For a minority carrier lifetime of 1 μs, τ_F = 333 μs.

c. Electrical Overstress

(1) K - Damage constant. Typical value - $K = 20.9\ A^{.62}$. For the diodes to be used in the example:

$A_1 = 1.66 \times 10^{-5}\ cm^2 \qquad K = .026$
$A_2 = 6.84 \times 10^{-6}\ cm^2 \qquad K = .015$
$A_3 = 2.32 \times 10^{-5}\ cm^2 \qquad K = .032$

These are damage constants for reverse biasing electrical overstress pulses. If the pulse forward biases the junction, the damage constants are typically multiplied by a factor of 10.

(2) R_B. Typical value - estimation of the bulk resistance is generally quite difficult. However, values of 30 Ω have given satisfactory results in previous investigations.

$$R_B = 30\ \Omega$$

3. Code Implementation

Only NET-2 has provisions for directly implementing drain and source photocurrent generators in the MOS model itself. Each of the codes require manual changes in the threshold voltage parameter in order to simulate total dose effects. SPICE2 can only implement the double exponential form of the photocurrent generators and cannot implement the electrical overstress subroutine. Table IV-6 gives parameter values for implementing photocurrent equations in NET-2. Otherwise, all implementation parameters are identical to those given previously in table IV-4. The areas for the source and drain diffusions have been used to calculate IP11, IP12, IP21, and IP22 according to the scheme indicated below.

$$IP11 = 6.4 * 10^{-6} * W * A_S$$

$$(N^+P)\ IP11 = \underbrace{\left[6.4\times10^{-6}\ \frac{A}{\frac{rad(Si)*cm^3}{s}}\right]}_{qg}\underbrace{\left(2.43\times10^{-5}cm\right)}_{W}\underbrace{\left(2.2\times10^{-5}\ cm^2\right)}_{\text{Source Area}}\left(10\ \frac{ergs}{J}\right)$$

$$= 3.43 \times 10^{-8}\ \frac{coul}{J}$$

TABLE IV-6. NET-2 MOS MODEL PHOTOCURRENT IMPLEMENTATION

Code Parameter	Definition	NMOS Value	PMOS Value
IP11	Source Depletion Region Photocurrent Constant	$3.43 \times 10^{-8}\ \frac{pC}{pJ}$	$1.40 \times 10^{-7}\ \frac{pC}{pJ}$
IP12	Source Diffusion Region Photocurrent Constant	$45.6 \times 10^{-12}\ \frac{mA\ \ ns}{pJ}$	$59.4 \times 10^{-12}\ \frac{mA\ \ ns}{pJ}$
IP21	Drain Depletion Region Photocurrent Constant	$4.75 \times 10^{-8}\ \frac{pC}{pJ}$	$1.40 \times 10^{-7}\ \frac{pC}{pJ}$
IP22	Drain Diffusion Region Photocurrent Constant	$6.31 \times 10^{-12}\ \frac{mA\ \ ns}{pJ}$	$59.4 \times 10^{-12}\ \frac{mA\ \ ns}{pJ}$

$$10^{7} \frac{\text{ergs}}{\text{g}} = 5.08 \times 10^{-8} \frac{\text{coul}}{\text{J}}$$

$$(N^{+}P) \quad IP12 = 6.4 \times 10^{-6} \left(\frac{L * A_s}{\sqrt{t_{DR} - t_{DF}}} \right)$$

$$= 6.4 \times 10^{-6} \frac{5.1 \times 10^{-3} \times 2.21 \times 10^{-5} \times 10^{7}}{\sqrt{25 \text{ ns}}}$$

$$= 45.6 \times 10^{-12} \frac{\text{mA} \sqrt{\text{ns}}}{\text{pJ}}$$

9. Computer Examples

Three computer examples are provided below. Figure IV-36 presents a SPICE2 listing of the inverter examined previously, with a complete set of photocurrent generators. Figure IV-37 shows the results of exercising this inverter to determine propagation delays as a function of the threshold voltage shifts listed in table IV-5. See the SPICE2 listing in chapter IV.C for circuit description for propagation delay analysis. Figure IV-38 shows the low state photo response of the inverter at 1×10^{9}, 1×10^{10}, and 5×10^{10} rad (Si)/s. Note that at 1×10^{10} rad (Si)/s, significant secondary photocurrents have been generated by the parasitic transistor.

Figure IV-39 gives a SCEPTRE listing of the input protection network such as that shown previously in figure IV-31. The gates of the N-channel and P-channel transistors have been replaced with an equivalent capacitor. Table IV-7 gives the result of exercising this circuit for a variety of electrical overstress pulse amplitudes.

```
INVRTR PHOTOCURRENT RUNS

     INPUT LISTING                        TEMPERATURE =   27.[illegible] DEG C

**********************************************************************************

.MODEL NCHNL1 NMOS(VTO 1.[illegible]          KP [illegible]          RD .21
+                    RS .21          CBD 3.[illegible]          CBS 3.[illegible]
+                    CGSO [illegible]-13     CGDO [illegible]-12    CGBO 3.86E-12
+                    JS 9.3 E-12     PB .8)
.MODEL PCHNL1 PMOS(VTO -1.13         KP 3.[illegible]          RD .55
+                    RS .55          CBD 9.[illegible]          CBS [illegible]
+                    CGSO 6.[illegible]-13   CGDO 8.[illegible]-12    CGBO 8.86E-12
+                    JS 6.[illegible]    PB .8)
.MODEL DIODEPN D(CJO [illegible] PB .[illegible])
.MODEL DIODENPN D(CJO 3.[illegible] PB .[illegible])
.MODEL BPXSTR NPN(BF 100.     BR 1.[illegible]     IS [illegible].3E-12      CJE 3.[illegible]
+                    PE .9      CJC [illegible] PC .7      MC .333)
.SUBCKT INVRTR 1 2 3
MP1   4  2  [illegible]  PCHNL1 W=[illegible]MIL L=.197MIL AD=2.8[illegible] AS=2.8[illegible]
MN1   3  2 11 1  NCHNL1 W=[illegible].71MIL L=.197MIL AD=1.9[illegible]-6 AS=2.[illegible]
QDON1 1 8    5 BPXSTR AREA=2.87E-5
RZON1 [illegible] 8[illegible] 33K
DPIN      2 1 DIODEPN AREA=[illegible]-6
DPOUT     3 1 DIODEPN AREA=[illegible]-6
DPDP1     7 1 DIODEPN AREA=3.[illegible]-5
CMIN      2       .[illegible]PF
CMOUT     3       .[illegible]PF
RPSP1     1   4 [illegible]
RPBP1     1   [illegible] .1
RPDP11    6   7 3.[illegible]
RPDP12    7   [illegible] [illegible]
RPDN11    3   8 1.[illegible]
RPDN12    8   9 1.[illegible]
RPBN1     1[illegible]      .1
RPSN1     1[illegible]    [illegible]
.ENDS
X1 2 4 5      INVRTR
VDD 1 [illegible] DC [illegible]
RDD 1 2 1
VIN 3 [illegible] PULSE([illegible]NS [illegible]NS [illegible]NS [illegible]US)
RIN 3 4 [illegible]K
CO 5 [illegible] [illegible]PF
.TRAN 4NS [illegible]
.PLOT TRAN V([illegible])
.END
```

Figure IV-36. SPICE2 Listing of Inverter Circuit with Photocurrent Generators

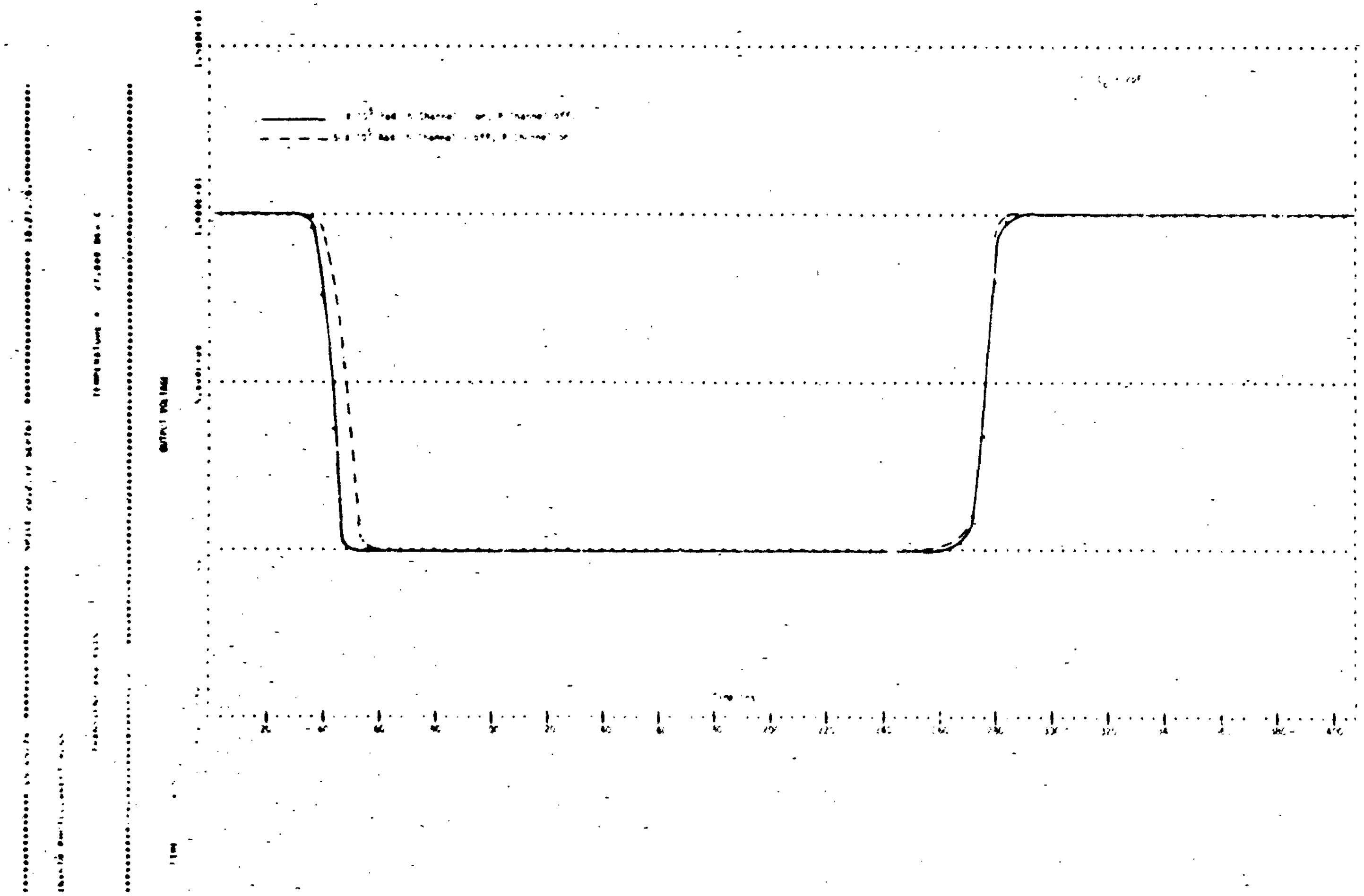


Figure IV-37. Inverter Propagation Delay for Different Values of Threshold Voltage Shift

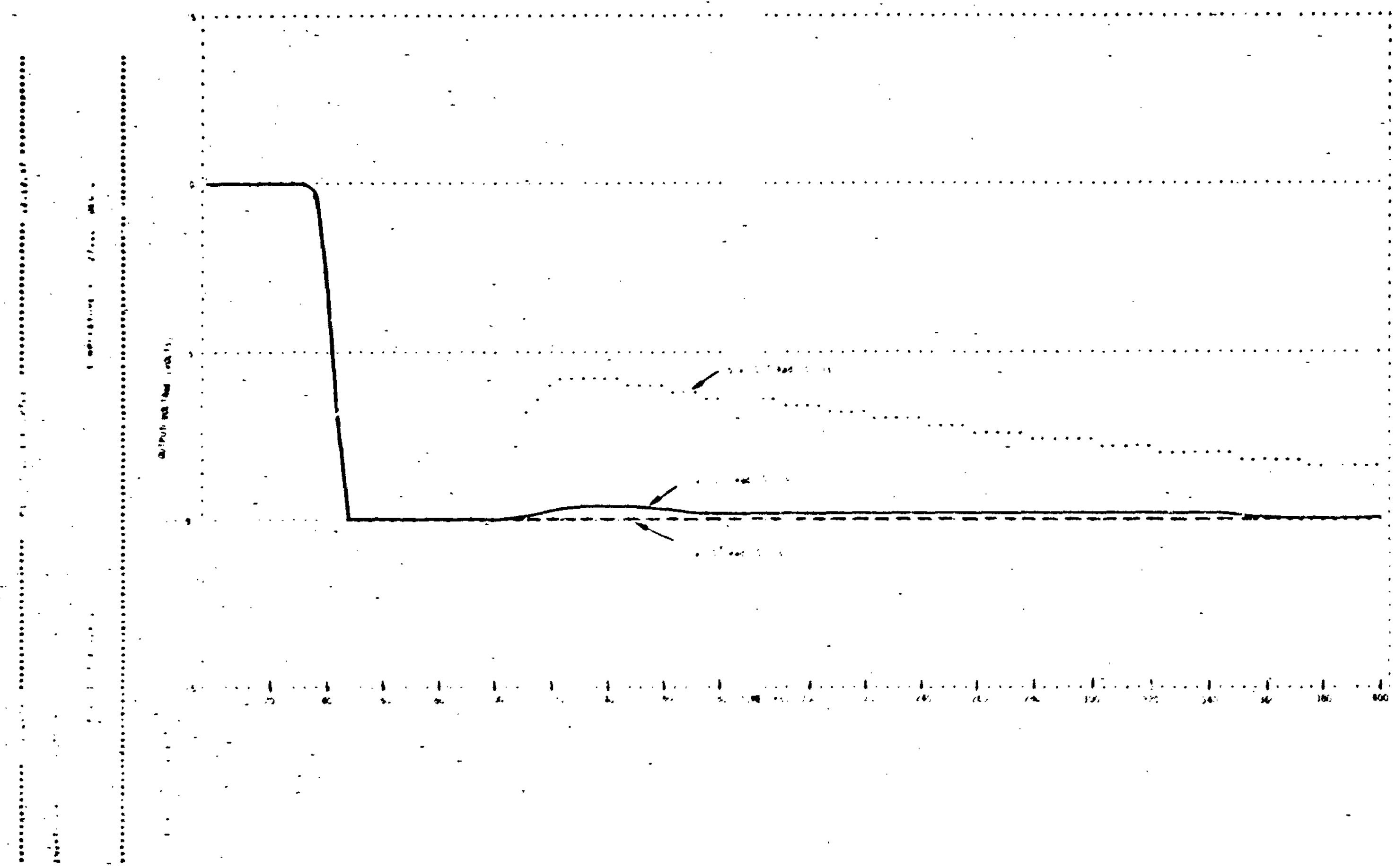


Figure IV-38. SPICE2 Analysis of Inverter Low State Photoresponse

```
MODEL  EAT PIN TO NSUB (A-C)
THIS MODEL REPRESENTS THE PORTION OF THE DISTRIBUTED DIODE/RESISTOR
      ATTACHED TO THE EXTERNAL CONNECTION.
UNITS [illegible]
    ELEMENTS
         [illegible]
         [illegible]
         [illegible]
         [illegible]
    DEFINED PARAMETERS
         [illegible] = 0.
         [illegible] = 0.
         [illegible]
         [illegible]
         [illegible]
         [illegible]
         [illegible]
         [illegible]
    FUNCTIONS
         [illegible]
         [illegible]
RCA CONSTANT MULTIPLEXER
INPUT PROTECTION NETWORK
EMP OVERSTRESS RESPONSE
    UNITS [illegible]
    ELEMENTS
         [illegible]
         [illegible]
         [illegible]
         [illegible]
         [illegible] MODEL  EAT PIN TO NSUB
         [illegible]
         [illegible] MODEL  EAT PIN TO NSUB
         [illegible] MODEL [illegible]
         [illegible]
    DEFINED PARAMETERS
         [illegible]
         [illegible]
    OUTPUTS
         [illegible],PLOT
         VOIN,PLOT
         [illegible],PLOT
         [illegible],PLOT
         [illegible],PLOT
         [illegible],PLOT
         [illegible],PLOT
         [illegible],PLOT
         [illegible],PLOT
         [illegible],PLOT
    FUNCTIONS
         TABLE [illegible]
         [illegible]
    INITIAL CONDITIONS
         [illegible]
         [illegible]
    RUN CONTROLS
         INTEGRATION ROUTINE = IMPLICIT
         NO OVERFLOW [illegible]
         STOP TIME = [illegible]
         TERMINATE [illegible]
         TERMINATE [illegible]
         TERMINATE [illegible]
         TERMINATE [illegible]
         TERMINATE [illegible]
         TERMINATE [illegible]
         TERMINATE [illegible]
```

Figure IV-39. SCEPTRE Listing for Input Protection Network Electrical Overstress Analysis

TABLE IV-7. SCEPTRE ELECTRICAL OVERSTRESS ANALYSIS OF CMOS INPUT PROTECTION NETWORK

INPUT NETWORK ELECTRICAL OVERSTRESS FAILURE PREDICTIONS

		ELEMENT		TERMINAL		
FAILED ELEMENT	FAIL TIME	THRESHOLD POWER	FAIL POWER	FAIL VOLT	FAIL POWER	OPEN CIRCUIT VOLTAGE
D3 (REVERSE)	7.00 μs	9.6	9.81	-165.0	17.3	-170
D3 (REVERSE)	1.60 μs	20.4	20.80	-166.0	27.9	-175
D3 (REVERSE)	0.72 μs	30.7	32.10	-168.5	38.7	-180
D3 (REVERSE)	0.38 μs	42.1	43.70	-170.0	49.8	-185
D3 (REVERSE)	0.29 μs	48.0	55.40	-172.0	61.2	-190
D3 (FORWARD)	3.10 μs	91.3	91.40	63.0	110.0	+150
D3 (FORWARD)	2.40 μs	168.0	168.00	81.6	193.0	+200
D3 (FORWARD)	0.98	263.0	268.00	100.0	300.0	+250
D3 (FORWARD)	0.51	365.0	391.00	119.0	430.0	+300
D3 (FORWARD)	0.30	471.0	537.00	137.0	584.0	+350

E. MOS MODELS INCLUDING SECOND ORDER EFFECTS

1. Description

The first order MOS model discussed in section B of this chapter is primarily useful for simulating the I/V characteristics of an individual MOS transistor. The threshold voltage and the transconductance factor are measured and used in the model equations to match the experimental data. This model can be useful in predicting circuit response from knowledge of electrical characteristics of individual pieceparts. However, there are two major limitations associated with the first order model. First, the analyst is often unable to measure the threshold voltage and transconductance factor of individual transistors. They may be inaccessible due to their location within an integrated circuit, or they may be in the design stage and the analyst may be interested in parametric trade-off studies before finalizing the design. For these cases, the analyst requires a model which he can parameterize from a physical description of the device in terms of doping concentrations, oxide thicknesses, etc. Such a model must provide reasonably accurate predictions of individual transistor characteristics if it is to be useful.

The other difficulty with the first order model is its unsophisticated functional form. Its mathematical construction is not sufficient to accurately represent the actual I/V characteristics of four terminal MOS devices. The so called second order effects which are responsible for the deviation of MOS characteristics from the simple theory represented by first order model are of major importance for the small geometry transistors found in integrated circuits. Failure to account for these second order effects can result in gross inaccuracies in prediction of integrated circuit response.

In this chapter, second order MOS models are discussed which are parameterized from physical data related to the fabrication process.

The discussion includes the following:

(1) Substrate Bias Effects

(2) Two-Dimensional Effects on Threshold Voltage

(3) Weak Inversion Effects

(4) Channel Length Modulation Effects

(5) Variable Mobility Effects

(6) Temperature Effects

All of these effects are not included in all of the models. The discussion will indicate how the effects are implemented and what parameters the analyst must supply to use them effectively. In general, the SCEPTRE/TRAC/CIRCUS2 subroutine (referred to as the SCEPTRE model) and the SPICE2 built-in model contain quite complete second order effects. The built-in NET-2 model remains an essentially empirical model with some provisions for including second order effects through increased mathematical sophistication. Example computer solutions have been included to demonstrate the modifications in I/V characteristics resulting from varying the value of parameters associated with each of the second order effects. The analyst should use these examples to determine if his problem requires modeling a particular effect.

2. Advantages

The functional form of the second order models are much more representative of MOS transistor behavior than the first order model. They will generally support analysis over a much greater range of forcing currents and voltages than the first order models. This is especially true for the small geometry transistors used in MOS medium and large scale integrated circuits.

3. Cautions

As models become more sophisticated, the analyst finds it increasingly difficult to retain a grasp of the interactions of all the model parameters. This is especially the case for very flexible models such as the one found in SPICE2. That model permits the analyst to either input certain second order effect parameters or to allow the code

to calculate them from basic physical data. Extreme caution must be exercised to insure that parameters are specified in a consistent manner. For example, if the analyst specifies KP, the intrinsic transconductance, in the SPICE2 model he will override any value for mobility which he may specify later in the parameter list. This potential for inconsistent parameterization increases the importance of exercising the models in "curve tracer" runs before using them in circuit analyses. Only by looking at the I/V characteristics in a format where he knows what to expect can the analyst insure that the model is parameterized properly.

4. Characteristics

a. Topology

Figure IV-40 shows the topology of the SPICE2 model for an N-channel transistor. Note that this is the same topology as used in previous sections of this chapter. The second order effects modeling is primarily concerned with the functional form of the drain current generator. Therefore, no topological variations are required.

b. Typical Effects

1) Substrate Bias

MOS transistors are actually four terminal devices. As a result, a reverse biasing potential can appear between the source and substrate. The use of MOS transistors as transmission gates is an application where the source and substrate are typically at different potentials. The result of reverse biasing drain to source voltage is to increase the amount of charge stored in the depletion region. Consequently, the drain current decreases for a fixed gate voltage. Figure IV-41 shows a qualitative representation of this effect.

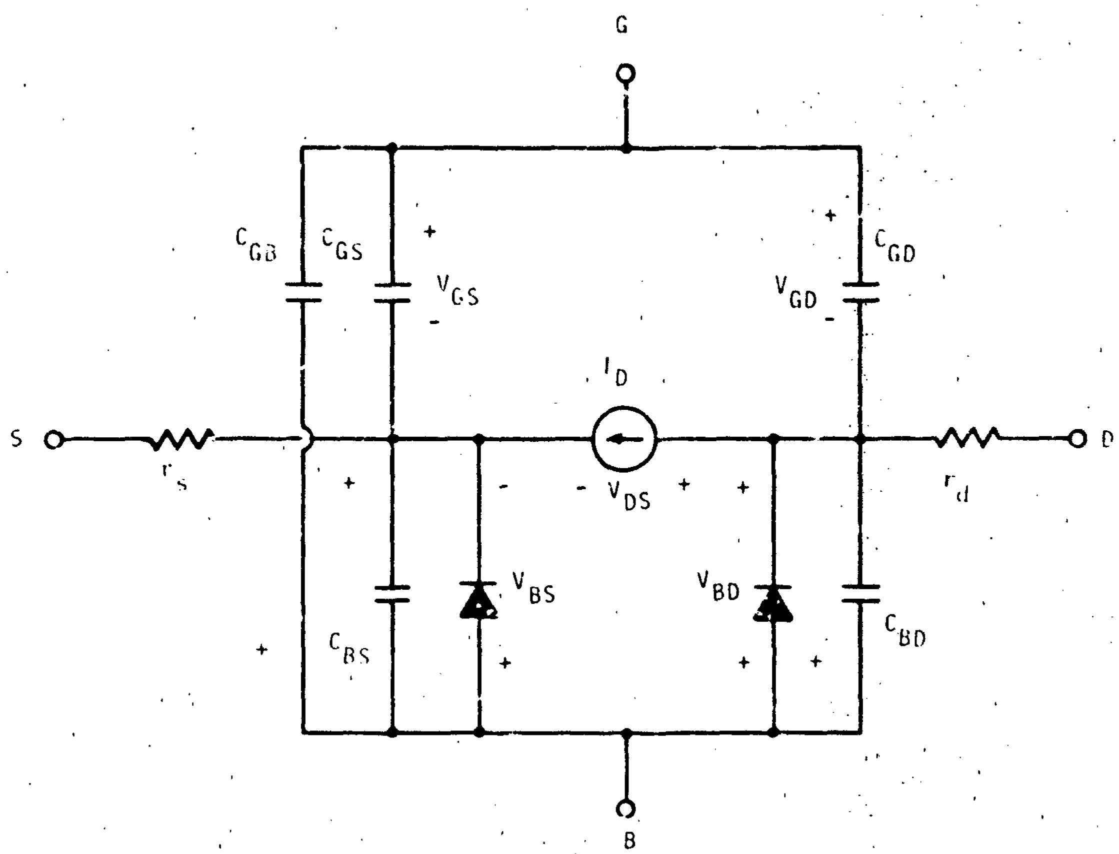


Figure IV-40. SPICL2 MOSFET Model

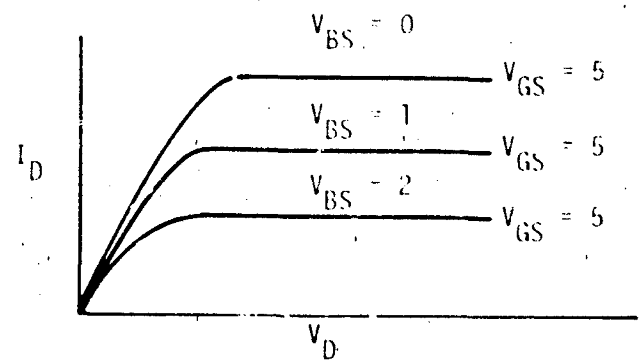


Figure IV-41. Substrate Bias Effects on Drain Current at a Fixed Gate Voltage

The SCEPTRE and SPICE2 second order models include substrate bias effects on the drain current; however the NET-2 model does not.

2) Two-Dimensional Effects on Threshold Voltage

As the channel length of an MOS transistor is shortened to less than approximately 5 μm, the amount of depletion layer charge which is effective in terminating the E-field lines due to the gate-substrate potential is significantly decreased. The result is a lower threshold voltage and a modified turn-on characteristic compared to that normally predicted. This effect can best be observed by comparing the characteristics of transistors with the same width to length ratios but different channel lengths. Figure IV-42 shows a qualitative example of the two-dimensional effect on threshold voltage. Only the SPICE2 model incorporates this effect.

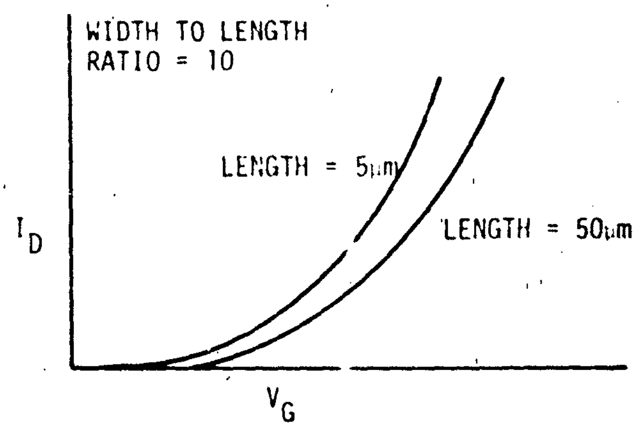


Figure IV-42. Two Dimensional Effects on Threshold Voltage

3) Weak Inversion Effects

Most first order models assume that drain-to-source conduction begins abruptly once the gate-to-source threshold voltage is reached. In reality, conduction begins below the threshold voltage and increases exponentially until it intersects the drain current predicted by the first order theory. Proper simulation of current in the weak inversion region below the threshold voltage can be of significant importance in modeling devices which have been subjected to ionizing radiation with a resulting increase in the surface state density. The SPICE2 model contains weak inversion effects explicitly within the model. Figure IV-43 shows a qualitative example of the weak inversion effect on the turn on characteristic of a MOS transistor.

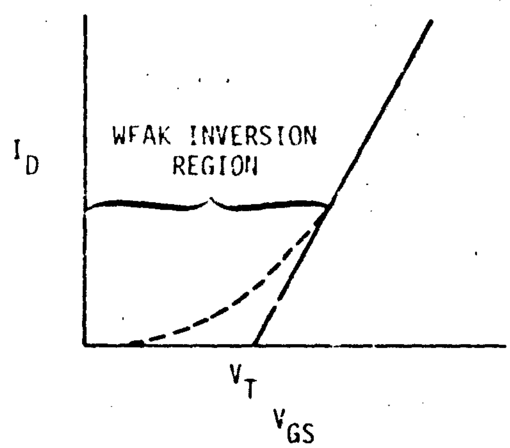


Figure IV-43. Weak Inversion Effects on Turn on Characteristic

4) Channel Length Modulation Effects

MOS transistors with relatively short channel lengths (< 10 μm) often exhibit finite drain-to-source conductance (i.e., an imperfect saturation characteristic) for drain-to-source voltages exceeding pinchoff. This is primarily due to the spread of the drain depletion region into the channel with a subsequent shortening of the effective channel length. Figures IV-44 and IV-45 illustrate the spread of the depletion region and its affect on drain characteristics. The SCEPTRE, NET-2, and SPICE2 models all contain provisions for modeling finite conductance in saturation. Each uses a different technique for implementing the effect.

5) Variable Mobility Effects

The surface mobility (μ_s) which is a factor in the transconductance term (β) is a function of the applied voltage. The value of μ_s increases to its maximum value when the gate voltage approaches the threshold voltage. Thereafter, it decreases with increasing gate-to-source, drain-to-source, and substrate-to-source voltage. Its maximum value is always less than the mobility in bulk silicon. The result of

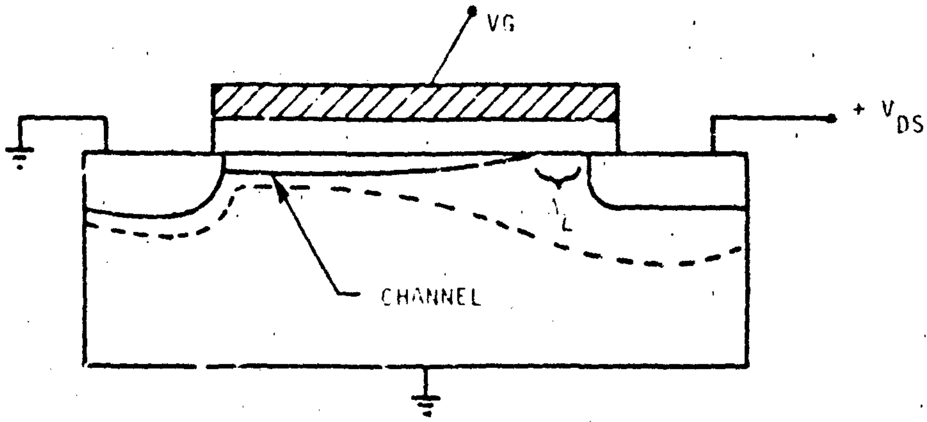


Figure IV-44. Schematic Representation of Channel Length Modulation

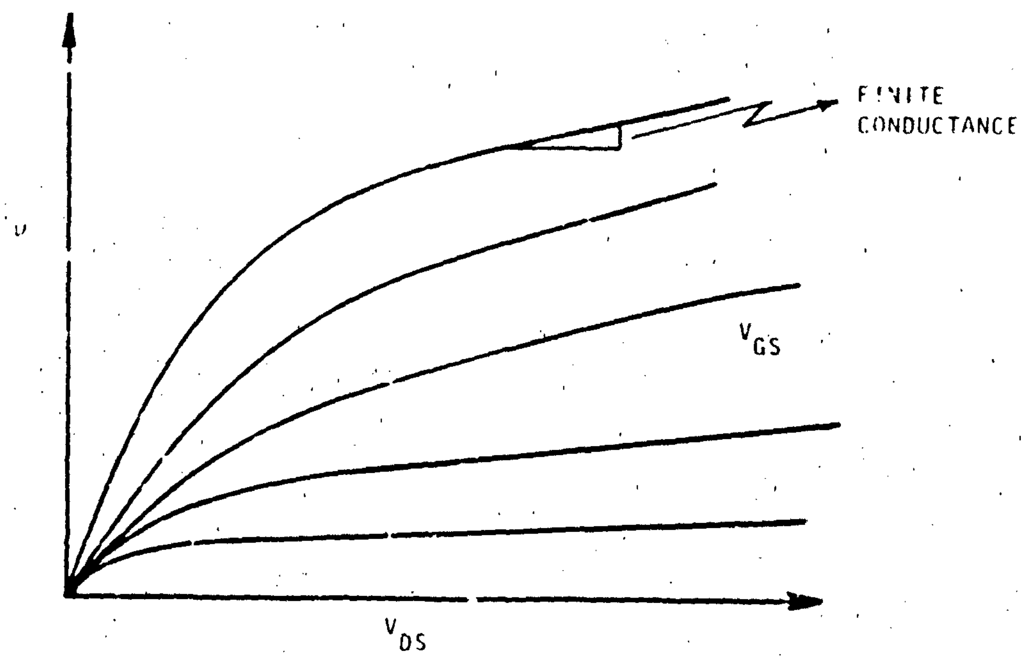


Figure IV-45. Finite Saturation Conductance Due to Channel Length Modulation

the decreased mobility is a decrease in drain current with gate voltage at the higher values of gate voltage. This effect is illustrated qualitatively in figure IV-46. The SCEPTRE, NET-2, and SPICE2 models incorporate variable mobility effects although different implementation approaches are used.

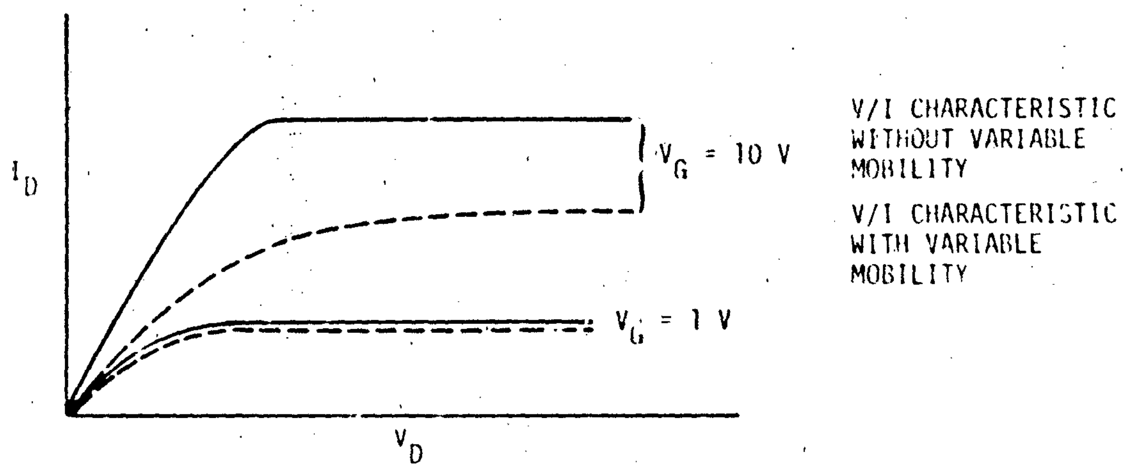


Figure IV-46. Variable Mobility Effects

6) <u>Temperature Effects</u>

Temperature variations affect many of the physical parameters used in the second order model. These include the Fermi level and several terms which are multiplied by the factor KT/q. For silicon gate devices, the silicon gate work function must also be varied with temperature. The SPICE2 model provides automatic updating of appropriate model parameters with temperature. This must be accomplished manually in the SCEPTRE model. Figure IV-47 qualitatively illustrates the effect of temperature on MOS transistor turn-on characteristics.

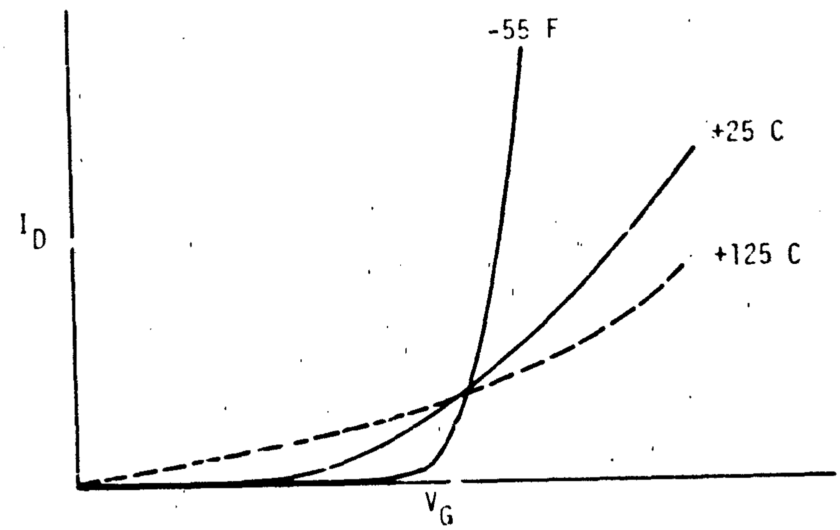


Figure IV-47. Temperature Effects on MOS Turn-On Characteristics

5. Defining Equations

a. Substrate Bias (SCEPTRE and SPICE2)

$$V_{FB} = \phi_{MS} - \frac{Q_{SS}}{C_{OX}} = \phi_m - \phi_{so} + \frac{Eg}{2q} - \phi_F - \frac{Q_{SS}}{C_{OX}}$$

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_B (2\phi_f - V_{BS})}}{C_{OX}}$$

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}} \; ; \; \phi_f = \frac{KT}{q} \ln \frac{NB}{n_i} \text{ or } \frac{KT}{q} \ln \frac{n_i}{N_B}$$

$$I_{DS} = \frac{\mu_s C_{OX} W}{L} \left[V_{DS} \left(V_{GS} - 2\phi_F - V_{FB} - \frac{V_{DS}}{2} \right) \pm \left(-\frac{2}{3} \right) \frac{\sqrt{2\varepsilon_s q N_B}}{C_{OX}} \right.$$

$$\left. (V_{DS} + 2\phi_F - V_{BS})^{3/2} - (2\phi_F - V_{BS})^{3/2} \right]$$

where (-) applies for N-Channel; (+) applies for P-Channel.

b. Two Dimensional Effects on Threshold Voltage (SPICE2 only)

$$V_T = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_B}}{C_{OX}} f(V_{BS}) \sqrt{2\phi_F - V_{BS}}$$

$$I_{DS} = \frac{\mu_s C_{OX} W}{L} \left\{ V_{DS}\left(V_{GS} - 2\phi_F - V_{FB} - \frac{V_{DS}}{2}\right) \pm \frac{2}{3} \frac{\sqrt{2\varepsilon_s q N_B}}{C_{OX}} f(V_{BS}) \left[(V_{DS} + 2\phi_F - V_{BS})^{3/2} - (2\phi_F - V_{BS})^{3/2} \right] \right\}$$

where:

$$f(V_{BS}) = 1 - \frac{x_j}{L}\left(1 + \sqrt{\frac{2x_d}{x_j}} - 1\right)$$

$$X_d = \sqrt{\frac{2\varepsilon_s}{qN_B}(2\phi_F - V_{BS})}$$

c. Weak Inversion Effects (SPICE2 only)

$$V_{ON} = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_B}}{C_{OX}} f(V_{BS}) \sqrt{2\phi_F - V_{BS}} + \frac{KT}{q}\left[1 + \frac{qN_{FS}}{C_{OX}} + \frac{f(V_{BS})\sqrt{2\varepsilon_s q N_B}}{2C_{OX}\sqrt{2\phi_F - V_{BS}}}\right]$$

for $V_{GS} < V_{ON}$

$$I_D = \frac{\mu_s C_{OX} W}{L} \left\{ \left(V_{ON} - V_{FB} - 2\phi_F - \frac{V_{DS}}{2}\right) V_{DS} - \frac{2}{3} \frac{\sqrt{2\varepsilon_s q N_B}}{C_{OX}} f(V_{BS}) \, (2\phi_F - V_{BS} + V_{DS})^{3/2} - (2\phi_F - V_{BS})^{3/2} \right\} *$$

$$\exp\left\{ \frac{(V_{GS} - V_{ON}) \; V_{DS}}{V_{ON} - V_{FB} - 2\phi_F - \frac{V_{DS}}{2} - \frac{2}{3}\frac{\sqrt{2\varepsilon q N_B}}{C_{OX}} f(V_{BS}) \left[(2\phi_F - V_{BS} + V_{DS})^{3/2} - (2\phi_F - V_{BS})^{3/2} \right]} \right\}$$

d. Channel Length Modulation Effects (SCEPTRE, SPICE2, NET-2)

For $V_D > V_P$:

(1) SCEPTRE Model

$$I_{DSAT} = \frac{I_P L}{L - \Delta L}$$

$$L = f(I_{DSAT}, E_C) \sqrt{\frac{2\varepsilon_s}{qN_B}} \quad (V_{DS} - V_P)$$

$$f(I_{DSAT}, E_C) = -K_1 \frac{\left[E_C L (V_{DS} - V_P)^{-\frac{1}{2}} + (V_D - V_P)\right]^{\frac{1}{2}}}{L(1+K_2 I_P) - K_1 E_C}$$

$$+ \frac{1}{2}\left\{ K_1^2 \frac{\left[E_C L (V_D - V_P)^{-\frac{1}{2}} + (V_D - V_P)^{\frac{1}{2}}\right]^2}{\left[L\,(1 + K_2 I_P) \quad K_1 E_C\right]^2}\right.$$

$$\left. + \frac{4L}{L\,(1 + K_2 I_P) - K_1 E_C}\right\}^{\frac{1}{2}}$$

$$K_1 = \left(\frac{2\varepsilon_{si}}{qN_B}\right)^{\frac{1}{2}} ; \quad K_2 = \frac{2}{qNWX_e V_L}$$

$$X_E = \frac{x_j}{\ell n\left(\frac{x_j}{x_c}\right) - 1}$$

$$V_P = \left(V_G - V_{FB} - 2\phi_F - \frac{I_P}{\beta E_C L}\right) + \frac{\phi^2}{2} \pm \phi \sqrt{V_G - V_{FB} - \frac{I_P}{\beta E_C L} \pm \frac{\phi^2}{4}}$$

where the upper sign is valid for N-channel devices and the lower sign is valid for P-channel devices.

$$\Phi = \frac{1}{C_{OX}} \quad 2\varepsilon_s q N_B$$

$$\beta = \frac{\mu_s W C_{OX}}{L}$$

$$I_P = \beta\left(\left(V_G - V_{FB} - 2\phi_F \pm \frac{\phi^2}{2} \pm \phi \sqrt{\left|V_G \quad V_{FB} \pm \frac{\phi^2}{4}\right|}\right)\right)\left[V_G - 2\phi_F - V_{FB}\right.$$

$$\left. - \frac{\left(V_G - V_{FB} - 2\phi_F \pm \frac{\phi^2}{2} \pm \phi \sqrt{\left|V_G - V_{FB} \pm \frac{\phi^2}{4}\right|}\right)}{2}\right] + \frac{2}{3}\phi$$

$$* \left\{ \left[\left(V_G - V_{FB} - 2\phi_F \pm \frac{\phi^2}{2} \pm \phi + \sqrt{\left|V_G - V_{FB} \pm \frac{\phi^2}{4}\right|}\right)\right.\right.$$

$$\left.\left. + 2\phi_F - V_{BS}\right|^{3/2} \left(2\phi_F - V_{BS}\right)^{3/2} \right\}\Bigg)$$

The SCEPTRE model equations account for the effect of the mobile carriers in the channel on the spread of the depletion region. This prevents the premature prediction of punch through of the depletion region from the source to drain.

(2) SPICE2 Model

$$I_{DSAT} = I_D \frac{L}{L-\Delta L}$$

$$L = \underbrace{\sqrt{\frac{2\varepsilon_{si}}{qN_B}}}_{\text{Term 1}} \underbrace{\sqrt{\frac{V_{DS}-V_{DSAT}}{4} + \left[1 + \left(\frac{V_{DS}-V_{DSAT}}{4}\right)^2\right]^{1/2}}}_{\text{Term 2}}$$

$$\text{LAMBDA} = \frac{\Delta L}{L_0 V_{DS}} \cdot \frac{1}{1-\lambda V_{DS}} = \frac{L_0}{L_0 - \Delta_L}$$

$$V_{DSAT} = V_{GS} - V_{FB} - 2\phi_F + \frac{\varepsilon_s q N_B}{C_{OX}^2} f^2(V_{BS})$$

$$\left[1 - \sqrt{1 + \frac{2C_{OX}^2}{\varepsilon_s q N_B}\left(V_{GS} - V_{FB} - 2\phi_F - V_{BS}\right)}\right]$$

$$I_{DSAT} = \left(\frac{1}{1-\lambda V_{DS}}\right) \beta \left\{ \left(V_{GS} - V_{FB} - 2\phi_F - \frac{V_{DSAT}}{2}\right) V_{DSAT} - \frac{2}{3} \sqrt{\frac{2\varepsilon_s q N_B}{C_{OX}}} \right.$$

$$\left. \cdot \left[(2\phi_F + V_{DSAT} - V_{BS})^{3/2} - (2\phi_F - V_{BS})^{3/2}\right] \right\}$$

Note that term 2 in the L equation has a functional form which was chosen to insure a smooth transition in current between linear and saturated regions of operation. For values of V_{DS} approaching zero and small values of V_{DSAT} ($V_{DSAT} = V_{GS} - V_T$), a significant value of L can be calculated from this functional form. This is not physical, and such areas should be examined carefully by the analyst.

(3) NET-2 Model

$$I_{DSAT} = V_p \left[A_1 + A_2 \sqrt{V_p} + A_3 V_p + V_{GS}(A_4 + A_5 V_{GS})\right]$$

$$+ \left(V_{DS} - V_p\right)\left(K_1 + K_2 V_{GS} + K_3 V_{GS}^2\right)$$

The term $(K_1 + K_2V_{GS} + K_3V_{GS}^2)$ is equivalent to a drain saturation conductance. Physically, the saturated drain conductance can be written as:

$$g_{DSAT} = \frac{I_{DSAT}\sqrt{\frac{2\varepsilon_s}{qN_B}}\quad L}{2(L - \Delta L)^2\ (V_D - V_{DSAT})^{\frac{1}{2}}}$$

$$I_{DSAT} = \frac{\beta}{2}\ (V_{GS} - V_T)^2 = \frac{\beta}{2}\ (V_{GS}^2 - 2V_{GS}V_T + V_T^2)$$

$$\Delta L = \sqrt{\frac{2\varepsilon_s}{qN_B}\ (V_D - V_{DSAT})}$$

$$K_1 = \frac{\beta L\sqrt{\frac{2\varepsilon_s}{qN_B}}\quad V_T^2}{8(L - \Delta L)^2\ (V_D - V_{DSAT})^{\frac{1}{2}}}$$

$$K_2 = \frac{-\beta L\sqrt{\frac{2\varepsilon_s}{qN_B}}\quad V_T}{4(L - \Delta L)^2\ (V_D - V_{DSAT})^{\frac{1}{2}}}$$

$$K_3 = \frac{\beta L\sqrt{\frac{2\varepsilon_s}{qN_B}}}{8(L - \Delta L)^2\ (V_D - V_{DSAT})^{\frac{1}{2}}}$$

Although these constants can be calculated, the analyst may wish to use only K_1 if a constant value of saturated conductance is sufficiently accurate over the operating region of interest. If experimental data are available, K_1, K_2, and K_3 may be selected to fit the data. NET-2 contains curve fitting routines for determining values for all model constants if the user provides experimental values for V_{GS}, V_{DS}, and I_D in the vicinity of the transition from triode to saturated operation.

e. Variable Mobility Effects

(1) SCEPTRE Model

$$\frac{\mu_s}{\mu_o} = \frac{V_L}{V_L + \mu_o E_s}$$

$$\beta = \frac{\beta_o}{\left[1 + \frac{C_{OX}}{2\varepsilon_s E_{SC}}\left(V_G - V_{FB} - 2\phi_F + \sqrt{\frac{2\varepsilon_s q N_B}{C_{OX}}}\sqrt{2\phi_F - V_{BS}}\right)\right]}$$

This reflects the voltage drop along the channel.

(2) SPICE2 Model

$$\mu_s = \mu_o\left[\frac{U_{CRIT}\,\varepsilon_s}{C_{OX}\,(V_{GS} - V_{ON} - U_{TRA}V_{DS})}\right]^{U_{EXP}}$$

$$\beta = \frac{WC_{OX}\mu_s}{L}$$

(3) NET-2 Model

The triode region equation for drain current in NET-2 is:

$$I_D = V_{DS}\left[A_1 + A_2\sqrt{V_{DS}} + A_3V_{DS} + V_{GS}(A_4 + A_5V_{GS})\right]$$

The coefficient A_4 is the transconductance factor and is of primary importance in determining the drain current as a function of gate voltage. If A_5 has a negative value, it can be used to reduce the transconductance as a function of gate and drain voltage. This is a purely empirical approach to simulating the effects of mobility degradation. Therefore, the analyst should have experimental data available before attempting to use this portion of the NET-2 model.

f. Temperature Effects (SPICE2 only)

$$V_{ON} = \phi_m - \phi_{so} - \frac{E_g}{2q} - \phi_F - \frac{Q_{SS}}{C_{OX}} + 2\phi_F + \sqrt{\frac{2\varepsilon_s q N_B}{C_{OX}}}\; f(V_{BS})$$

$$+ \frac{KT}{q}\left(1 + \frac{qN_{FS}}{C_{OX}} + \frac{\sqrt{2\varepsilon_s q N_B}}{C_{OX}} \quad f(V_{BS})\sqrt{\frac{1}{2\phi_f \quad V_{BS}}}\right)$$

$$\phi_f = \frac{KT}{q}\, \ell n\, \frac{n_i}{N_B} \quad \text{or} \quad \frac{KT}{q}\, \ell n\, \frac{N_B}{n_i}$$

$$n_i - 3.86 \times 10^{16}\, T^{3/2} \exp\left(-\frac{Eg}{2KT}\right)$$

For aluminum metal gate devices, $\phi_m \approx 3.2$ V; for silicon gate devices,

$$\phi_m = \phi_{so} + \frac{E_g}{2q} + \phi_F$$

The variations in V_{ON} with temperature are made automatically in SPICE2 for whatever temperature is specified by the analyst. Similar parametric variations can be made in the SCEPTRE model, but they must be made manually.

6. Parameter List

C_{OX}	=	oxide capacitance (farad)
t_{OX}	=	oxide thickness (cm)
L	=	channel length (the spacing between source and drain) (cm)
W	=	channel width (the drain or source dimension perpendicular to the channel length) (cm)
ϕ_m	=	gate - SiO_2 work function (3.2 V)
ϕ_{sox}	=	Si - SiO_2 work function
ϕ_{so}	=	potential difference between the bottom of the SiO_2 conduction band and the bottom of the SiO_2 conduction band (3.25 V)
Eg/2q	=	intrinsic Fermi potential ($\approx$ .56 V)

ϕ_F = Fermi level (volt)

n_i = intrinsic carrier concentration (cm^{-3})

N_B = substrate doping concentration (cm^{-3})

V_{FB} = flat band voltage (volt)

ϵ_{OX} = permittivity of silicon dixoide (3.54×10^{-13} F/cm)

ϵ_s = permittivity of silicon (1.05×10^{-12} F/cm)

q = electronic charge (1.6×10^{-19} coulombs)

X_j = drain junction depth

X_d = depletion layer width

N_{FS} = surface state density (cm^{-2})

KT/q = 0.26 V at 27°C

Ec = critical E field intensity for the onset of space charge limited velocity effects

Xc = channel depth

V_p = pinchoff voltage (P-channel)

V_L = space charge limited velocity = 6×10^7 cm/s (N-channel)
= 3×10^7 cm/s (P-channel)

μ_s = surface mobility (cm^2/V-s)

μ_o = maximum surface mobility = 805 cm^2/V-s (N-channel)
= 156 cm^2/V-s (P-channel)

Es = surface E field intensity

U_{CRIT} = surface E field required for onset of variable mobility effects in SPICE2

U_{TRA} = transverse field coefficient for variable mobility effects in SPICE2

U_{EXP} = mobility variation exponent in SPICE2

7. Parameterization

Each of the major second order effects are parameterized in the following subsections. The parameterization is accomplished from the following physical characteristics for the N-channel and P-channel transistors. The parameters given in table IV-8 will be used to calculate

TABLE IV-8. MOS MODEL PARAMETER VALUES

PHYSICAL PARAMETER	N-CHANNEL VALUE	P-CHANNEL VALUE
t_{OX}	7×10^{-6} cm	7×10^{-6} cm
N_{SS}	1×10^{11} cm^{-2}	1×10^{11} cm^{-2}
N_{FS}	1×10^{11} cm^{-2}	1×10^{11} cm^{-2}
ϕ_M	3.2 V	3.2 V
ϕ_{SO}	3.25 V	3.25 V
Eg	.56 V	.56 V
n_i (27°C)	1.45×10^{10} cm^{-3}	1.45×10^{10} cm^{-3}
N_B	2×10^{16} cm^{-3}	2×10^{15} cm^{-3}
KT/q (27°C)	.026 V	.026 V
x_j	2×10^{-4} cm	2×10^{-4} cm
L	5×10^{-4} cm	5×10^{-4} cm
W	5×10^{-3} cm	5×10^{-3} cm
ϵ_{OX}	3.54×10^{-13} F/cm	3.54×10^{-13} F/cm
ϵ_s	1.05×10^{-12} F/cm	1.05×10^{-12} F/cm
E_c	7.45×10^{4} V/cm	1.81×10^{5} V/cm
X_c	1×10^{-6} cm	1×10^{-6} cm
μ_o	805 cm^2/V-s	166 cm^2/V-s
U_{CRIT}	1×10^{4} V/cm	1×10^{4} V/cm
U_{EXP}	.100	.242
U_{TRA}	300	.300

model variables for transistors representing an aluminum gate CMOS process which yields devices which can operate with supply voltages (V_{DD}) between 5 and 15 V.

a. Substrate Bias Effects

The second order models for SCEPTRE and SPICE2 do not require the specification of the threshold voltage. In fact, the analyst should not specify the parameter VTO in SPICE2 if he specifies the substrate doping parameter (NSUB). However, the analyst must calculate some parameters related to threshold voltage for the SCEPTRE model and he may find it useful to continue the calculation for the complete threshold voltage to serve as a check on the model for both SCEPTRE and SPICE2. NET-2 does not contain provisions for modeling substrate bias in the drain-source current. However, the effect of threshold voltage variation for fixed values of substrate source voltage can be accounted for in the parameter A_1. The reader is referred to chapter IV.E.5.b for the relationship of the following calculations to the model parameters.

1) Transconductance Factor

N-Channel Value

$$\frac{\mu_s C_{OX} W}{L} \qquad \frac{805 \times 5.06 \times 10^{-8} \times 5 \times 10^{-3}}{5 \times 10^{-4}} = 4.07 \times 10^{-4}$$

P-Channel Value

$$\frac{166 \times 5.06 \times 10^{-8} \times 5\ 10^{-3}}{5 \times 10^{-4}} = 8.40 \times 10^{-5*}$$

*μ_s is set equal to μ_o for these calculations

The SCEPTRE MOS model parameter is:

$$BO = \frac{\mu_o C_{OX} W}{L}$$

The SPICE2 MOS model parameter is:

$$KP = \mu_o C_{OX}$$

In SPICE2, specification of K_p will override subsequent specifications of variable mobility parameters. The analyst should not specify K_p when working with the second order model in SPICE2.

The NET-2 transconductance parameters are:

$$A_4 = \frac{\mu_s C_{OX} W}{2L}$$

$$A_3 = -\frac{1}{4}\ \frac{\mu_s C_{OX} W}{L}$$

2) Bulk Threshold Parameter

	N-Channel Value	P-Channel Value
$\frac{\sqrt{2\epsilon_s q N_B}}{C_{OX}}$	1.62	.52

The SCEPTRE MOS model parameter is:

$$PHI = \frac{|\phi_F| \sqrt{2\epsilon_s q N_B}}{\phi_F\ C_{OX}}$$

The SPICE MOS model parameter is:

$$GAMMA = \frac{\sqrt{2\epsilon_s q N_B}}{C_{OX}}$$

The GAMMA value will be automatically calculated by SPICE2 if values for the N_B and t_{OX} parameters are provided by the analyst. Therefore, a separate value for GAMMA should be entered only if the indicated calculation procedure is not acceptable.

The NET-2 MOS model parameter is:

$$A_2 = \frac{\frac{\beta}{2}\sqrt{2\varepsilon_s q N_B}}{C_{OX}}$$

Note that A_2 only multiplies V_{DS} in the NET-2 mode and does not produce variations in drain current or threshold voltage with V_{BS}.

3) Fermi Potential

	N-Channel Value	P-Channel Value
$2\phi_F$	$2 \times .026 \ \ln\left(\frac{2 \times 10^{16}}{1.45 \times 10^{10}}\right) = .735$	$2 \times .026 \ \ln\left(\frac{1.45 \times 10^{10}}{2 \times 10^{15}}\right) = -.615$

The SCEPTRE MOS model parameter is:

$FLEF = 2\phi_F$

The SPICE2 MOS model parameter is:

$PHI = 2\phi_F$

SPICE2 will automatically calculate the value of PHI if the value of N_B is specified in the parameter list. The analyst should only specify a value for PHI if he wishes to use an experimental value.

The NET-2 MOS model does not use the Fermi level as an explicit parameter.

4) Flat Band Voltage

N-Channel Value

$$V_{FB} = 3.2 - 3.25 - .56 - .3675 - \frac{1.6 \times 10^{-19} * 1 \times 10^{11}}{5.06 \times 10^{-8}} = -1.29 \text{ V}$$

P-Channel Value

$$V_{FB} = 3.2 - 3.25 - .56 + .3075 - \frac{1.6 \times 10^{-19} * 1 \times 10^{11}}{5.06 \times 10^{-8}} = .62 \text{ V}$$

The SCEPTRE MOS model parameter is:

$$VF = V_{FB}$$

The SPICE2 model calculates the value of flatband voltage automatically using the equation listed previously in chapter IV.E.5.b.

The NET-2 MOS model does not use the flatband voltage as an explicit parameter.

5) Threshold Voltage

N-Channel Value

$$V_T(V_{BS}) \cdot 1.29 + .735 + 1.62 \sqrt{.735} = .83 \text{ V}$$

P-Channel Value

$$-.62 - .615 - .52 \sqrt{|-.615|} = -1.64 \text{ V}$$

The SCEPTRE MOS model does not use the threshold voltage as an explicit parameter. However, the value of V_T is calculated internally.

The SPICE2 MOS model will calculate the value of threshold voltage automatically if the value of substrate doping is specified in the parameter list. This value will be printed out as VTO in the SPICE2 output. The analyst should not specify VTO in the SPICE2 parameter list if he wishes to use the second order model. A specified value of VTO will be overriden by the calculated value if both VTO and substrate doping (NSUB) are specified.

The NET-2 MOS model parameter is:

N-Channel Value

$$A_1 = -\beta/2\ (V_T) = \frac{-4.08 \times 10^{-4} * .83}{2} = -1.69 \times 10^{-4}$$

P-Channel Value

$$= -8.40 \times 10^{-5} * - \frac{1.64}{2} = 6.89 \times 10^{-5}$$

Note that V_T is considered positive for both N-channel and P-channel enhancement transistors in NET-2.

b. Two-Dimensional Effects on Threshold Voltage

As indicated previously in chapter IV.E.5.b, the bulk threshold parameter (GAMMA) in the SPICE2 model is modified by a function of substrate bias. The calculation of the value of this function is performed automatically if the value of the source and drain diffusion depths are provided in the parameter list. A sample calculation is performed below to provide an indication of the value of the function.

N-Channel Value

$$f(V_{BS})\ [\text{at } V_{BS}=10] = \left[1 - \frac{2\times10^{-4}}{5\times10^{-4}}\left(\sqrt{1+2\ \frac{\sqrt{\frac{2\times1.05\times10^{-12}}{1.6\times10^{-19}\times2\times10^{16}}}\ (.735+10)}{2\times10^{-4}}}-1\right)\right]$$

$= .86$

P-Channel Value

$$f(V_{BS}) = \left[1 - \frac{2\times10^{-4}}{5\times10^{-4}}\left(\sqrt{1+2\ \frac{\sqrt{\frac{2\times1.05\times10^{-12}}{1.6\times10^{-19}\times2\times10^{15}}}\ 10.615}{2\times10^{-4}}}-1\right)\right]$$

$= .64$

The SPICE2 MOS model also uses the parameter XJ (junction depth) together with the parameter LD (lateral diffusion) coefficient to decrease the channel length by the amount of out diffusion from the source and drain. The effective channel length then becomes:

$$L_E = L - 2*LD*XJ$$

If the analyst has specified L as the channel length from the mask dimensions, he will wish to specify a value for LD. A typical value would be:

$$LD = .8$$

Specification of either XJ or LD as zero eliminates the calculation of effective channel length in SPICE2.

c. Weak Inversion Effects

As indicated previously in chapter IV.E.5.c, the drain current generator provides current at gate-to-source voltages less than the classical threshold voltage. This current is described by an exponential function up to the point where $V_{GS} = V_{ON}$. V_{ON} is a function of the classical threshold voltage, the number of fast surface states, and the substrate bias. SPICE2 automatically calculates the value of V_{ON} if substrate doping and fast surface state density parameters are specified. Example values of V_{ON} are calculated below. These may be compared with the values of classical threshold voltage calculated previously.

N-Channel Value

$$V_{ON}\begin{bmatrix} \text{at } f(V_{BS}) = 1 \\ V_{BS} = 0 \end{bmatrix} = .83 + .026\left(1 + \frac{1.6\times10^{-19}*1\times10^{11}}{5.06\times10^{-8}} + \frac{1.62}{2\sqrt{.735}}\right)$$

$$= .83 + .06 = .89$$

P-Channel Value

$$= -1.64 - .026\left(1 + \frac{1.6\times10^{-19}*1\times10^{11}}{5.06\times10^{-8}} + \frac{.52}{2\sqrt{.615}}\right)$$

$$= -1.64 - .04 = -1.68$$

d. Channel Length Modulation Effects

As noted previously in chapter IV.E.5.d, all three of the models discussed here contain provisions for modeling incomplete saturation effects resulting from channel length modulation. The parameters which must be specified for each model are indicated below.

1) SCEPTRE Channel Length Modulation

The SCEPTRE MOS model requires specification of the following parameters to simulate channel shortening effects:

$$C = \frac{qN_B}{2\varepsilon_s}$$

$$G = \frac{2}{q\,N_B W\,V_L X_e}$$

$E = E_C$ = critical E field to achieve thermal limiting velocity

	N-Channel Value	P-Channel Value
$C =$	$\frac{1.6\times10^{-19}*\ 2\times10^{16}}{2\times1.05\times10^{-12}} = 1.52\times10^{9}$	$\frac{1.6\times10^{-19}*2\times10^{15}}{2\times1.05\times10^{-12}} = 1.52\times10^{8}$
$E =$	7.45×10^{4}	1.81×10^{5}
$X_e =$	$\frac{2\times10^{-4}}{\ell n\left(\frac{2\times10^{-4}}{1\times10^{-6}}\right)-1} = 4.65 \times 10^{-5}$	$\frac{2\times10^{-4}}{\ell n\left(\frac{2\times10^{-4}}{1\times10^{-6}}\right)-1} = 4.65 \times 10^{-5}$

N-Channel Value

$$G = \frac{2}{1.6\times10^{-19} * 2\times10^{16} * 5\times10^{-3} * 6\times10^{7} * 4.65\times10^{-5}} = 44.8$$

P-Channel Value

$$\frac{2}{1.6\times10^{-19} * 2\times10^{15} * 5\times10^{-3} * 3\times10^{7} * 4.65\times10^{-5}} = 896$$

2) SPICE2 Channel Length Modulation

If a zero value or no value is specified for the LAMBDA parameter in SPICE2, channel length modulation effects will be automatically calculated from the equations specified in chapter IV.E.5.d. If the analyst wishes to modify the saturation characteristic he may specify a value for LAMBDA. This will override any automatic calculations. As a general rule, the analyst should not specify LAMBDA. Note that if channel length modulation effects are to be excluded from the model, a small but nonzero value of LAMBDA should be used (LAMBDA $\leq$ .001).

3) NET-2 Incomplete Saturation

The NET-2 MOS model uses a conductance to produce incomplete saturation effects. The parameters for that conductance are estimated below.

N-Channel Value

$$V_D - V_{DSAT} = 10 - (10 - .83) = .83$$

$$\sqrt{\frac{2\varepsilon_s}{qN_B}} = \sqrt{\frac{2 \times 1.05 \times 10^{-12}}{1.6 \times 10^{-19} \times 2 \times 10^{15}}} = 8.1 \times 10^{-5}$$

$$\Delta L = 2.57 \times 10^{-5} \sqrt{.83} = 2.34 \times 10^{-5}$$

$$\beta L = 4.08 \times 10^{-4} * 5 \times 10^{-4} = 2 \times 10^{-7}$$

$$K_1 = \frac{2.0 \times 10^{-7} * 8.1 \times 10^{-5} (.83)^2}{8\left(5 \times 10^{-4} - .234 \times 10^{-4}\right)^2 (.83)^{\frac{1}{2}}} = 6.74 \times 10^{-6}$$

$$K_2 = \frac{2.0 \times 10^{-7} * 8.1 \times 10^{-5} * .83}{4\left(5 \times 10^{-4} - .234 \times 10^{-4}\right)^2 (.83)^{\frac{1}{2}}} = 1.62 \times 10^{-5}$$

$$K_3 = \frac{2.0 \times 10^{-7} * 8.1 \times 10^{-5}}{8\left(5 \times 10^{-4} - .234 \times 10^{-4}\right)^2 (.83)^{\frac{1}{2}}} = 9.[illegible] \times 10^{-6}$$

P-Channel Value

$$V_D - V_{DSAT} = -10 - [-10 (-1.64)] = 1.64$$

$$\sqrt{\frac{2\varepsilon_s}{qN}} = \sqrt{\frac{2 \times 1.05 \times 10^{-12}}{1.6 \times 10^{-19} \times 2 \times 10^{15}}} = 8.11 \times 10^{-5}$$

$$\Delta L = 8.11 \times 10^{-5} \sqrt{1.64} = 1.04 \times 10^{-4}$$

$$\beta L = 8.4 \times 10^{-5} \times 5 \times 10^{-4} = 4.2 \times 10^{-8}$$

$$K_1 = \frac{4.20 \times 10^{-8} * 8.11 \times 10^{-5} * (1.64)^2}{8(5 \times 10^{-4} - 1.04 \times 10^{-4})^2 \sqrt{1.64}} = 5.76 \times 10^{-3} \text{ mA/V}$$

$$K_2 = \frac{4.20 \times 10^{-8} * 8.11 \times 10^{-5} * 1.64}{4(5 \times 10^{-4} - 1.04 \times 10^{-4})^2 \sqrt{1.64}} = 6.95 \times 10^{-6} \text{ mA/V}^2$$

$$K_3 = \frac{4.2 \times 10^{-8} * 8.11 \times 10^{-5}}{8(5 \times 10^{-4} - 1.04 \times 10^{-4})^2 \sqrt{1.64}} = 2.12 \times 10^{-3} \text{ mA/V}^3$$

e. Variable Mobility Effects

As noted previously in chapter IV.E.5.c, each of the three MOS models discussed here contain provisions for modeling variable mobility effects on the drain current. Since the physics of variable surface

mobility is not completely understood, each of the models can be most effectively parameterized from experimental data on the transconductance as a function of gate voltage. An example of such data for N-channel and P-channel device is shown in figures IV-48 and IV-49. In the absence of such data, the variation in mobility as a function surface E-field can be estimated from typical parameter values.

1) SCEPTRE Variable Mobility

Examination of the SCEPTRE model equation for variable mobility indicates that the low voltage transconductance factor (β_0) is reduced to one-half its original value when:

$$\frac{C_{OX}}{2\varepsilon_s E_{SC}} (V_G - V_T) = 1$$

From figures IV-48 and IV-49, the slope of the drain current versus gate voltage curve is reduced to one-half of its low voltage value at $V_G = V_{GCN} = 3.73$ volts and $V_G = V_{GCP} = 4.5$ volts for the N-channel and P-channel transistors, respectively. The SCEPTRE model parameter is

$$DB = \frac{C_{OX}}{2\varepsilon_s E_{SC}} = \frac{1}{V_{GC} - V_T}$$

and can be calculated as follows:

	N-Channel Value	P-Channel Value
DB	$\frac{1}{3.73 - 2.01} = .58$	$\frac{1}{4.5 - 1.7} = .36$

The value of E_{SC} can also be calculated as:

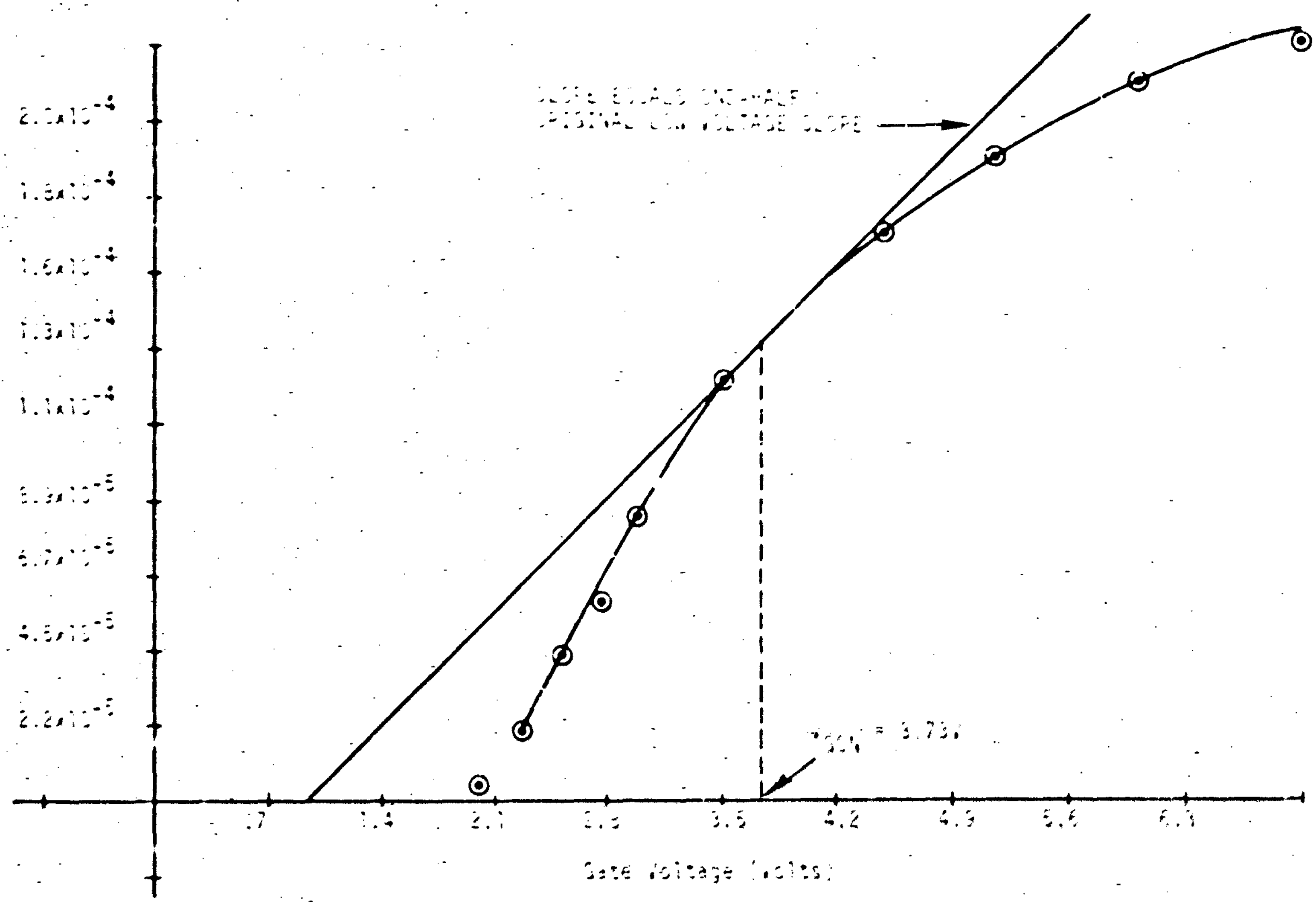


Figure I-41. N-Channel Data for Variable Mobility Modeling

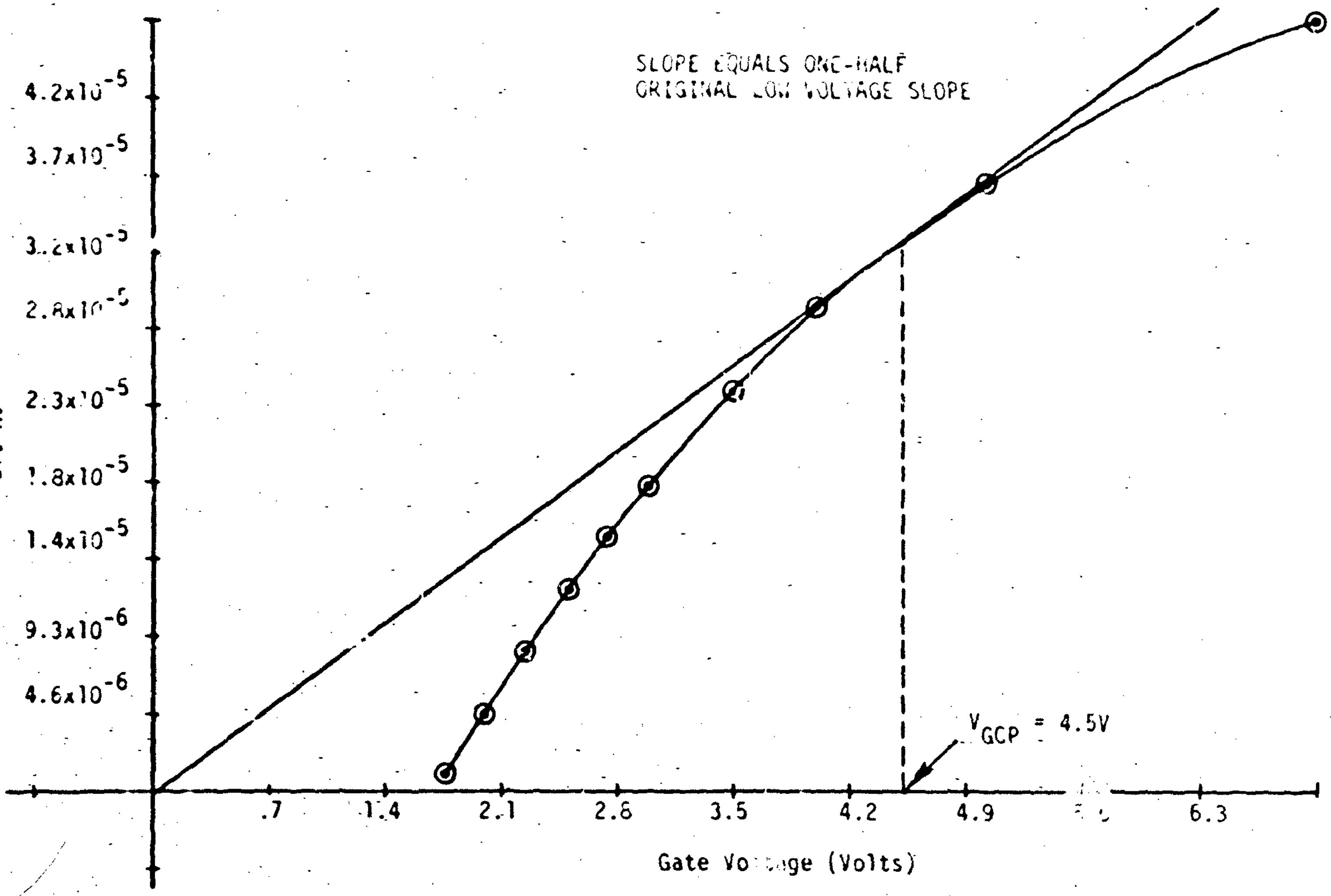


Figure IV-49. P-Channel Data for Variable Mobility Modeling

N-Channel Value

P-Channel Value

$$E_{SC} = \frac{1.72\,(5.06 \times 10^{-8})}{2 \times 1.05 \times 10^{-12}} = 4.16 \times 10^{4} \qquad \frac{2.8\,(5.06 \times 10^{-8})}{2 \times 1.05 \times 10^{-12}} = 6.75 \times 10^{4}$$

Note that these values are reasonably close (approximately a factor of 2) to those recorded previously for the critical E field (E_C) required for the onset of thermal limiting velocity. In the absence of experimental data the value of DB can be calculated from E_C as shown below.

N-Channel Value

P-Channel Value

$$DB = \frac{5.06 \times 10^{-8}}{2 * 1.05\times10^{-12} * 7.45\times10^{4}} = .32 \qquad \frac{5.06 \times 10^{-8}}{2 * 1.05\times10^{-12} * 1.81\times10^{5}} = .14$$

2) SPICE2 Variable Mobility Modeling

Parameterization of the SPICE2 variable mobility model requires specification of values for μ_0, U_{CRIT}, U_{TRA}, and U_{EXP}. See chapter IV.E.5.e.3 for the functional relationship of these parameters to the surface mobility. If the width-to-length ratio is known, the value of μ_0 can be calculated from experimental data for β_0.

$$\mu_0 = \frac{\beta_0 L}{W C_{OX}}$$

N-Channel Value

P-Channel Value

$$\mu_0 = \frac{1.68 \times 10^{-3}}{60 * 5.06 \times 10^{-8}} = 555\ (@\ W/L = 60) \qquad \frac{2.96 \times 10^{-4}}{40 * 5.06 \times 10^{-8}} = 146\ (@\ W/L = 40)$$

Since the ratio of the effective gate voltage to the critical voltage for mobility degradation is raised to a power in the SPICE2 model, a logarithmic plot of drain voltage versus $V_G - V_T$ is often useful for parameterization.

Taking the logarithm of both sides of the equation describing drain current with variable mobility effects yields the approximate result:

$$\log I_D = \log \left| \mu_0 V_{DS} \left(\frac{U_{CRIT}\, \epsilon_s}{C_{OX}} \right)^{U_{EXP}} \right| + (1-U_{EXP}) \log (V_{GS} - V_T)$$

Figures IV-50 and IV-51 show plots of log drain current versus log $(V_{GS}-V_T)$ for P and N-channel transistors, respectively. Two regions are shown. For low gate voltages the mobility is undegraded. At higher gate voltages, mobility degradation sets in and the slope of the log I_D versus log $(V_{GS} - V_T)$ curve is reduced. The boundary between the two regions is set by U_{CRIT}, while the slope of the degraded curve is given by $(1-U_{EXP})$.

The values of U_{EXP} can be obtained from the curves given in figures IV-50 and IV-51.

U_{EXP} = 1-Slope

	N-Channel Value	P-Channel Value
U_{EXP}	1 - .44 = .56	1 - .49 = .51

The reader should recall that the SPICE* model does not consider variable mobility effects until $V_{GS} - V_T$ exceeds the critical voltage defined by $\frac{U_{CRIT}\, \epsilon_s}{C_{OX}}$. Appropriate values of U_{CRIT} may be obtained from the curves shown in figures IV-50 and IV-51. The breakpoint in the curves identifies the critical value of $(V_{GS} - V_T)$. From this, U_{CRIT} may be calculated as:

$$U_{CRIT} = \frac{C_{OX}}{\epsilon_S} (V_{GS} - V_T)_{CRIT}$$

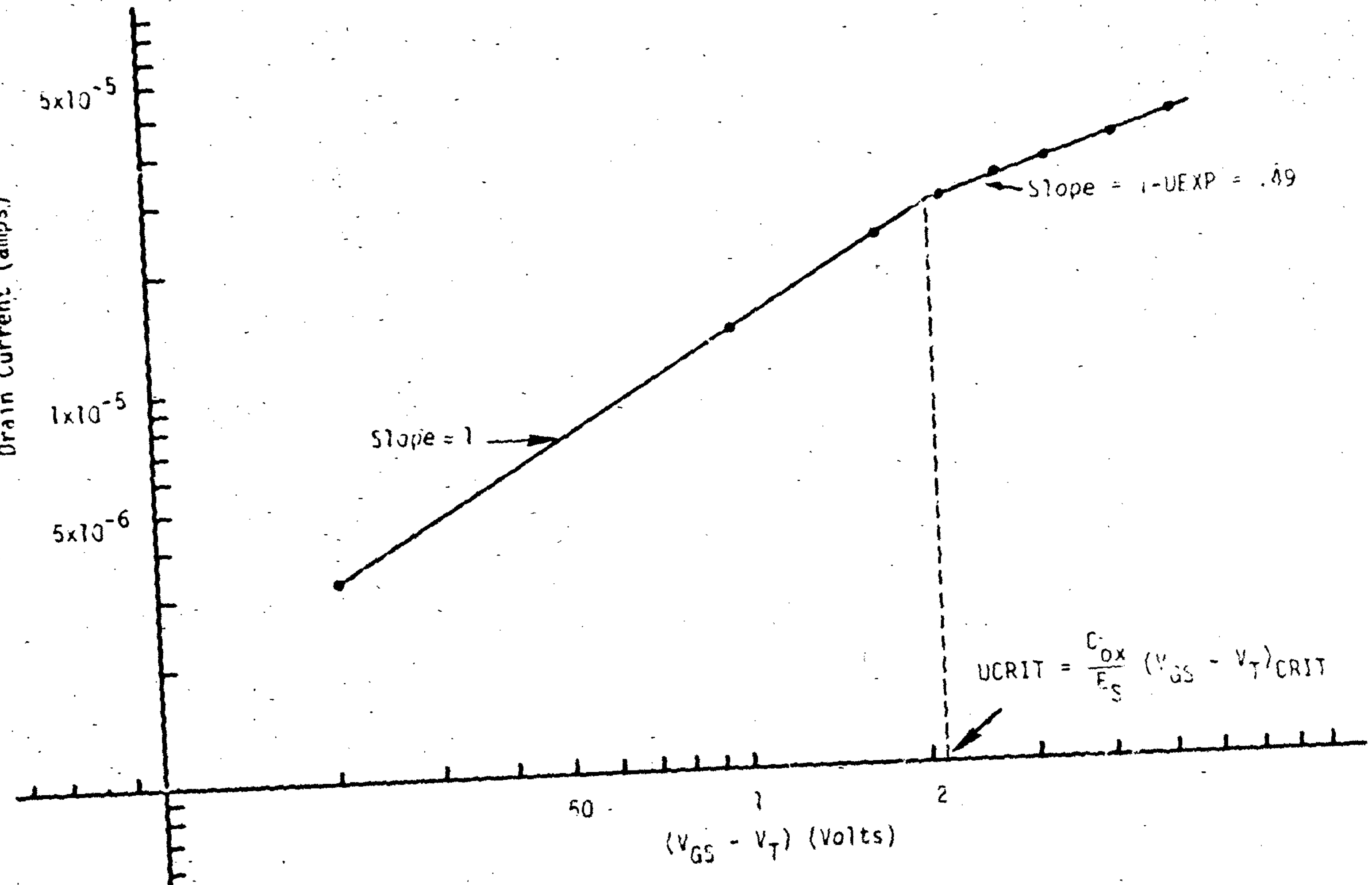


Figure IV-50. P-Channel Data for Parameterizing the SPICE2 Variable Mobility Model

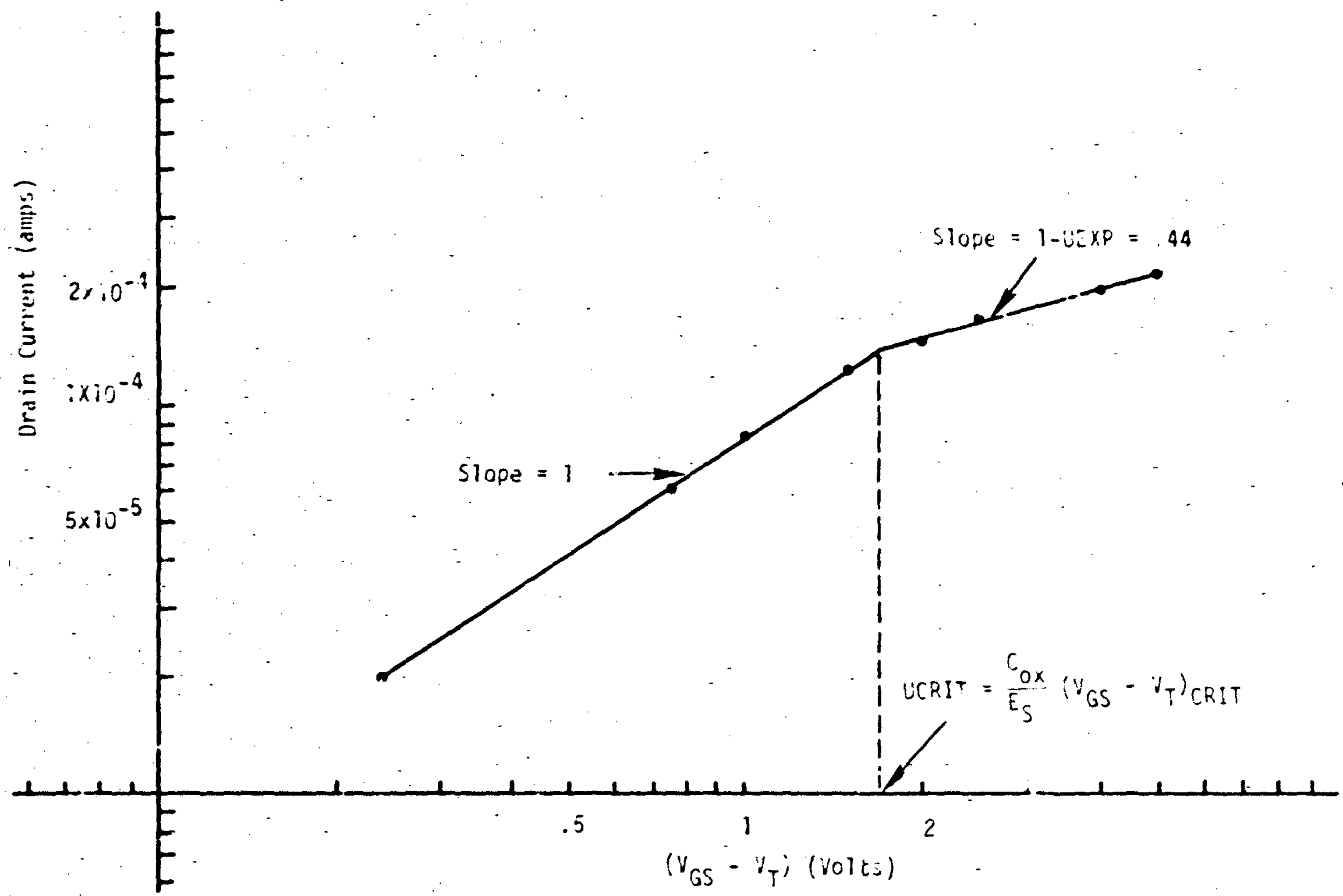


Figure IV-51. N-Channel Data for Parameterizing the SPICE2 Variable Mobility Model

These values are:

N-Channel

$$U_{CRIT} = \frac{5.06 \times 10^{-8}}{1.05 \times 10^{-12}} (1.75 \text{ V}) = 8.43 \times 10^4 \text{ V/cm}$$

P-Channel

$$= \frac{5.06 \times 10^{-8}}{1.05 \times 10^{-12}} (2.05) = 9.88 \times 10^4 \text{ V/cm}$$

The remaining SPICE2 variable mobility parameter, U_{TRA}, is extremely difficult to parameterize. Degradation of mobility with drain voltage is usually important only in devices with channel lengths shorter than 3 μm. In these cases, the functional form of the SPICE2 model is probably not appropriate. The analyst is advised to set U_{TRA} to zero for most analyses.

3) NET-2 Variable Mobility

The NET-2 variable mobility model is entirely empirical. The parameter A5 can be determined from the gate voltage (V_{GC}) where the initial value of the transconductance parameter (β_0) is decreased by one-half.

$$A_5 = \frac{-\frac{1}{8}\beta_0}{V_{GC}}$$

N-Channel Value

$$A_5 \quad -\frac{1}{8}\,\frac{8.42 \times 10^{-5}}{3.73} = -2.82 \times 10^{-6}$$

P-Channel Value

$$-\frac{1}{8}\,\frac{1.48 \times 10^{-5}}{4.5} = -4.11 \times 10^{-7}$$

f. Temperature Effects

In SPICE2, temperature dependent parameters in the equation for the voltage V_{ON} are automatically updated if the analyst specifies a temperature other than the default value of 27°C. Similar temperature effects modeling could be accomplished by manually updating appropriate

parameters in the SCEPTRE model. A sample calculation is shown below for calculating the threshold voltage of the N-channel and P-channel devices at a temperature of 125°C.

N-Channel Value

$$2\phi_F(\text{at } 125°C) = 2 * .0345 \ \ell n \left[\frac{2 \times 10^{16}}{3.86 \times 10^{16} * 398^{3/2} \exp\left(\frac{-1.12}{2 * 8.61 \times 10^{-5} * 398} \right)} \right]$$

$$= .463$$

$$V_{FB} (\text{at } 125°C) = 3.2 - 3.25 - .56 - .2315 - .315 = -1.16$$

$$V_T(V_{BS} = 0 \text{ at } 125°C) = -1.16 + .463 + 1.62 \sqrt{.463}$$

$$= .41 \text{ V}$$

P-Channel Value

$$2\phi_F(\text{at } 125°C) = 2 \times .0345 \ \ell n \left[\frac{3.86 \times 10^{16} \times 398^{3/2} \exp\left(\frac{-1.2}{2 \times 8.61 \times 10^{-5} * 398} \right)}{2 \times 10^{15}} \right]$$

$$= -.384$$

$$V_{FB} (\text{at } 125°C) = 3.2 - 3.25 - .56 + .152 - .315 = -.77$$

$$V_T (V_{BS}=0 \text{ at } 125°C) = -.77 - .304 - .52 \sqrt{|-.304|}$$

$$= -1.36 \text{ V}$$

8. Code Implementation and Notes

Table IV-9 provides values for parameterizing the second order effects inclusive models described previously in this subsection. The values included in the table were taken from those calculated in the parameterization subsection.

In order to use the SCEPTRE model, the subroutine FMOS must be included in the SCEPTRE deck. An anotated listing of FMOS is shown in

TABLE IV-9. SCEPTRE, CIRCUS 2, TRAC, NET-2, AND SPICE 2 MODEL PARAMETERS REQUIRED FOR SECOND ORDER EFFECTS MODEL*

[illegible] IMPLEMENTATION				[illegible]				[illegible]			
PARAMETER	DEFINITION	[illegible]	[illegible]	PARAMETER	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	Type & Transit [illegible] Factor	[illegible]	[illegible]		[illegible]	[illegible]					
[illegible]	[illegible]	[illegible]	[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
				[illegible]							
[illegible]	Substrate Bias	[illegible]	[illegible]	[illegible]	[illegible]			[illegible]	[illegible]	[illegible]	
				[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		[illegible]
[illegible]	[illegible] Factor	[illegible]	[illegible]			[illegible]		[illegible]	[illegible]	[illegible]	[illegible]
								[illegible]	[illegible]		
								[illegible]	[illegible]		
[illegible]***	[illegible]	[illegible]	[illegible]	[illegible]***	[illegible]	[illegible]	[illegible]	[illegible]***	[illegible]	[illegible]	[illegible]
[illegible]***	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]***	[illegible]	[illegible]	[illegible]
[illegible]***	[illegible]	[illegible]	[illegible]					[illegible]**	[illegible]	[illegible]	[illegible]

TABLE IV-9. SCEPTRE, CIRCUS 2, TRAC, NET-2, AND SPICE 2 MODEL PARAMETERS REQUIRED FOR SECOND ORDER EFFECTS MODEL* (Continued)

[illegible]				[illegible]				[illegible]			
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
				[illegible]	[illegible]	[illegible]	[illegible]				
				[illegible]	[illegible]	[illegible]	[illegible]				
				[illegible]	[illegible]	[illegible]	[illegible]				
				[illegible]	[illegible]	[illegible]	[illegible]				
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]		[illegible]		
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[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]					
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]				
				[illegible]	[illegible]	[illegible]	[illegible]				
				[illegible]	[illegible]	[illegible]	[illegible]				
				[illegible]	[illegible]	[illegible]	[illegible]				
				[illegible]	[illegible]	[illegible]	[illegible]				
				[illegible]	[illegible]	[illegible]	[illegible]				
				[illegible]	[illegible]	[illegible]	[illegible]				

TABLE IV-9. SCEPTRE, CIRCUS 2, TRAC, NET-2, AND SPICE 2 MODEL PARAMETERS REQUIRED FOR SECOND ORDER EFFECTS MODEL* (Continued)

SCEPTRE, CIRCUS 2, TRAC (SUBROUTINE IMPLEMENTATION)				NET-2				SPICE 2			
CODE PARAMETERS	DEFINITION	[illegible]	[illegible]	[illegible]	DEFINITION	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
N***	Substrate to Source/Drain [illegible] Constant	[illegible]	[illegible]	[illegible]	[illegible]						
				[illegible]	[illegible]						
					[illegible]						
B***	[illegible] Constant	[illegible]	[illegible]	[illegible]	[illegible]						
				[illegible]	[illegible]						
				[illegible]	[illegible]						
				[illegible]	[illegible]						
				[illegible]	[illegible]						
				[illegible]	[illegible]						
V_{BS}***	Substrate-Source Contact Potential	[illegible]	[illegible]	[illegible]	Substrate-Source Contact Potential	[illegible]	[illegible]	[illegible]	[illegible]		
V_{BD}	Substrate-Drain Contact Potential	[illegible]	[illegible]	[illegible]	Substrate-Drain Contact Potential	[illegible]	[illegible]				
$F_{C_{BS}}$	Substrate-Source [illegible] Factor	[illegible]	[illegible]	[illegible]	[illegible]						
$F_{C_{BD}}$	Substrate-Drain [illegible] Factor	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]				

TABLE IV-9. SCEPTRE, CIRCUS 2, TRAC, NET-2, AND SPICE 2 MODEL PARAMETERS REQUIRED FOR SECOND ORDER EFFECTS MODEL* (Concluded)

SCEPTRE/CIRCUS/TRAC (SUBROUTINE IMPLEMENTATION)				NET-2 BUILT-IN MODEL				SPICE 2 BUILT-IN MODEL			
CODE PARAMETER	DEFINITION	NMOS VALUE	PMOS VALUE	CODE PARAMETER	DEFINITION	NMOS VALUE	PMOS VALUE	CODE PARAMETER	DEFINITION	NMOS VALUE	PMOS VALUE
FEEF	Strong Inversion Potential	.735 V	-.615 V					PHI	PHI Strong Inversion Surface Potential	**	**
RD	Total Drain Resistance***	3.46	7.56					RD***	Intrinsic Transistor Drain Resistance	[illegible]	[illegible]
RS	Total Source Resistance***	2.55	7.56					RS***	Intrinsic Transistor Source Resistance	[illegible]	[illegible]
								TOX	Gate Oxide Thickness	[illegible]	[illegible]
								NSUB	Substrate Doping Concentration	[illegible]	[illegible]
								NSS	Effective Surface State Density	[illegible]	[illegible]
								NFS	Effective Fast Surface State Density	[illegible]	[illegible]
								XJ	Metallurgical Depth	2E-4	2E-4
								NGATE	Silicon Gate Doping Concentration		
								TPG	Gate Doping Concentration Type	+1 Opposite Substrate Polar Type; -1 Same as Substrate Polar Type	
R1	P-well Resistan	NA	NA								
R2	P-well Resistance	3582	NA								

* Values based on typical parameters from chapter IV E 7 and [illegible]
** Do not specify unless a modification of the calculation procedures described in chapter IV E 5 is desired
*** Parasitics calculated in chapter IV [illegible] have been retained

figure IV-52. The reader is referred to the next section for a series of example calculations demonstrating second order effects.

9. Computer Examples

Figures IV-53 through IV-55 give listings of "curve tracer" programs implemented for the SCEPTRE, NET-2, and SPICE2 MOS models. The model parameters were taken from table IV-9 unless specific changes are indicated in the examples to follow. These examples have been chosen to illustrate the influence of the various second order effects on current/voltage characteristics of MOS devices. They should provide some guidance to the analyst in attempting to determine if he should consider these effects in his problem.

a. Substrate Bias Effects

Figures IV-56 and IV-57 show the effects of substrate bias on the drain characteristics of N-channel and P-channel transistors as modeled in SCEPTRE.

b. Two Dimensional Effects on Threshold Voltage

Figures IV-58 and IV-59 show the effects of two dimensional modifications to the threshold voltage of N-channel and P-channel transistors as modeled in SPICE2.

c. Weak Inversion Effects

Figures IV-60 and IV-61 demonstrate weak inversion effects on the turn-on characteristics of N-channel and P-channel transistors as modeled in SPICE2.

d. Channel Length Modulation Effects

Figures IV-62 and IV-63 demonstrate incomplete saturation resulting from channel length modulation in N-channel and P-channel transistors as modeled in NET-2.

e. Variable Mobility Effects

Figures IV-64 and IV-65 demonstrate the effects of mobility variation with gate voltage on the drain characteristics of N-channel and P-channel devices as modeled in SCEPTRE.

```
      FUNCTION FMOS(VG,VD,VBS,BO,DB,C,E,U,G,VF,PHI,FEEF,S)
      FSWTCH(X,R,S) = 1./(1.+EXP(AMIN1(100.,S*(R-X))))
      FA(VDA,VDE,VGE,B,VX,APHI,AFE)= B*SIGN(ABS(VDE)*ABS(VGE-VX-VDE/2.)
     1  -2.*APHI*((ABS(VDE)+AFE)**1.5-AFE**1.5)/3.,VDA)
      FP  (  VGE,ADE ,BEU,VX,PHI,APHI,VBE) =      VGE- ADE/BEU -VX +
     1 PHI*(APHI/2. -SQRT(ABS(VGE-ADE /BEU -VF-VBE+PHI*APHI/4.)))
      APHI = ABS(PHI)
      VX = VF + FEEF
      IF(VD*S.LT.0) GO TO 5
      VDE = VD
      VGE = VG
      VBE = VBS
      GO TO 10
    5 VDE = -VD
      VGE = VG - VD
      VBE = VBS - VD
   10 CONTINUE
      VMAX = 1.E3
      IF(ABS(VGE).GT.VMAX)  GO TO 50
      IF(ABS(VDE).GT.VMAX)  GO TO 50
      IF(ABS(VBE).GT.VMAX)  GO TO 50
      AFE = ABS(FEEF-VBE)
      VT = VX + PHI*SQRT(AFE)
      B = BO/(1. DB*ABS(VGE-VT))
      BEU = B*E*U
      AU = FA(VD,VDE,VGE,B,VX,APHI,AFE)
   30 VP = FP    (VGE,0.,BEU,VX,PHI,APHI,VBE)
   31 ADSS =       FA(VD,VP,VGE,B,VX,APHI,AFE)
      ADE = SIGN(ADSS,VP)
   32 VP = FP    (VGE,ADE ,BEU,VX,PHI,APHI,VBE)
   33 ADSS = FA(VD,VP,VGE,B,VX,APHI,AFE)
      A = U*(1.+G*ABS(ADSS)) -E/C
      AA = SIGN(AMAX1(1.E-100,ABS(A)),A)
      P = (ABS(VDE-VP)+E*U)/C
      TEMP = P**2 +4.*AA*U*ABS(VDE-VP)/C
      IF (TEMP.LT.0.) PRINT 100
      DU = (-P + SQRT(ABS(TEMP)))/(2. AA)
      F1 = FSWTCH(VGE,VT,S)
      F2 = FSWTCH(VDE,VP,S)
      FMOS = F1*F2*ADSS*U/(U+DU) +F1*(1.-F2)*AU
      RETURN
   50 FMOS = 0.
      RETURN
  100 FORMAT(5X,*NEGATIVE VALUE UNDER RADICAL IN DELTA L EQUATION *
     1  *CAUSED BY PARAMETER ERRORS IN FMOS REFERENCE.*)
      END
```

Figure IV-52. FMOS Subroutine Incorporating Second Order Effects for use With SCEPTRE

```
SUBPROGRAM

      FUNCTION FMOS(VG,VD,VBS,[illegible],PHI,FEEF,S)
      F [illegible] = 1./(1.+[illegible]AMIN1(130.,S*[illegible]))
      FA(VD,A,VDE,VGE,[illegible],APHI,AF) = [illegible]ABS(VGE-VA-VDE/2.)
     1 -2.*APHI*((ABS(VDE)+AFE)**1.5-AFE**1.5)/3.)*VDA)
      FP [illegible] VGE,ADE [illegible] VGE - ADE/HEU -VA +
     1 PHI*(APHI/2. +SQRT(ABS(VDE+ADE/HEU -VD-VBE+PHI*APHI/4.)))
      APHI = ABS(PHI)
      VX = VF + FEEF
      IF(VD*S.LT.0) GO TO 5
      VDE = VD
      VGE = VG
      VBE = VBS
      GO TO 10
    5 VDE = -VD
      VGE = VG - VD
      VBE = VBS - VD
   10 CONTINUE
      VMAX = 1.E4
      IF(ABS(VGE).GT.VMAX) GO TO [illegible]
      IF(ABS(VDE).GT.VMAX) GO TO [illegible]
      IF(ABS(VBE).GT.VMAX) GO TO [illegible]
      AFE = ABS(FEEF-VBE)
      VT = VA + PHI*SQRT(AFE)
      H = HO/(1.+[illegible]*ABS(VGE-VT))
      HEU = H*[illegible]
      AD = FA(VD,VDE,VGE,[illegible],VA,APHI,AFE)
   10 VP = FP [illegible] (VGE,[illegible]PHI,APHI,VBE)
   11 ADSS = [illegible] FA(VP,VP,V[illegible],VA,APHI,AFE)
      ADE = SIGN(ADSS,VP)
   12 VP = FP [illegible] (VGE,ADE [illegible],VA,PHI,APHI,VBE)
   13 ACSS = FA(VD,VP,VGE,[illegible],VA,APHI,AFE)
      A = [illegible]1.+[illegible]ABS(AD-S[illegible])
      AA = SIGN(AMA[illegible]1.E-100,ABS(A)),A)
      P = (ABS(VDE-VP))[illegible]
      TEMP = [illegible]*ABS(VGE-VT)[illegible]
      IF (TEMP.LT.0.) PRINT 103
      [illegible] = [illegible]P + SQRT(ABS([illegible]/2.)[illegible]AA)
      Z1 = FSWTCH(VGE,VT,S)
      Z2 = FSWTCH(VDE,VT,S)
      FMOS = [illegible]ADSS[illegible]AA
      RETURN
    0 FMOS = 0.
      RETURN
  103 FORMAT(5X,*NEGATIVE VALUE UNDER RADICAL IN DELTA L EQUATION *
     1 *CAUSED BY PARAMETER ERRORS IN FMOS REFERENCE.*)
      END

      FUNCTION FSTEP(T,TR,TO,TD,VO,VD)
C          RESTRICTIONS
C           TD CAN NOT BE 0
C            TO MUST BE LESS THAN AND NOT EQUAL TO 1.
      IF(T.GT.TO) GO TO 5
      FSTEP = VD
      IF(T.LT.T[illegible]2.) FSTEP = VO+[illegible]2.*TD
      RETURN
    5 TN = (T-TO)/TP
      N = 0
    6 IF(TN.LT.1.) GO TO 10
      TN = TN - 1.
      N = N + 1
      GO TO 6
   10 FSTEP = VO+N*DV
      IF(TN.GE.TOP) FSTEP = VO+V[illegible](TN-TOP)/(1.-TOP))
      RETURN
      END
```

(a) NMOS Listing

Figure IV-53. SCEPTRE Curve Tracer Program for Exercising Second Order Effects Model

```
      FUNCTION FSWEEP(T,TP,TO,TMAX,TD,TMIN,VMAX,VMIN)
C          RESTRICTIONS
C          TP CAN NOT BE 0.
      IF(T.GT.TO) GO TO 5
      FSWEEP = VMIN
      IF( T.LT.TO/2.) FSWEEP = VMIN*T*2./TO
      RETURN
 5    TN = (T-TO)/TP
 6    IF(TN.LT.2.0) GO TO 10
      TN = TN - 2.
      GO TO 6
 10   IF(TN.LE.TMAX) GO TO 20
      IF(TN.GE.TMIN) GO TO 30
      IF(TN.GE.TD) GO TO 40
      FSWEEP = VMAX
      RETURN
 20   FSWEEP = VMIN+(VMAX-VMIN)*TN/TMAX
      RETURN
 30   FSWEEP = VMIN
      RETURN
 40   FSWEEP = VMAX+(VMIN-VMAX)*(TN-TD)/(TMIN-TD)
      RETURN
      END

MODEL DESCRIPTION
    MODEL PMOS (G-S-D-B)
    UNITS = R=OHM,V=VOLT,I=AMP,T=SEC,L=HENRY,C=FARAD
        ELEMENTS
            RD,D -DD = 7.06
            RS,SS -S = 7.06
            CGD,G -DD = 2.44E-13
            CGS,G -SS = 2.44E-13
            CBD,BD -DD =5.05E-13
            CBS,BS -SS = 5.35E-13
            CBG,G -B = 1.68E-15
            JB,BS -SS = 0.
            JG,G -SS = 0.
            JD,DD -SS = FMOS(VJG,VJD,VJB,R,8E-5,.16,1.52E8,1.81E5,
                        5.3E-6,AVG,-.62,-.52,-.815,-10.)
            JSD,BD -DD = DIODE Q(2.30E-15,38.5)
            JSS,SS -BS = DIODE Q(2.30E-15,38.5)
            J1,DD -G = 0.
            J2,SS -G = 0.
            R3,BD -DD = 1.E12
            R4,BS -SS = 1.E12
            R5,B -BD = 5.
            R6,B -BS = 5.
        DEFINED PARAMETERS
            PFD = G 1(V(J1,PFI))
            PFS = G 1(V(J2,PFI))
            PFI = 100.
        FUNCTIONS
            G 1(V,VMAX) = (ABS(V/VMAX))

CIRCUIT DESCRIPTION
CURVE TRACER PROGRAM
    UNITS = R=OHM,V=VOLT,I=AMP,T=SEC,L=HENRY,C=FARAD
    ELEMENTS
        EG,S-GR  FSTEP(TIME,PTP,PTO,.,0.,-2.,0.,-2.,0)
        ED,S-DR  FSWEEP(TIME,PTP,PTO,.,0.,1.,0.,1.,P10.,-10.)
        RD,DR-D = 50.
        RG,GR-G =  1.E3
        T1,G-S-D-S = MODEL PMOS
    DEFINED PARAMETERS
        PTP = 1.E-3
        PTO = 0.
    OUTPUTS
        IRDT1,PLOT(ED)
            IRDT1,PLOT
        VJGT1,PLOT
        ED,PLOT
        JDT1,PLOT
    RUN CONTROLS
        RUN INITIAL CONDITIONS
        INTEGRATION ROUTINE = IMPLICIT
            MINIMUM STEP SIZE = 1.E-30
        MAXIMUM STEP SIZE = 65.E-6
        MAXIMUM INTEGRATION PASSES = 2.E5
        NO OVERFLOW PRINTOUTS
        STOP TIME = 5.E-3
            TERMINATE IF(PFS,GE,1.)
            TERMINATE IF(PFD,GE,1.)
END
```

(a) NMOS Listing (Concluded)

Figure IV-53. SCEPTRE Curve Tracer Program for Exercising Second Order Effects Model (Continued)

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```
SUBPROGRAM
      FUNCTION FMOS( [illegible] )
      [illegible]
      [illegible] VOE-VA-VOE/2. [illegible]
    1 [illegible] ,VOA)
      [illegible] = [illegible] VDE- ADE/HEU -VA +
    1 [illegible]
      [illegible] = ABS( [illegible] )
      VA = VP + [illegible]
      IF( [illegible] )
      VFE = VP
      V [illegible] = V
      VHE = VHS
      GO TO 10
    5 VF [illegible] = -VD
      V [illegible] = VC - V
      [illegible] = VHS - VD
   10 CONTINUE
      VMAX = 1.E [illegible]
      IF(ABS( [illegible] ).GT.VMAX) GO TO [illegible]
      IF(ABS( [illegible] ).GT.VMAX) GO TO [illegible]
      IF(ABS( [illegible] ).GT.VMAX) GO TO [illegible]
      A [illegible] = ABS( [illegible] )
      [illegible]
```

(b) PMOS Listing

Figure IV-53. SCEPTRE Curve Tracer Program for Exercising Second Order Effects Model (Continued)

[illegible]

(b) PMOS Listing (Concluded)

Figure IV-53. SCEPTRE Curve Tracer Program for Exercising Second Order Effects Model (Concluded)

```
***** 05/05/78 ******** SPICE 20.2 (26SEP76) ******** 12.24.12 *****

        NNOS CURVE TRACER

     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

***********************************************************************

.MODEL NCHNL1 NMOS(       NSUB 2.0E16     NSS 1.0E11      NFS 1.0E11
+                         XJ 2.0E-4       TOX 700.E-8     UO 805.
+                         UCRIT 1.0E4     UEXP .1         UTRA 0.0
+                         RD .21          RS .21          CBD 3.04E-8
+                         CBS 3.04E-8     CGB 6.65E-13    CGD 8.86E-12
+                         CGS 8.86E-12    JS 9.80E-12     PB .9)
       MN1 11 12 0 13 NCHNL1 W=1.97MIL L=.197MIL AD=1.88E-6 AS=1.88E-6
       VD1 0 11 PWL(0 0 15MS -15)
       VG1 12 0 DC 10
       VB1 13 0 DC 0
       MN2 21 22 0 23 NCHNL1 W=1.97MIL L=.197MIL AD=1.88E-6 AS=1.88E-6
       VD2 0 21 PWL(0 0 15MS -15)
       VG2 22 0 DC 10
       VB2 23 0 DC -2.0
       MN3 31 32 0 33 NCHNL1 W=1.97MIL L=.197MIL AD=1.88E-6 AS=1.88E-6
       VD3 0 31 PWL(0 0 15MS -15)
       VG3 32 0 DC 10
       VB3 33 0 DC -4.0
       MN4 41 42 0 43 NCHNL1 W=1.97MIL L=.197MIL AD=1.88E-6 AS=1.88E-6
       VD4 0 41 PWL(0 0 15MS -15)
       VG4 42 0 DC 10
       VB4 43 0 DC -6.0
       MN5 51 52 0 53 NCHNL1 W=1.97MIL L=.197MIL AD=1.88E-6 AS=1.88E-6
       VD5 0 51 PWL(0 0 15MS -15)
       VG5 52 0 DC 10
       VB5 53 0 DC -8.0
       MN6 61 62 0 63 NCHNL1 W=1.97MIL L=.197MIL AD=1.88E-6 AS=1.88E-6
       VD6 0 61 PWL(0 0 15MS -15)
       VG6 62 0 DC  10
       VB6 53 0 DC -10.0
                .TRAN 150US 15MS
       .PLOT TRAN I(VD1) I(VD2) I(VD3) I(VD4) I(VD5) I(VD6) (0,8E-3)
                .END
```

(a) NMOS

Figure IV-54. SPICE2 Curve Tracer Program for Exercising Second Order Effects Model

```
***** 05/05/78 ******** SPICE 2D.2 (26SEP76) ******** 12.12.42 *****

       PMOS CURVE TRACER

    INPUT LISTING                          TEMPERATURE =   27.000 DEG C

**************************************************************************

.MODEL PCHNL1 PMOS(    NSUB 2.0E15     NSS 1.0E11      NFS 1.0E11
+                      XJ 2.0E-4       TOX 700.E-8     UO 166.
+                      UCRIT 1.0E4     UEXP .1         UTRA 0.0
+                      RD .55          RS .55          CBD 9.62E-9
+                      CBS 9.62E-9     CGB 6.65E-13    CGD 8.86E-12
+                      CGS 8.86E-12    JS 6.20E-11     PB .9)
       MP1 11 12 0 13 PCHNL1 W=1.97MIL L=.197MIL AD=2.9E-6 AS=2.9E-6
       VD1 11 0 PWL(0 0 15MS -15)
       VG1 12 0 DC -10
       VB1 13 0 DC 0
       MP2 21 22 0 23 PCHNL1 W=1.97MIL L=.197MIL AD=2.9E-6 AS=2.9E-6
       VD2 21 0 PWL(0 0 15MS -15)
       VG2 22 0 DC -10
       VB2 23 0 DC 2.0
       MP3 31 32 0 33 PCHNL1 W=1.97MIL L=.197MIL AD=2.9E-6 AS=2.9E-6
       VD3 31 0 PWL(0 0 15MS -15)
       VG3 32 0 DC -10
       VB3 33 0 DC 4.0
       MP4 41 42 0 43 PCHNL1 W=1.97MIL L=.197MIL AD=2.9E-6 AS=2.9E-6
       VD4 41 0 PWL(0 0 15MS -15)
       VG4 42 0 DC -10
       VB4 43 0 DC 6.0
       MP5 51 52 0 53 PCHNL1 W=1.97MIL L=.197MIL AD=2.9E-6 AS=2.9E-6
       VD5 51 0 PWL(0 0 15MS -15)
       VG5 52 0 DC -10
       VB5 53 0 DC 8.0
       MP6 61 62 0 63 PCHNL1 W=1.97MIL L=.197MIL AD=2.9E-6 AS=2.9E-6
       VD6 61 0 PWL(0 0 15MS -15)
       VG6 62 0 DC -10
       VB6 63 0 DC 10.0
               .TRAN 150US 15MS
       .PLOT TRAN I(VD1) I(VD2) I(VD3) I(VD4) I(VD5) I(VD6) (0.,3.E-3)
               .END
```

(b) PMOS

Figure IV-54. SPICE2 Curve Tracer Program for Exercising Second Order Effect Model (Concluded)

```
NET-2 NETWORK ANALYSIS PROGRAM    RELEASE 9
 05/05/78    17.27.46.

        00000000011111111112222222222333333333344444444445555555555666666666677777777778
        12345678901234567890123456789012345678901234567890123456789012345678901234567890
        *DRAIN CHARACTERISTICS OF NET2 FIRST ORDER MODEL--N-CHANNEL/ENHANCEMENT
        LIBRARY
            MFET NMOS 5
                A1 -.17
                A2 -.22
                A3 -1.02
                A4 .204
                A5 -2.62E-6
                CO1 1.31
                CO2 .95
                CGD1 .083
                CGS1 .183
                IS1 .217E-12
                IS2 .300E-12
                K1 2.83E-3
                K2 -5.66E-3
                K3 3.11E-3
                N1 .5
                N2 .5
                S 1
                T 1000.
                TH1 38.5
                TH2 38.5
                VG1 .47
                VG2 3.3
                VGD1 .47
                VGD2 3.3
                VZ1 .5
                VZ2 .9
                W1 6.28E-3
                W2 6.28E-3
        MFET1 0 1 2 0 NMOS
        V1 1 0 P1
        V2 2 0 P2
        P1 0
        P2 0
        STATE1
            P2 0 (20) 2 (24) 15
            *P1 0 (7) 15
            PLOT I(V2) VS V(2)
            PLOT I(V2) VS V(1)
        END
```

(a) NMOS

Figure IV-55. NET-2 Curve Tracer Program for Exercising Second Order Effects Model

```
NET-2 NETWORK ANALYSIS PROGRAM    R4 PAGE 1
 05/05/76    16.47.18.

         0000000001111111111222222222233333333334444444444555555555566666666667777777777
         1234567890123456789012345678901234567890123456789012345678901234567890123456789
         * GATE CHARACTERISTICS OF NET2 FIRST ORDER MODEL--P-CHANNEL/ENHANCEMENT
         LIBRARY
              MFET PMOS 5
                   A1 -.059
                   A2 -.015
                   A3 -.521
                   A4 .042
                   A5 -4.36E-7
                   CG1 .595
                   CG2 .595
                   CGS1 .129
                   CGS1 .243
                   IS1 2.39E-12
                   IS2 2.39E-12
                   K1 5.7E-3
                   K2 -5.43E-3
                   K3 2.12E-3
                   N1 .5
                   N2 .5
                   S -1
                   T 1000.
                   TH1 300.
                   TH2 300.
                   VG1 .27
                   VG2 2.0
                   VGO1 2.9
                   VGO2 2.5
                   VZ1 .9
                   VZ2 .9
                   W1 5.28E-3
                   W2 5.28E-3
         MFET1 0 1 2 0 PMOS
         V1 1 0 W1
         V2 2 0 W2
         W1 0
         W2 0
         STATE1
              W2 0 (20) -2 (26) -15
              *W1 0 (7) -14
              PLOT I(V2) VS V(2)
              PLOT I(V2) VS W(1)
         END
```

(b) PMOS

Figure IV-55. Net-2 Curve Tracer Program for Exercising Second Order Effects Model (Concluded)

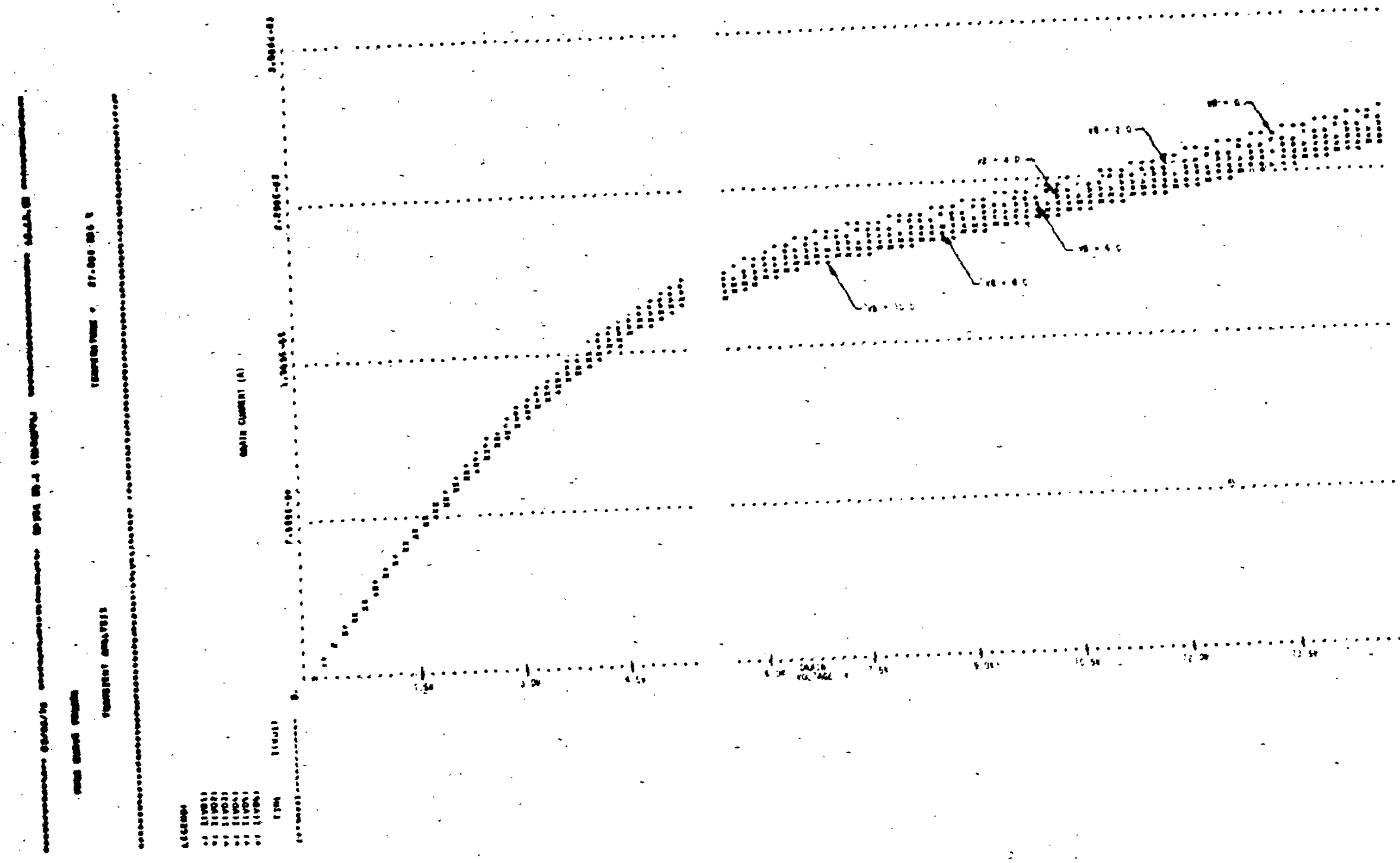


Figure IV-56. SCEPTRE N-Channel Model Demonstrating Substrate Bias Effects

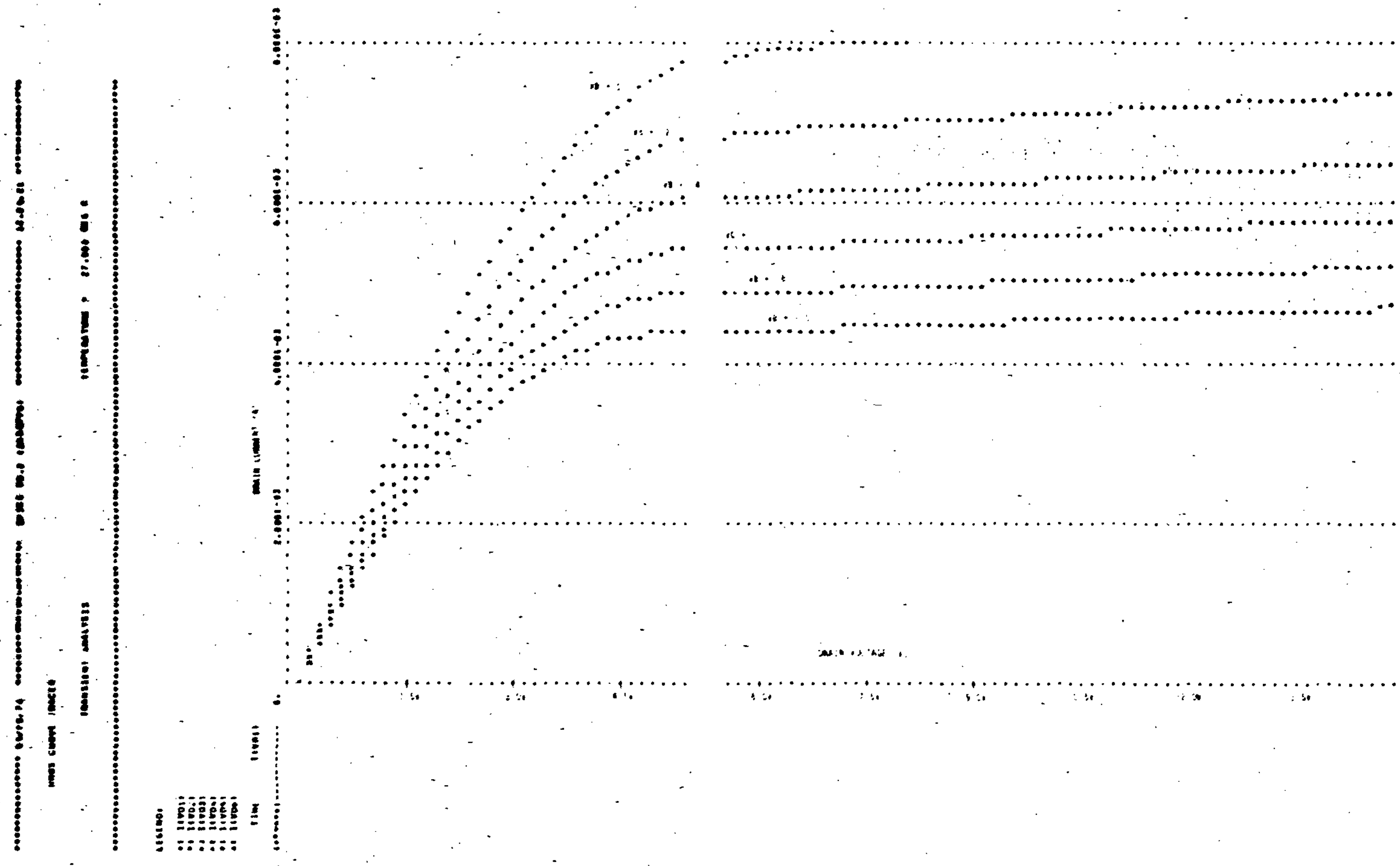


Figure IV-57. SCEPTRE P-Channel Model Demonstrating Substrate Bias Effects

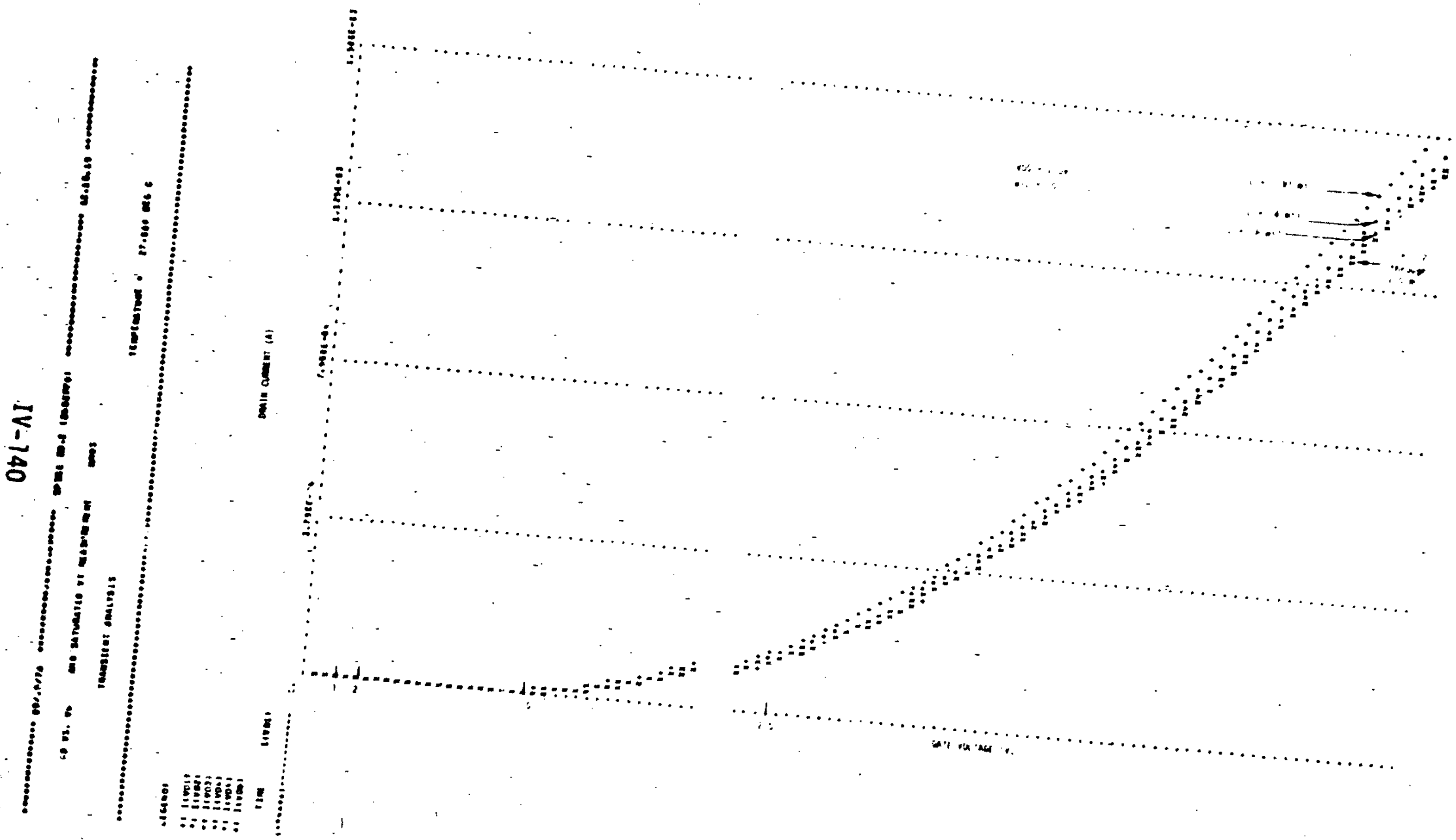


Figure IV-58. SPICE2 N-Channel Model Demonstrating Two Dimensional Effects on Threshold Voltage

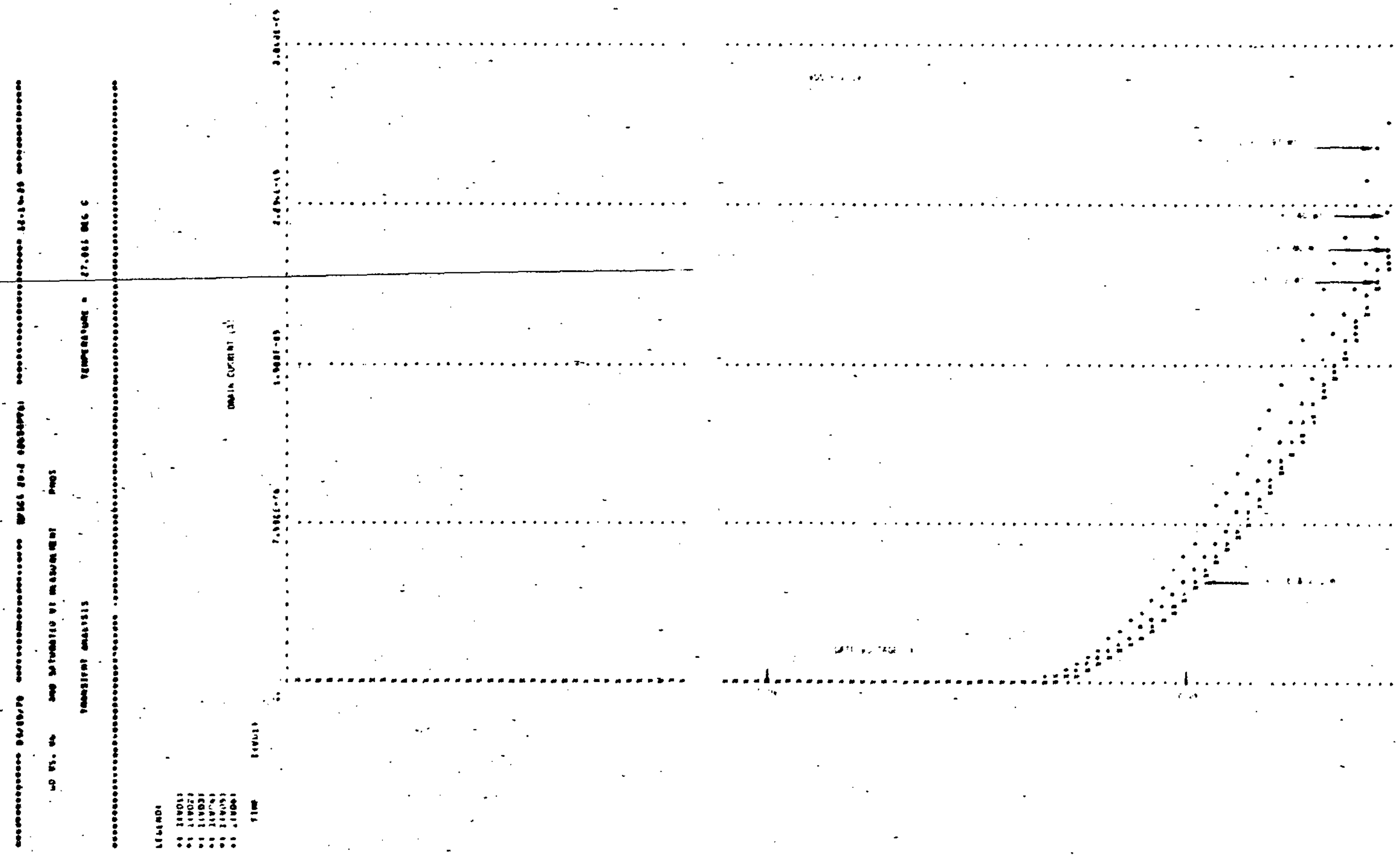


Figure IV-59. SPICE2 P-Channel Model Demonstrating Two Dimensional Effects on Threshold Voltage

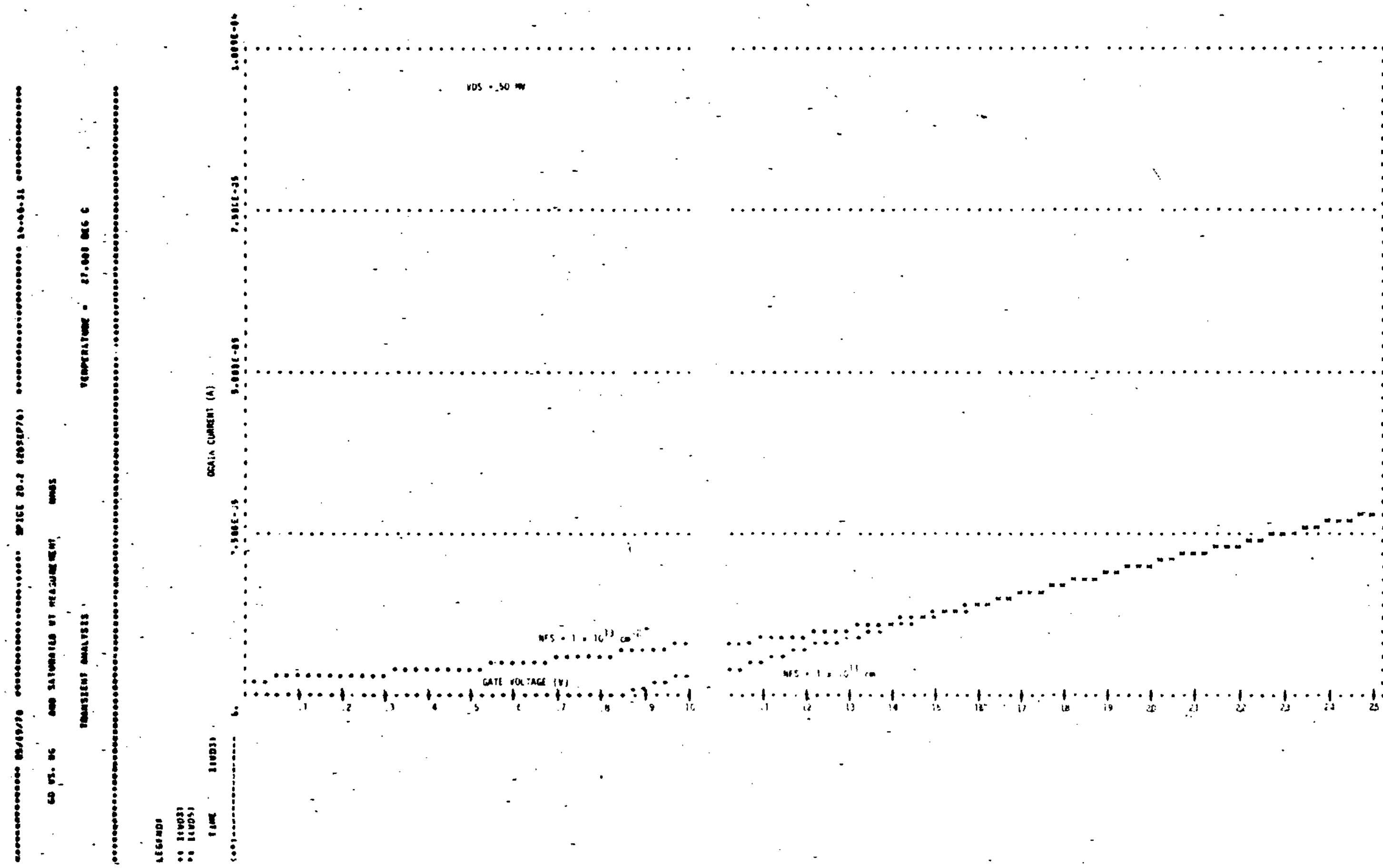


Figure IV-60. SPICE2 N-Channel Model Demonstrating Weak Inversion Effects

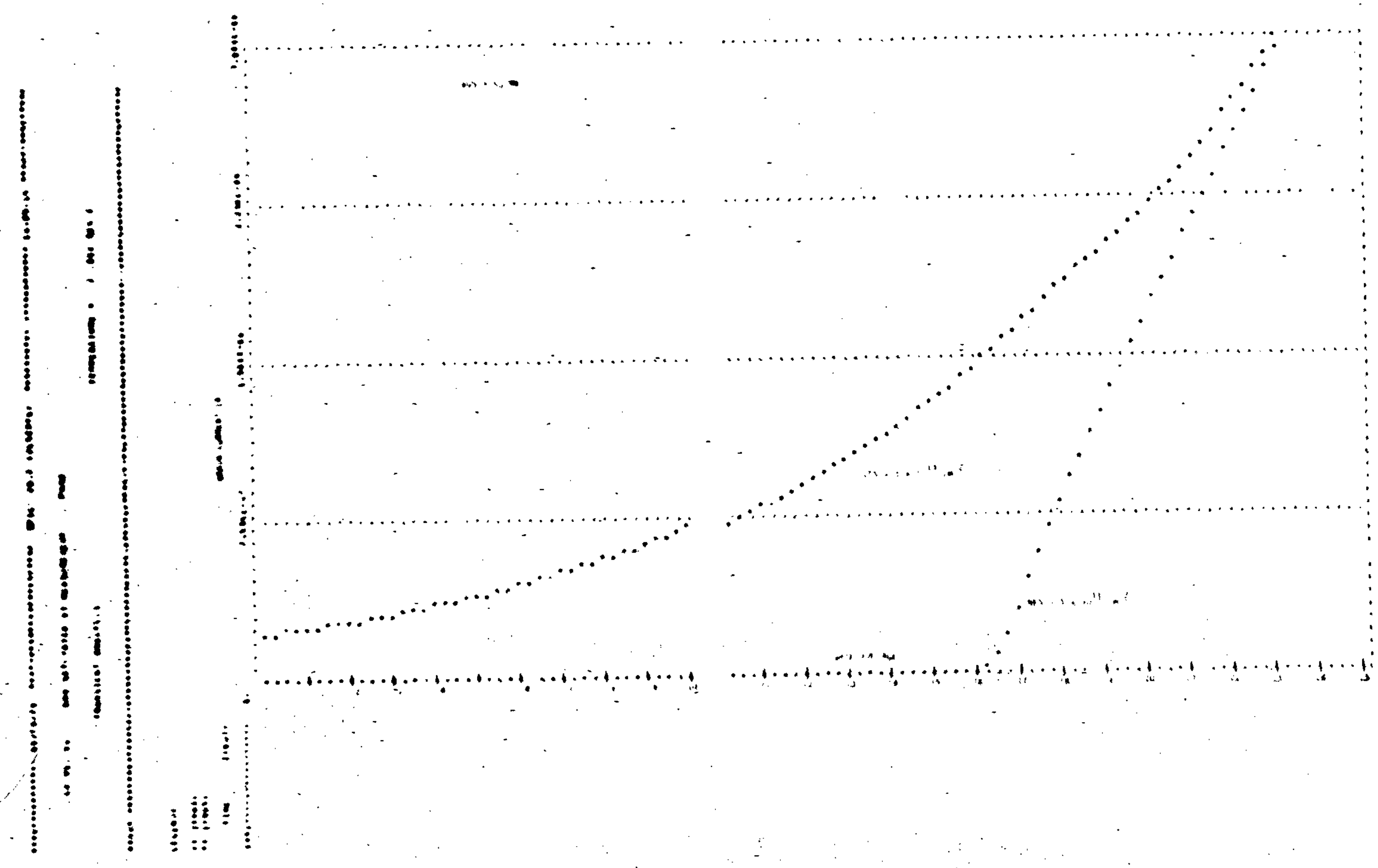
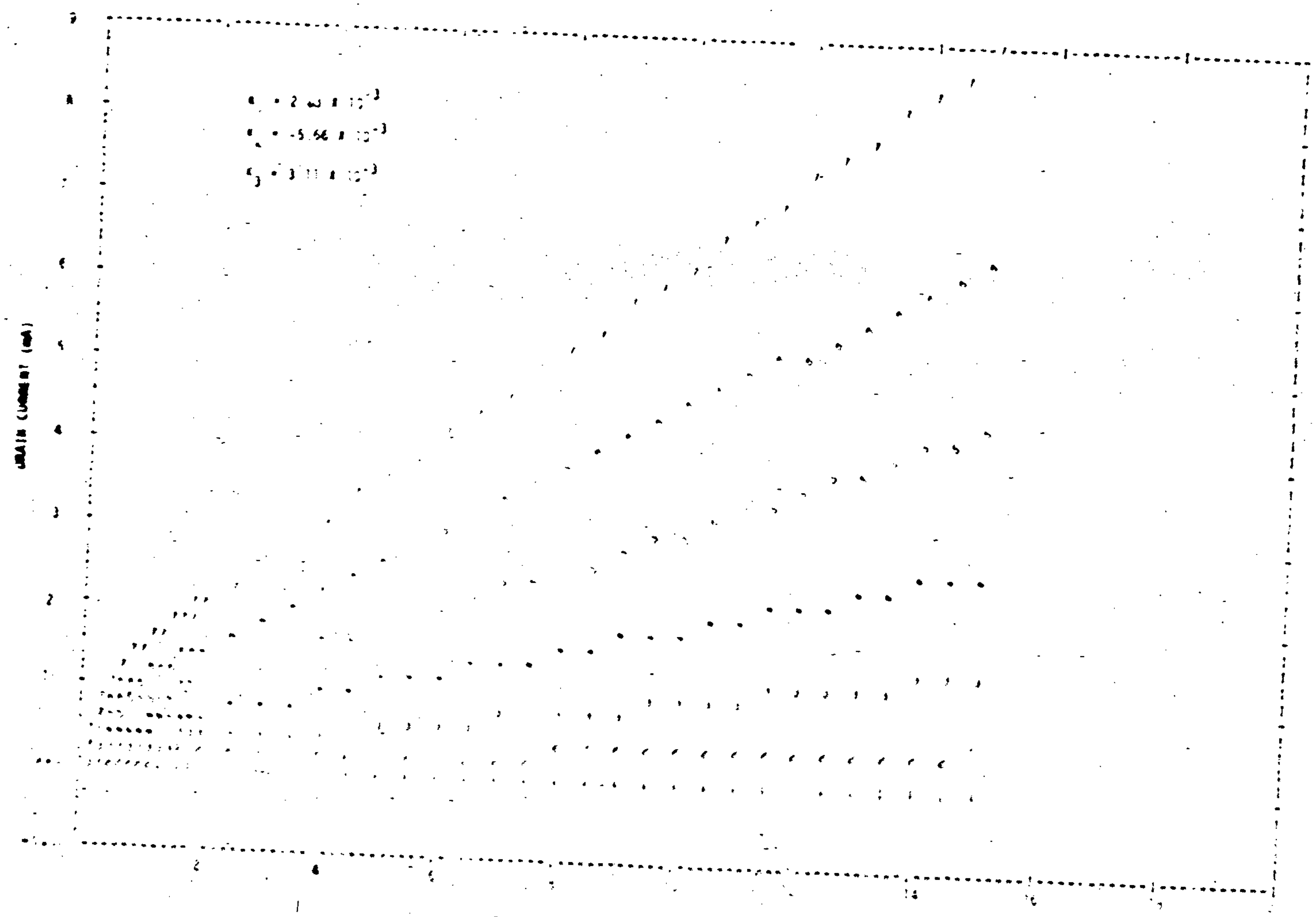
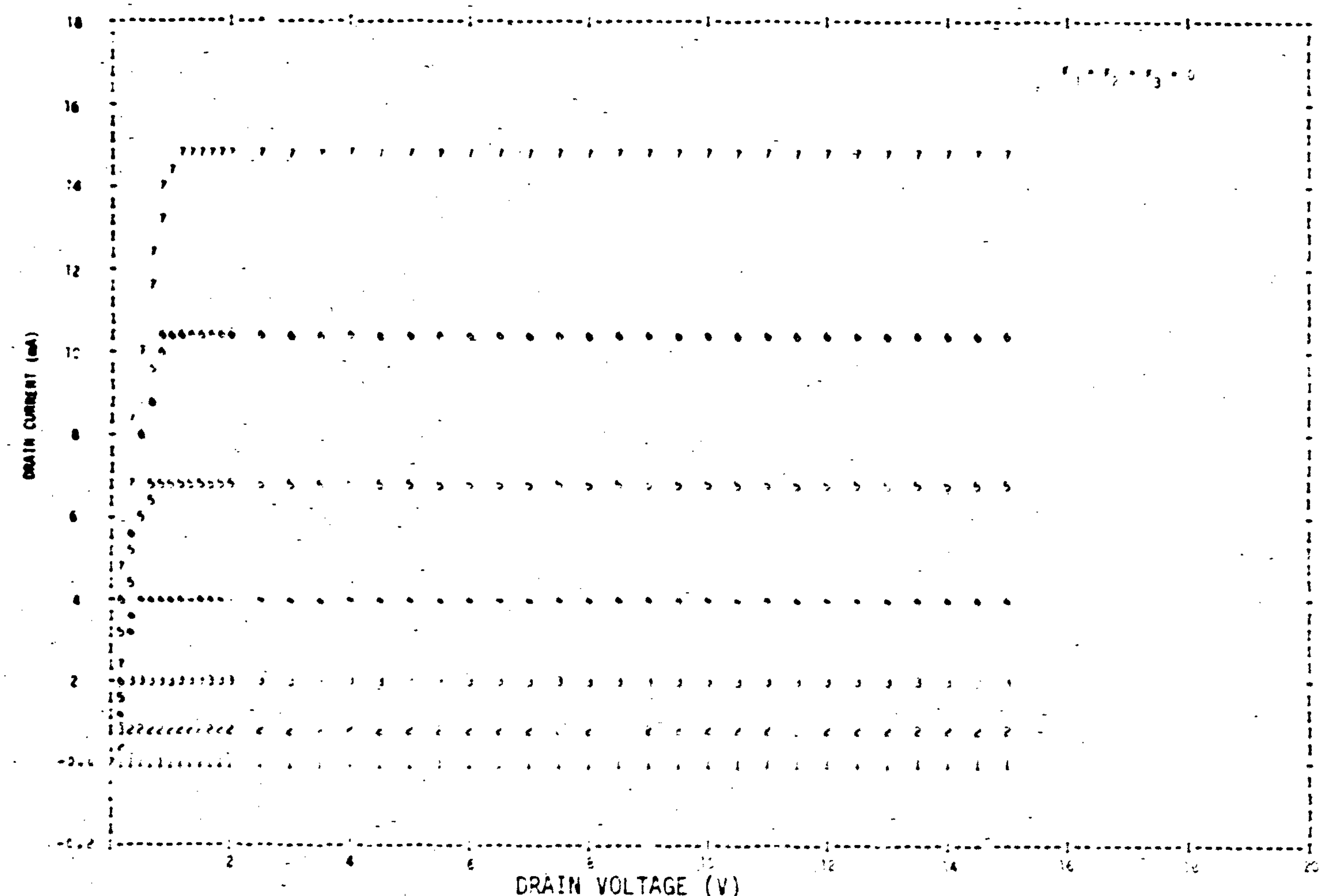


Figure IV-61. SPICE2 P-Channel Model Demonstrating Weak Inversion Effects



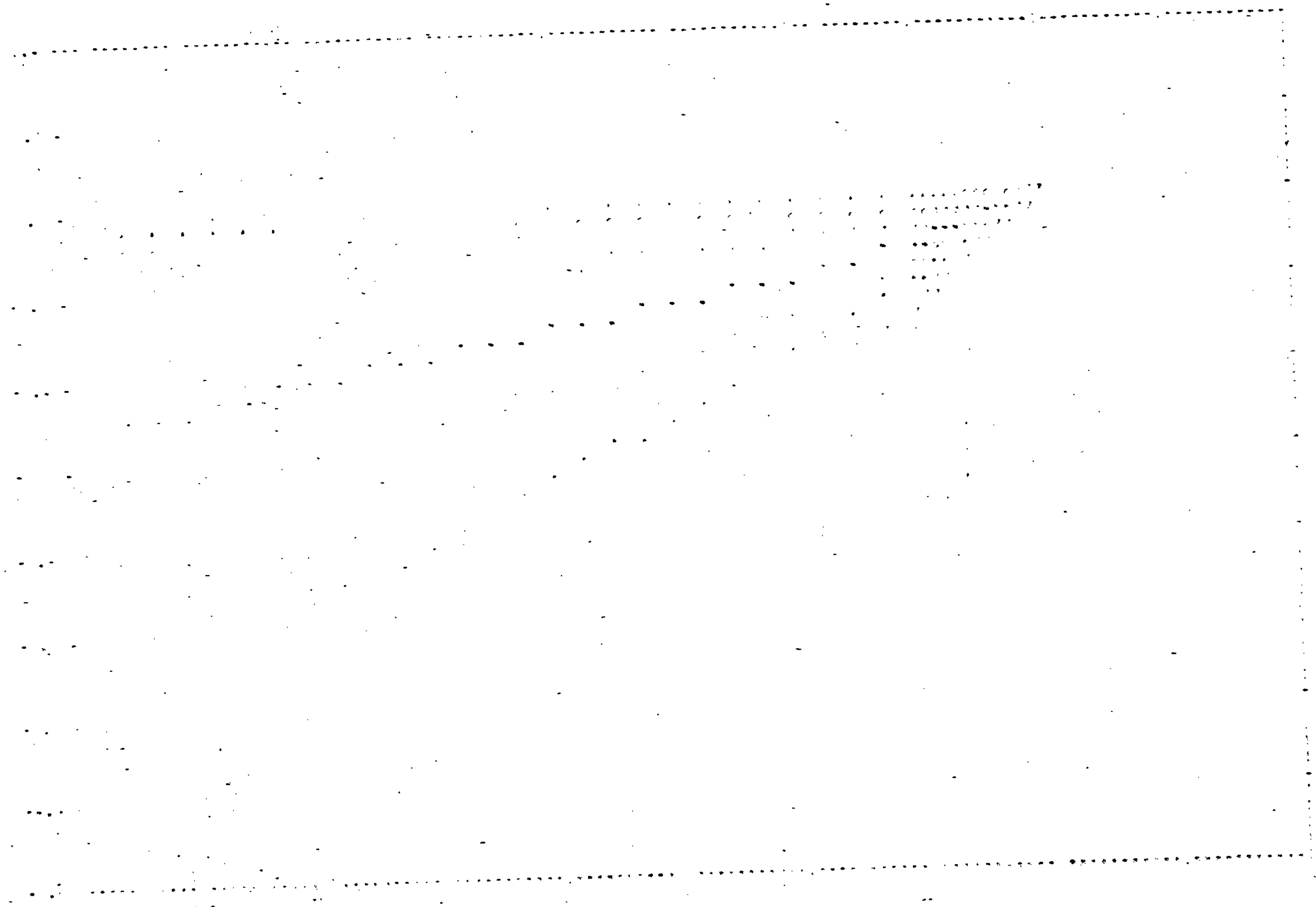
(a) Incomplete Saturation

Figure IV-62. NET-2 N-Channel Model Demonstrating Incomplete Saturation Effects



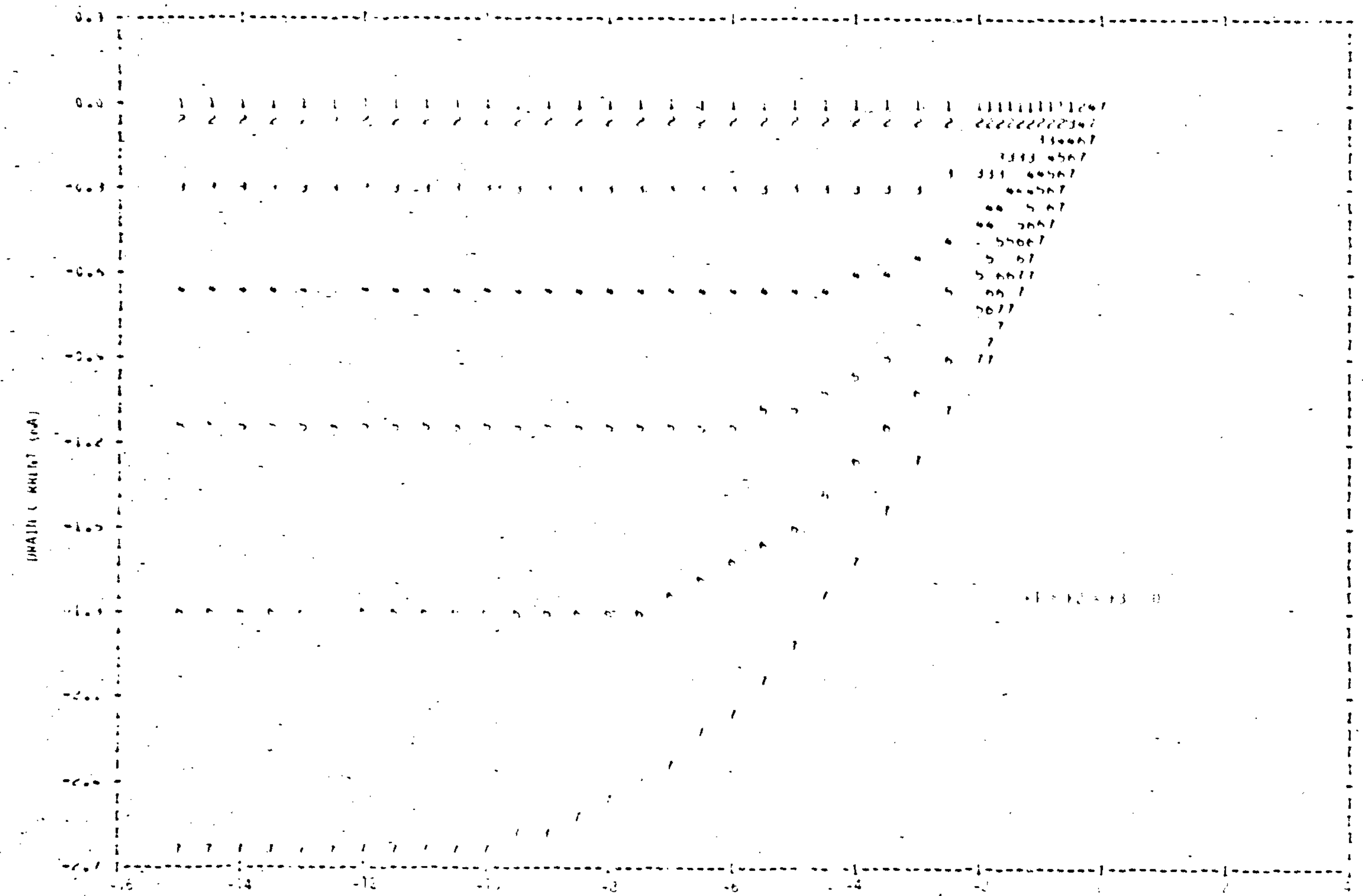
(b) Ideal Saturation

Figure IV-62. :.ET-2 N-Channel Model Demonstrating Incomplete Saturation Effects (Concluded)



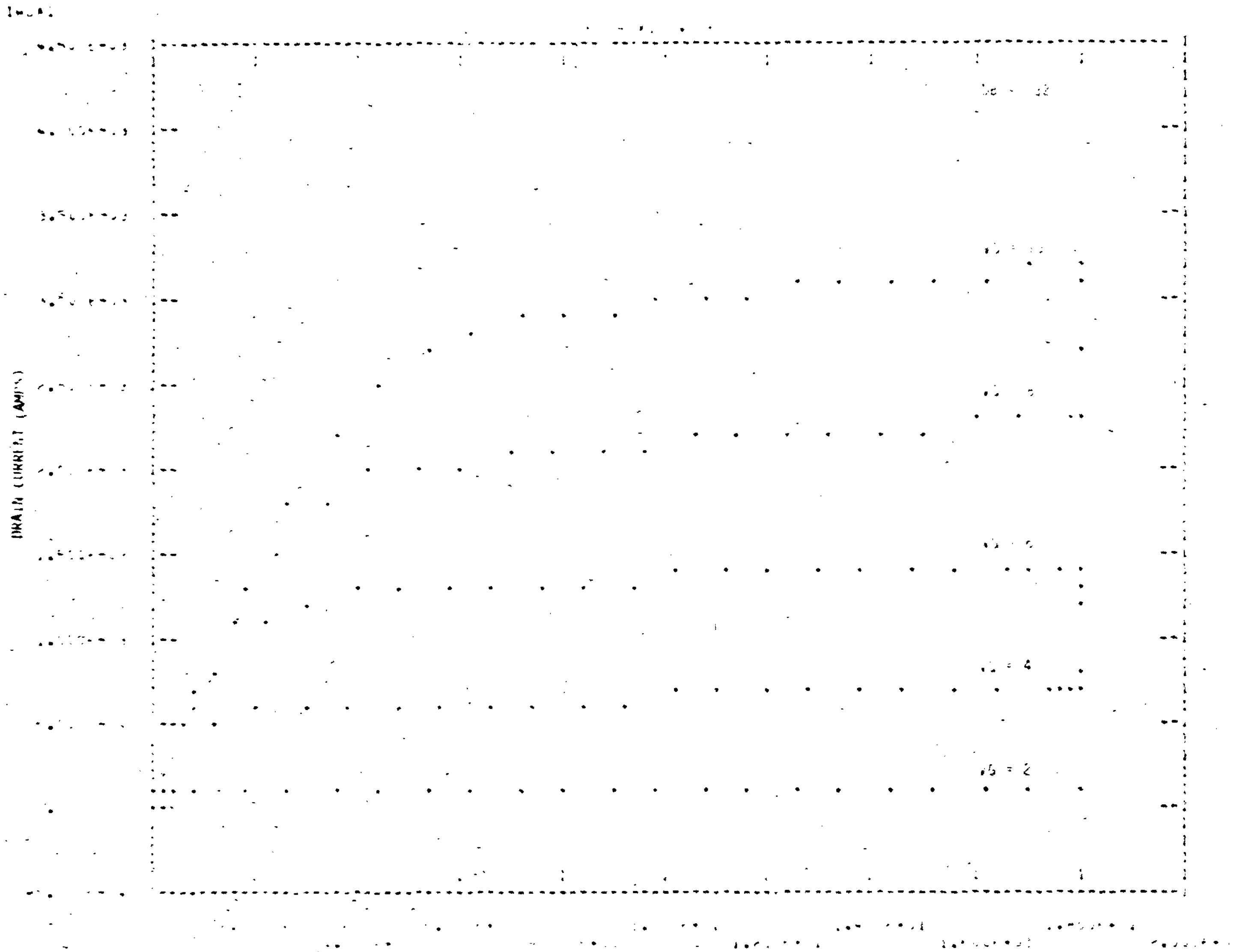
(a) Incomplete Saturation

Figure IV-6[illegible]. NET-2 P-Channel Model Demonstrating Incomplete Saturation Effects



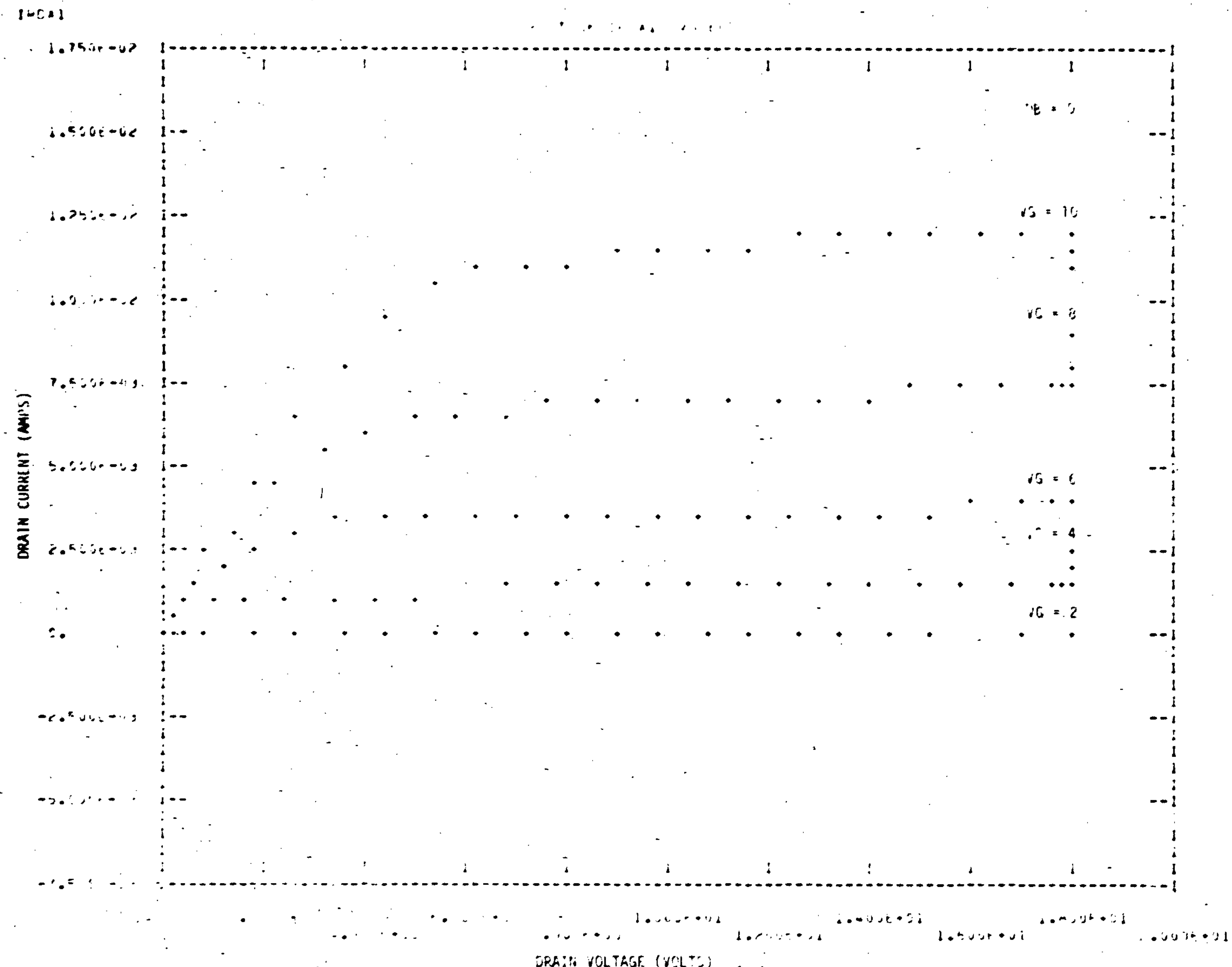
(b) Ideal Saturation

Figure IV-63. NET-2 P-Channel Model Demonstrating Incomplete Saturation Effects (Concluded)



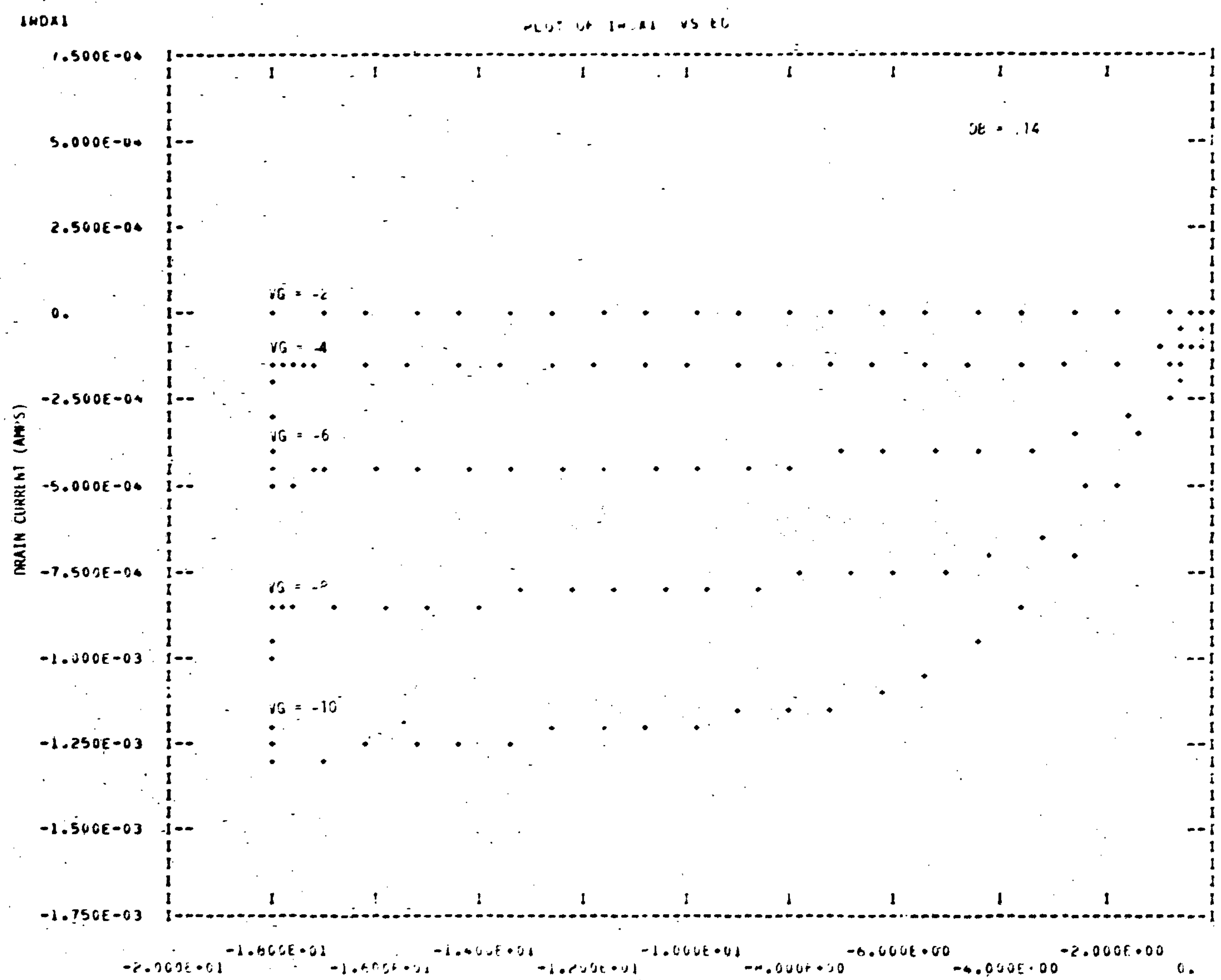
(a) Variable Mobility Effects Included

Figure IV-64. SCEPTRE N-Channel Model Demonstrating Variable Mobility Effects



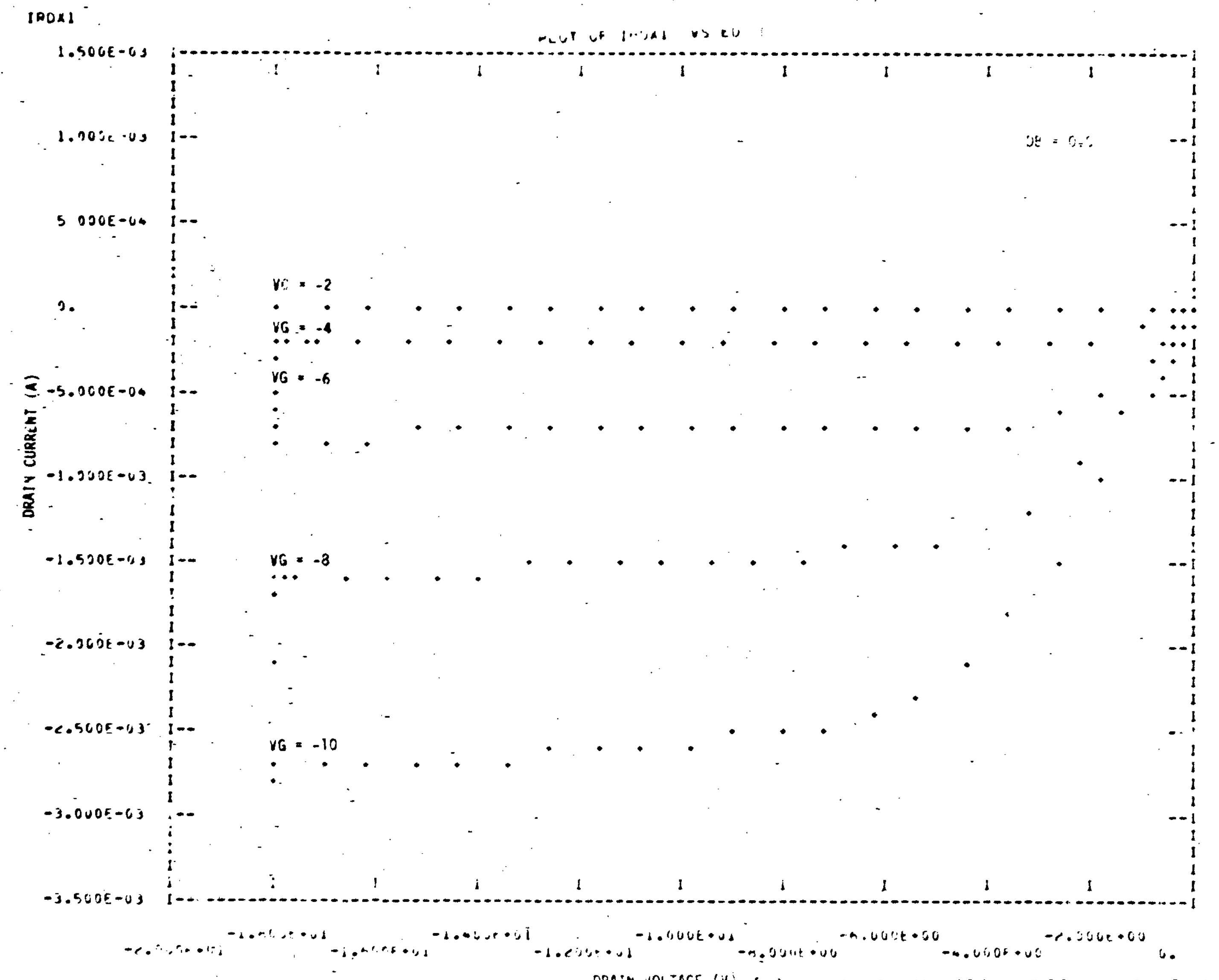
(b) Variable Mobility Effects Excluded

Figure IV-64. SCEPTRE N-Channel Model Demonstrating Variable Mobility Effects (Concluded)



(a) Variable Mobility Effects Included

Figure IV-65. SCEPTRE P-Channel Model Demonstrating Variable Mobility Effects



(b) Variable Mobility Effects Excluded

Figure IV-65. SCEPTRE P-Channel Model Demonstrating Variable Mobility Effects (Concluded)

f. <u>Temperature Effects</u>

Figures IV-66 and IV-67 show the variations in turn on characteristics of N-channel and P-channel devices with temperature as modeled in SPICE2.

F. REFERENCES

IV-1. Meyer, J. E. "MOS Models and Circuit Simulation," RCA Review, vol. 32, March 1971, pp. 42-63.

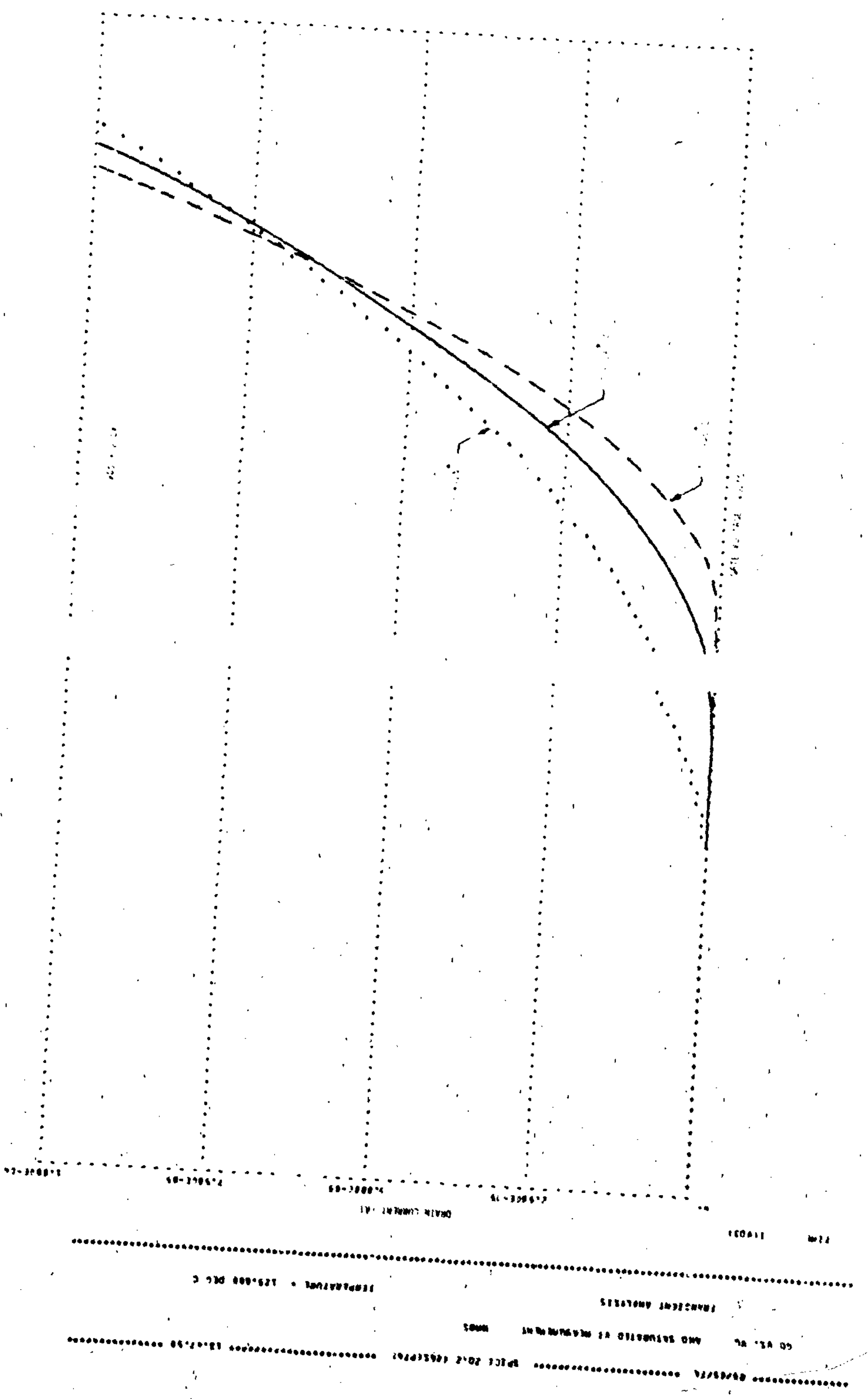


Figure IV-66. SPICE2 N-Channel Model Demonstrating Temperature Effects

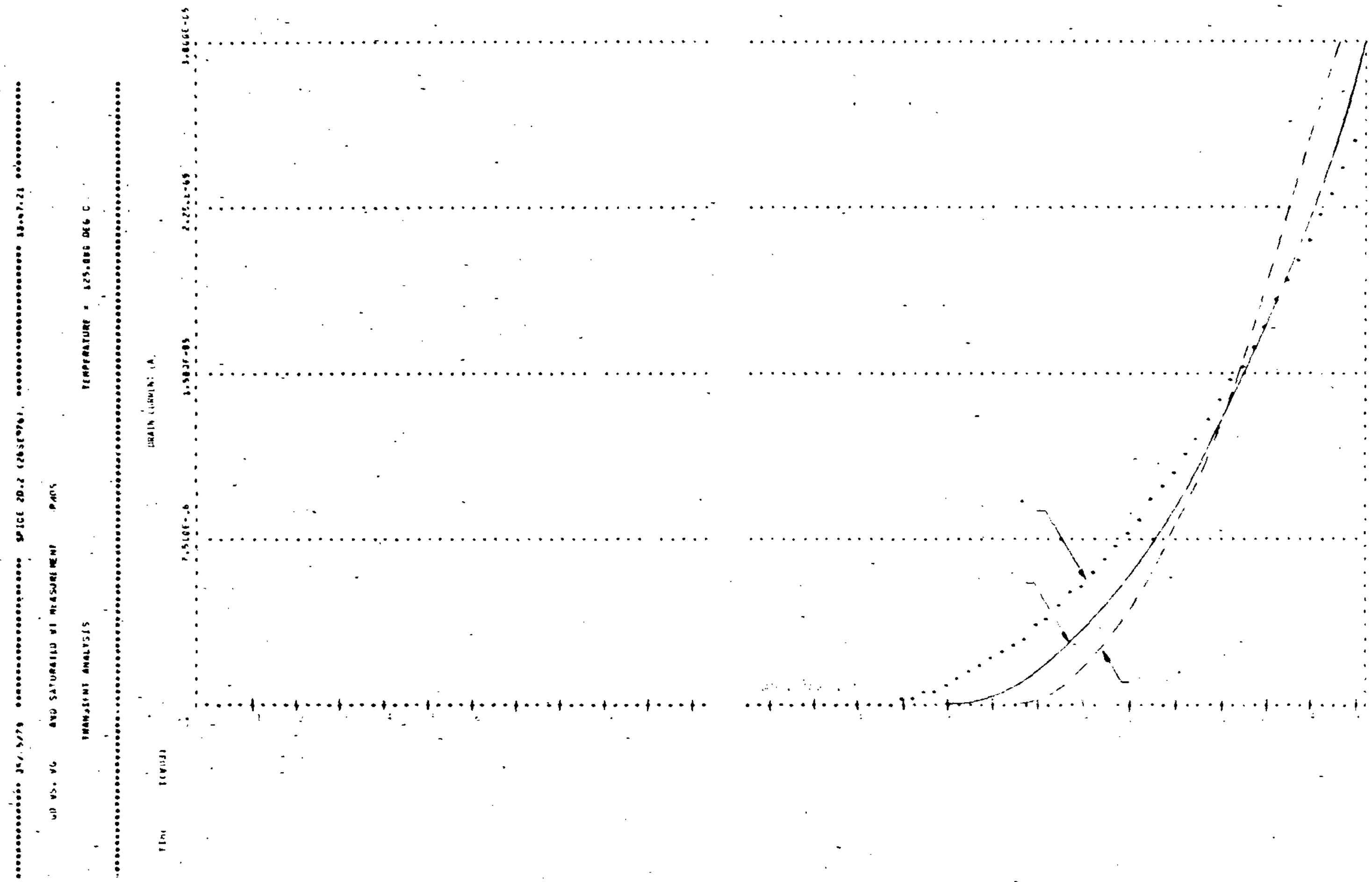


Figure IV-67. SPICE2 P-Channel Model Demonstrating Temperature Effects

CHAPTER V

MISCELLANEOUS DEVICES

CHAPTER V

TABLE OF CONTENTS

CHAPTER V
MISCELLANEOUS DEVICES

A. JFET MODELING

1. Introduction

The JFET (junction field affect transistor) differs from the bipolar transistor in that the depletion region of a reverse biased P-N junction is used to modulate the conduction area available to majority carriers. This is illustrated in figure V-1.

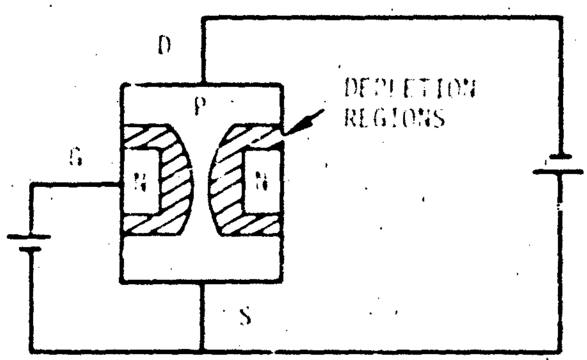


Figure V-1. JFET Geometry

When the depletion regions have not pinched off the channel, the channel behaves as a resistor, and the device is in the linear region. If the gate voltage is increased to the point where the depletion regions pinch off the channel, a saturated current will continue to flow in a manner analogous to the injection current across the reverse biased base-collector junction. Increasing drain voltage in the saturation region will merely widen the depletion regions in a manner so that no net increase in drain current will occur.

2. Basic JFET Model

a. Description

The basic JFET model is a direct implementation of the basic equations which describe JFET operation over various modes of operation.

b. Advantages

The parameterization of the basic JFET model requires only a "curve tracer" photograph. The model can be used for most practical applications.

c. Cautions

The basic JFET model does not include any second order effects beyond channel shortening effects. Discontinuities in the derivative of the characteristic exist at the transition between operating regions. High frequency characteristics are not included.

d. Characteristics

The topology of the basic JFET model is given in figure V-2. The characteristic produced by the basic JFET model is shown in figure V-3.

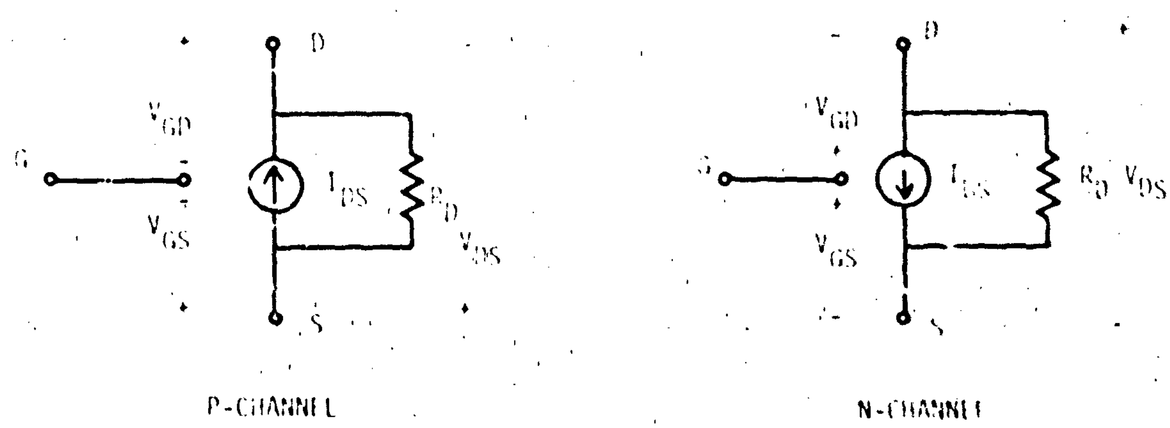


Figure V-2. JFET Topology

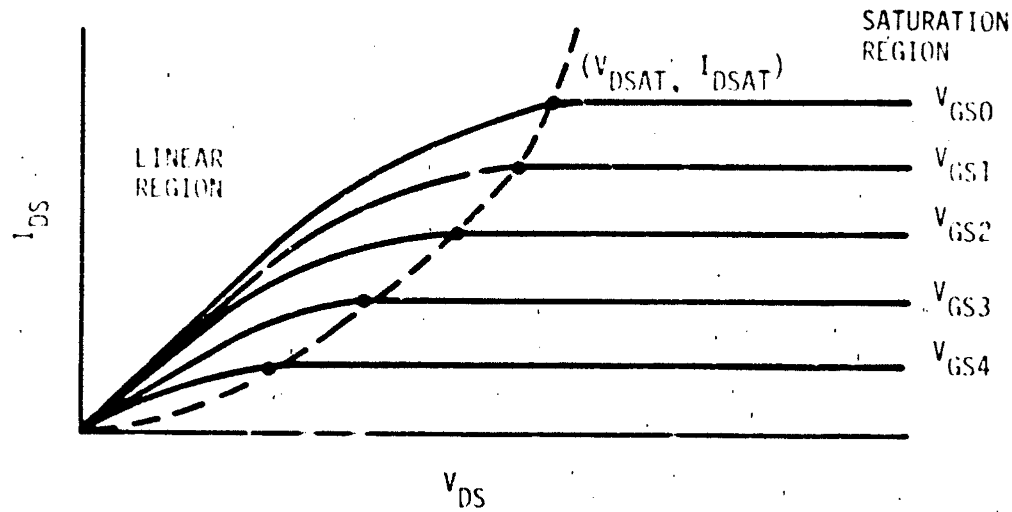


Figure V-3. JFET Characteristics

e. Defining Equations

If $V_{GD} \geq V_T$ and $V_{GS} \geq V_T$,

then $$I_{DS} = G_C \left\{ V_{GS} - V_{GD} + \frac{2}{3\sqrt{V_P}} \left[\left(-V_{GS} + \phi_B \right)^{3/2} - \left(-V_{GD} + \phi_B \right)^{3/2} \right] \right\}$$

(Linear Region)

If $V_{GD} < V_T$ and $V_{GD} < V_{GS}$,

then $$I_{DS} = G_C \left[V_{GS} + \frac{V_P}{3} - \phi_B + \frac{2}{3\sqrt{V_P}} \left(-V_{GS} + \phi_B \right)^{3/2} \right]$$

(Pinchoff Region)

If $V_{GS} < V_T$ and $V_{GS} < V_{GD}$,

then
$$I_{DS} = -G_C\left[V_{GD} + \frac{V_P}{3} - \phi_B + \frac{2}{3\sqrt{V_P}}(-V_{GD} + \phi_B)^{3/2}\right]$$

(Inverted Region)

If $V_{GD} = V_{GS}$ or ($V_{GD} < V_T$ and $V_{GS} < V_T$), then $I_{DS} = 0$.

(Cutoff Region)

If $V_{GD} > \phi_B$ or $V_{GS} > \phi_B$, then $I_{DS} = 0$.

(Forward Biased Forbidden Region)

$$V_T = \phi_B - V_P$$

For all regions:

$$R_D = \frac{I_T \cdot R_O}{I_{DS} + K}$$

f. Parameter List

I_{DS} = drain-to-source current generator

V_P = the pinchoff voltage

ϕ_B = the junction contact potential

V_{GS} = the gate-to-source voltage

V_{GD} = the gate-to-drain voltage

R_D = the resistance which models the variation in drain current with drain-to-source voltage in the pinchoff region with $V_{GS} = 0$

I_T = the drain-to-source current for $V_{GS} = 0$ and drain-to-source voltage $= -|V_T|$

K = the current chosen to reduce the V_{DS}/R_D ratio to a small leakage current when $I_{DS} = 0$

G_C = the channel conductance

g. Parameterization

1) V_p, G_C, ϕ_B

a) Definition

V_p is the device pinchoff voltage. It is the gate voltage required to pinch off the device channel. G_C is the conductance of the device channel. ϕ_B is the built-in voltage of the P-N junction.

b) Typical Values

A typical value of V_p is 2 V. A typical value of G_C is 1×10^{-3} A/volt. ϕ_B has a typical value of about 0.6 V.

c) Measurement

The parameters V_p, G_C, and ϕ_B may be obtained from the saturation region of the device characteristic. This region is illustrated in figure V-3. V_p, G_C, and ϕ_B are found using the following process:

(1) Assume a value for ϕ_D.

(2) Guess V_{DSSAT} for the $V_{GS} = 0$ trace.

(3) Calculate V_p as:

$$V_p = |\phi_B| + |V_{DSSAT}|$$

(4) Calculate G_C as:

$$G_C = \frac{I_{DS}}{\frac{|V_p|}{3} - |\phi_B| + \frac{2}{3\sqrt{|V_p|}}\left(|\phi_B|\right)^{3/2}}$$

(5) Substitute values of V_{GS} from the curve trace in:

$$I_{DS} = G_C\left[-|V_{GS}| + \frac{|V_p|}{3} - |\phi_B| + \frac{2}{3\sqrt{|V_p|}}\left(|V_{GS}| + |\phi_B|\right)^{3/2}\right]$$

(6) Compare the values from step (5) with the measured values of drain current in the saturation region at:

$$V_{DS} = \left[-\left|V_{GS}\right| + \left|V_p\right| - \left|\phi_B\right| \right]$$

(7) If the comparison is unsatisfactory, guess another value for V_{DSSAT} and repeat the process.

d) Example -2N5462

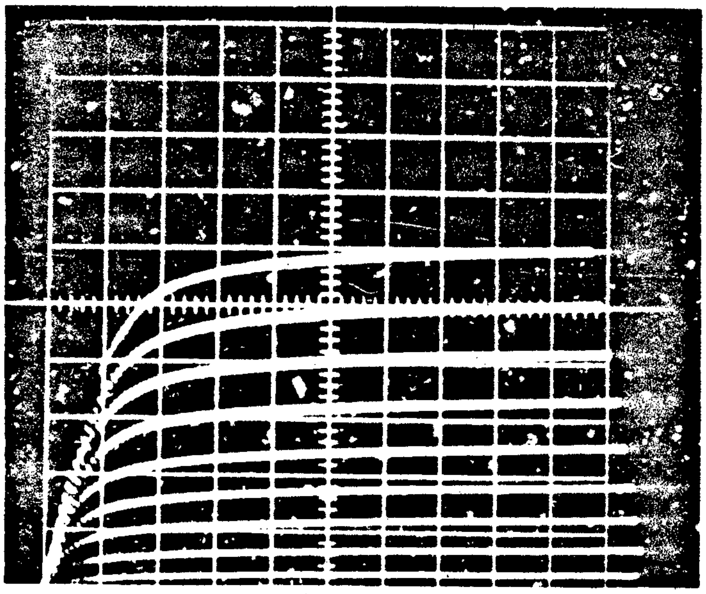
From measurement, V_p, G_C, and ϕ_B can be obtained from the curve tracer photograph shown in figure V-4. The iterative procedure outlined in the parameterization section was implemented using a programmable calculator.

ϕ_B was assumed to be 1 volt. When the point V_{DS} = 13 V at V_{GS} = 0 V and I_{DS} = 5.9 mA at V_{GS} = 0 V was chosen as the saturation point, the results shown in table V-1 were obtained. When the decision was made that a reasonable fit existed between the measured and calculated drain current, the values of V_p and G_C were:

V_p = 14 volts
G_C = 1.53 x 10^{-3} siemens

TABLE V-1. PARAMETER DETERMINATION

V_{GS}	V_{DS}	I_{DS}	I_{DS} (Actual)
0 V	13 V	5.90 mA	5.9 mA
1	12	4.87	4.9
2	11	3.98	4.1
3	10	3.21	3.2
4	9	2.55	2.4
5	8	1.97	1.7
6	7	1.48	1.1
7	6	1.07	0.4
8	5	0.733	0.2



-20 V/div Horiz.
-1 mA/div Vert.
1 V/Trace

Figure V-4. 2N5462 Characteristic

2) R_0, I_T, K

a) Definition

R_0, I_T, and K are parameters that describe R_D. R_D is a variable resistance that models the variation of I_{DS} with V_{DS} in the saturation region.

b) Typical Values

Typical values for R_0, I_T, and K are 30 kilohms, 5 mA, and 0.1 μA, respectively.

c) Measurement

R_0 may be determined from two points on the drain-to-source characteristic for $V_{GS} = 0$. The first point occurs at V_{DSSAT} and I_{DSSAT} for $V_{GS} = 0$. The second point is chosen on the $V_{GS} = 0$ curve to yield the best simulation of the change in drain current with drain to source voltage in the saturation region. R_0 is then calculated from:

$$R_0 = \frac{\Delta V_{DS}}{\Delta I_{DS}} \text{ at } V_{GS} = 0$$

I_T is I_{DSSAT} at $V_{GS} = 0$

K is assigned an arbitrary value for most applications, generally less than 1 μA.

d) Example 2N5462

The first point chosen is at the breakpoint between the saturation and triode region. This point was found in the previous section to be:

$V_{DS} = 13$ V
$I_{DS} = 5.9$ mA

The next point was chosen to be:

$$V_{DS} = 18\ V$$
$$I_{DS} = 6\ mA$$

$$R_0 = \frac{18\ V - 13\ V}{5\ mA - 5.9\ mA} = 5 \times 10^4\ \text{ohms}$$

I_T is fixed as 5.9 mA and K was chosen as 0.1 microampere.

3. Addition of Parasitic Capacitance

a. Description

If a JFET model is to be included in a circuit where high frequencies are present, parasitic capacitances should be included as part of the model.

b. Advantages

The inclusion of the junction capacitors produces a more realistic and useful model of the JFET.

c. Cautions

Three terminal capacitance measurements are required for determination of the capacitance parameters. The capacitance bridge must have the ability to apply a dc bias.

d. Characteristics

Inclusion of the capacitors in the JFET model will produce the topology of figure V-5.

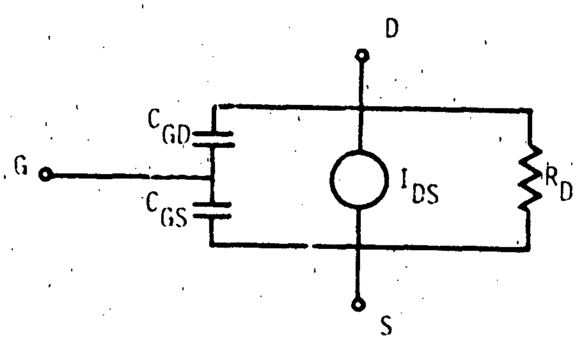


Figure V-5. JFET Parasitic Capacitance

C_{GD} and C_{GS} are depletion region capacitors, and have the voltage dependent characteristics of depletion region capacitance.

e. Defining Equations

$$C_{GD} = \frac{C_D}{\left(\phi_B - V_{GD}\right)^{n_D}}$$

$$C_{GS} = \frac{C_G}{\left(\phi_B - V_{GS}\right)^{n_G}}$$

f. Parameterization (C_G, C_D, n_G, n_D)

1) Definition

C_G, C_D, n_G, and n_D are parameters which describe the two junction capacitors C_{GS} and C_{GD}. n_D and n_G are related to the doping distribution at the junction. C_D and C_G are constants of the capacitance equations.

2) Typical Values

Typical values of C_G and C_D are 5 pF and 1 pF, respectively. n_G and n_D generally lie between 0.5 and 0.333.

3) Measurement

The values for these parameters are obtained from measurements of C_{iss} as a function of gate-to-source voltage and C_{rss} as a function of gate-to-drain voltage. Example test fixtures are given in figure V-6.

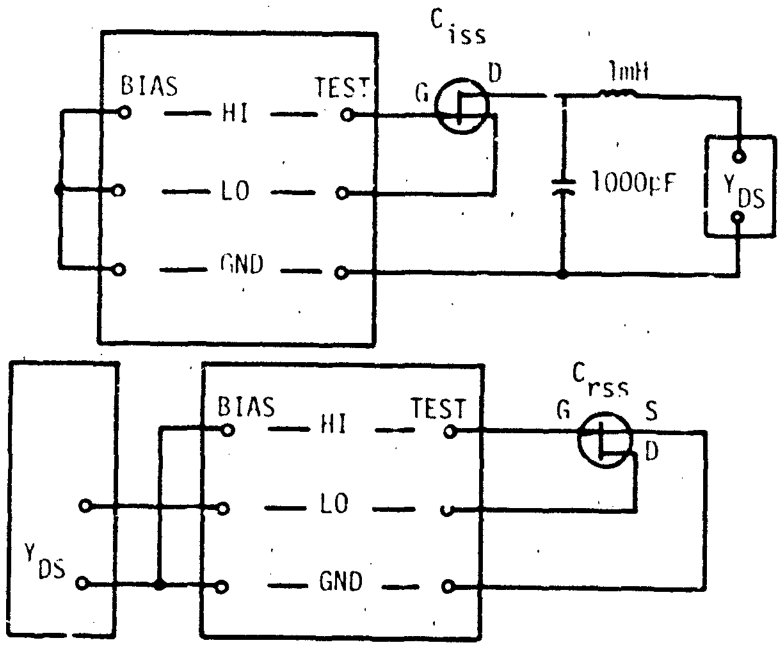


Figure V-6. Capacitance Measurement

For the C_{iss} measurement, the drain-to-source voltage is kept constant and C_{iss} is then measured for a range of gate-to-source voltages. For the C_{rss} measurement, the drain-to-source voltage and the gate-to-source voltage are varied. The following expressions may now be applied:

$$C_{GS} = C_{iss} - C_{rss}$$

$$C_{GD} = C_{rss}$$

From two points on the curve of C_{GS} versus voltage, the value for n_G is:

$$n_G = \frac{\ell n\,(C_{GS1}) - \ell n\,(C_{GS2})}{\ell n\,(\phi_B - V_2) - \ell n\,(\phi_B - V_1)}$$

C_G is then calculated from one C-V point as:

$$C_G = C_{GS}\left(\phi_B - V\right)^{n_G}$$

n_D is determined in a similar manner as:

$$n_D = \frac{\ell n\,(C_{GD1}) - \ell n\,(C_{GD2})}{\ell n\,(\phi_B - V_2) - \ell n\,(\phi_B - V_1)}$$

C_D is calculated from one C-V point as:

$$C_D = C_{GD}\left(\phi_B - V\right)^{n_D}$$

g. Example - 2N5462

Reduced and raw capacitance data are shown in tables V-2 and V-3. The voltage behavior of C_{GS} and C_{GD} is illustrated in figures V-7 and V-8, respectively.

n_G can now be calculated from two arbitrarily chosen points as shown in tables V-2 and V-3.

$$n_G = \frac{\ell n\,(3.55\ \text{pF}) - \ell n\,(2.38\ \text{pF})}{\ell n\,[1\ \text{V} - (-10\ \text{V})] - \ell n\,[1\ \text{V} - (-0\ \text{V})]}$$

$$n_G = 0.167$$

C_G can be calculated at the (-0.5 V, 3.08 pF) point as:

$$C_G = 3.08\ \text{pF}\ [1\ \text{V} - (-0.5\ \text{V})]^{0.167}$$

$$C_G = 3.31\ \text{pF}$$

TABLE V-2. DRAIN CAPACITANCE MEASUREMENTS

V_{BD}	V_{GS}	$V_{GD} = V_{DS} - V_{GS}$	$C_{rss} = C_{GD}$
-0.5 V	0 V	-0.5 V	~55 pF
-1.0	0	-1.0	~8.00
-2.0	0	-2.0	3.22
-5.0	0	-5.0	2.42
-10.0	0	-10.0	2.20
-10.0	0.5	-10.5	2.18
-10.0	1.0	-11.0	2.14
-10.0	2.0	-12.0	2.12
-10.0	5.0	-15.0	2.02
-10.0	10.0	-20.0	1.92

TABLE V-3. GATE CAPACITANCE MEASUREMENTS

V_{DS}	V_{GS}	C_{iss}	$C_{GS} = C_{iss} - C_{rss}$			$@V_{DS} = -10$ V
-10 V	0 V	5.75 pF	5.75 pF	- 2.2 pF	=	3.55 pF
-10	0.5	5.26	5.26	- 2.18	=	3.08
-10	1.0	5.07	5.07	- 2.14	=	2.93
-10	2.0	4.85	4.85	- 2.12	=	2.73
-10	5.0	4.51	4.51	- 2.02	=	2.49
-10	10.0	4.30	4.30	- 1.92	=	2.38

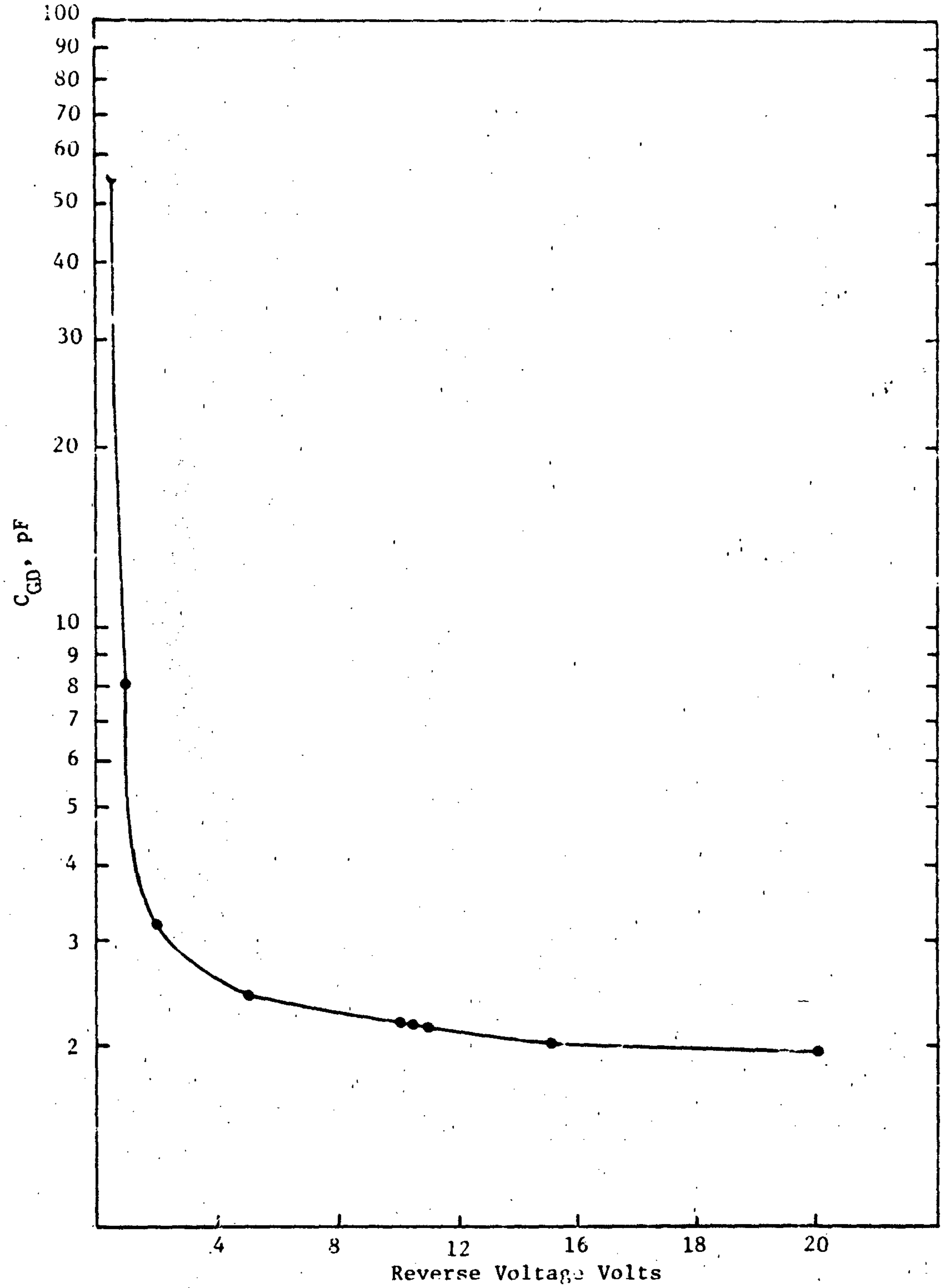


Figure V-7. C_{GD} as a Function of V_{GD}

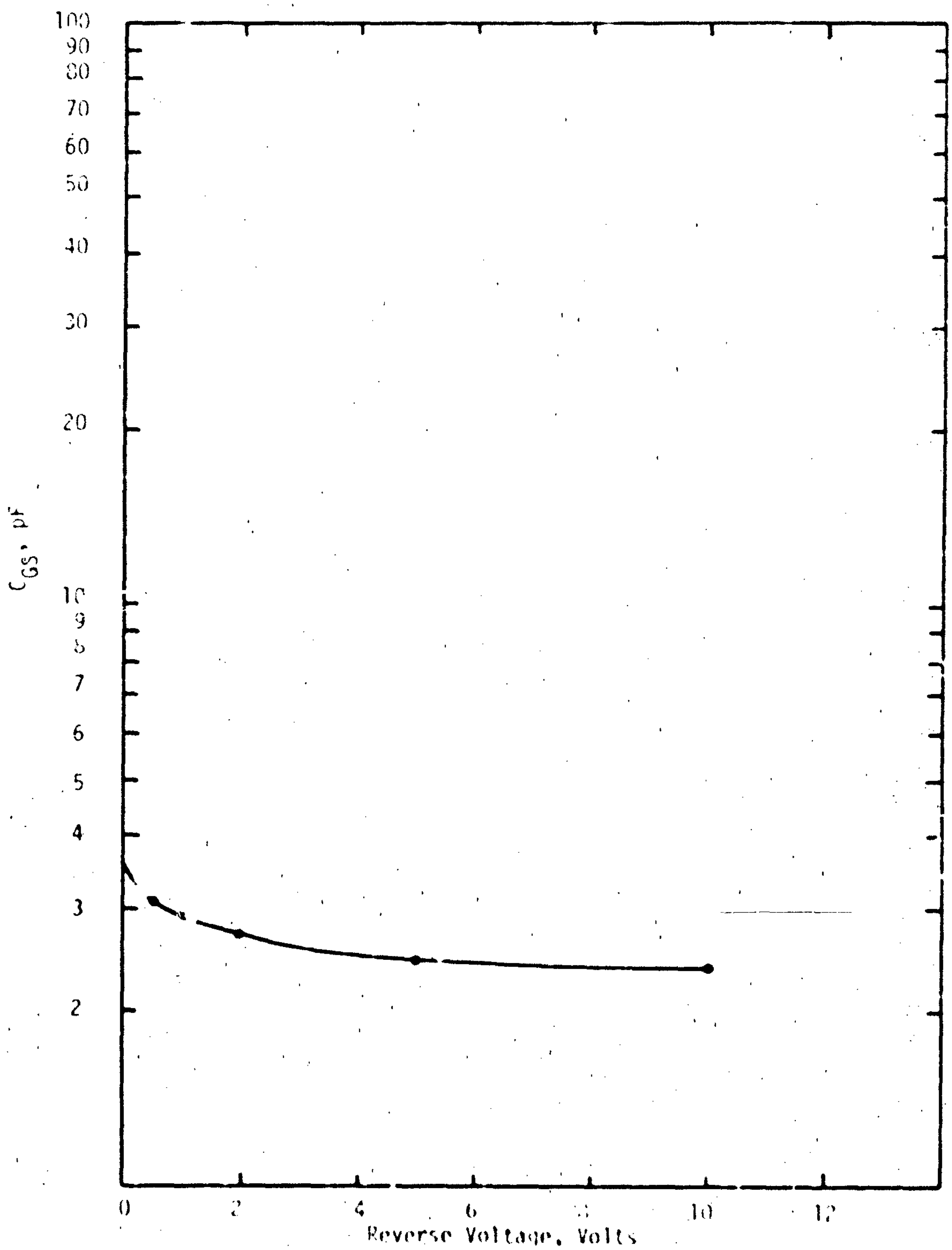


Figure V-8. C_{GS} as a Function of V_{GS}

n_D can be found in the same manner as n_G:

$$n_D = \frac{\ln (3.22 \text{ pF}) - \ln (1.92 \text{ pF})}{\ln [1 \text{ V} - (-20 \text{ V})] - \ln [1 \text{ V} - (-2 \text{ V})]}$$

$$n_D = 0.266$$

C_D can now be calculated at the (-10 V, 2.2 pF) point as:

$$C_D = 2.2 \text{ pF } [1 \text{ V} - (-10 \text{ V})]^{0.266}$$

$$C_D = 4.16 \text{ pF}$$

4. Data Sheet JFET Model Development

Parameters for the JFET model can be determined from the manufacturer specification sheets.

a. V_P

The pinchoff voltage is often listed as V_{GS} (cutoff), gate-to-source cutoff voltage. The data sheets shown in figure V-9 list V_P ($V_{GS(OFF)}$) between 1.0 V and [illegible] 5 V. The unrealistically large value of derived V_P, [illegible] V, is explained by the failure of this simple model to accurately reflect such second order effects as variable mobility, inhomogeneous doping, and varying charge distribution. The net effect is that while the saturation region is adequately modeled, significant errors exist in the modeling of the linear region.

b. G_C

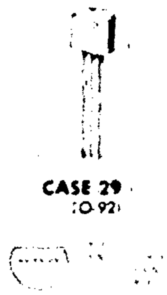
G_C, the channel conductance parameter, is often found in data sheets as Y_{FS}, the forward transadmittance. For the 2N5462, Y_{FS} is listed between 2000 and 6000 µS. The derived value was 1530 µS.

c. C_{GD}

C_{GD}, the gate-to-drain capacitance, is often found as C_{rss}, the reverse transfer capacitance. For the 2N5462, C_{rss} is plotted as a function of V_{DS} in figure V-9.

2N5460 (SILICON)
thru
2N5465

P-channel depletion mode (Type A) junction field-effect transistors designed for use in general-purpose amplifier applications.



CASE 29
(TO-92)

MAXIMUM RATINGS

Rating	Symbol	2N5460 2N5461 2N5462	2N5463 2N5464 2N5465	Unit
[illegible]	[illegible]	40	60	Vdc
Reverse Gate-Source Voltage	[illegible]	40	60	Vdc
Forward Gate Current	$I_{G(f)}$	10		mAdc
Total Device Dissipation @ T_A = 25°C	P_D	310		mW
Derate above 25°C		2.82		mW/°C
Storage Temperature Range	T_{stg}	-65 to +150		°C
Operating Junction Temperature Range	T_J	-65 to +135		°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
[illegible]	[illegible]	[illegible]		[illegible]	[illegible]
ON CHARACTERISTICS					
[illegible]	[illegible]	[illegible]		[illegible]	[illegible]
SMALL SIGNAL CHARACTERISTICS					
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

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Figure V-9. 2N5460 - 2N5665 Manufacturer Specification Sheets (ref. V-1)

DRAIN CURRENT versus GATE SOURCE VOLTAGE

FIGURE 1 — 2N5460 and 2N5463

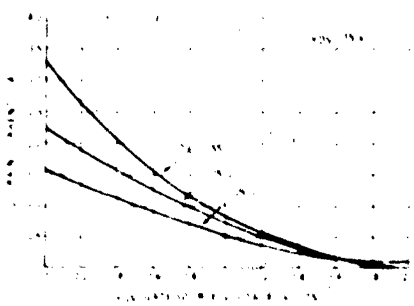


FIGURE 2 — 2N5461 and 2N5464

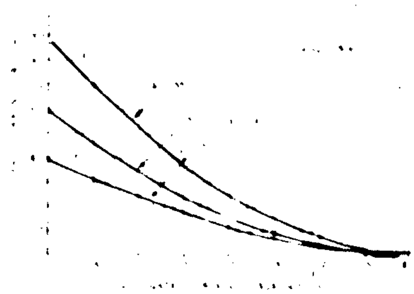
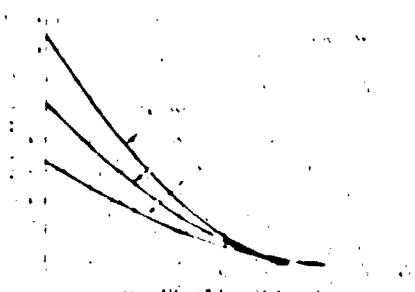


FIGURE 3 — 2N5462 and 2N5465



FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

FIGURE 4 — 2N5460 and 2N5463

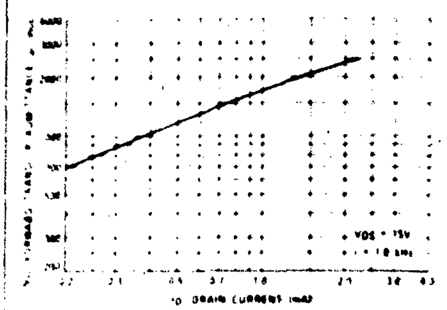


FIGURE 5 — 2N5461 and 2N5464

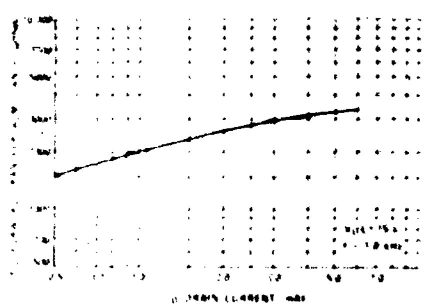


FIGURE 6 — 2N5462 and 2N5465

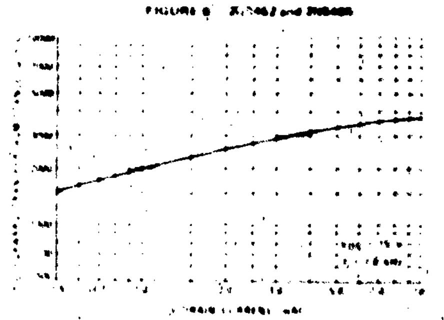


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Figure V-9. 2N5460 - 2N5665 Manufacturer Specification Sheets (Continued)

FIGURE 7 - OUTPUT RESISTANCE VERSUS DRAIN CURRENT

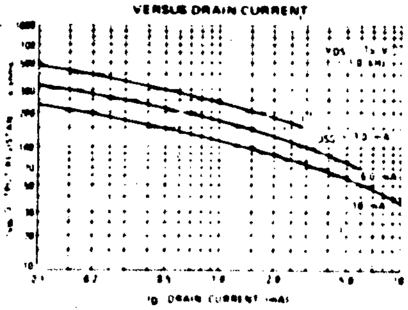


FIGURE 8 - CAPACITANCE VERSUS DRAIN SOURCE VOLTAGE

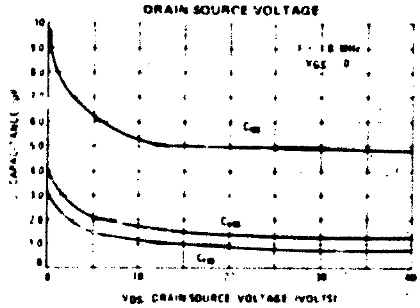


FIGURE 9 - NOISE FIGURE VERSUS FREQUENCY

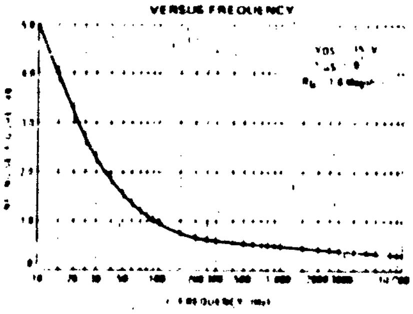


FIGURE 10 - NOISE FIGURE VERSUS SOURCE RESISTANCE

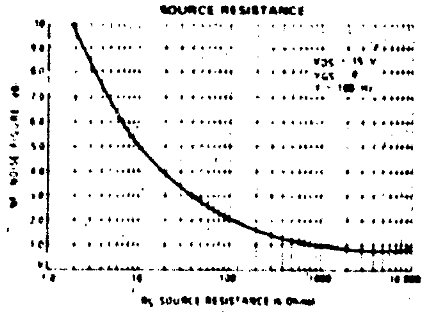


FIGURE 11 - EQUIVALENT LOW FREQUENCY CIRCUIT

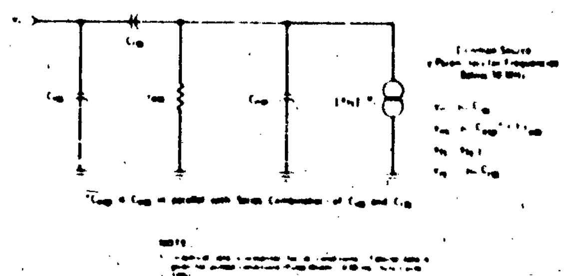


Figure V-9. 2N5460 - 2N5665 Manufacturer Specification Sheets (Concluded)

d. $\underline{C_{GS}}$

C_{GS}, the gate-to-source capacitance, is found from:

$$C_{GS} = C_{iss} - C_{rss}$$

The data sheets shown in figure V-9 list C_{iss} and C_{rss} as a function of V_{DS}.

e. $\underline{R_0}$

R_0, the resistor which models the slope of the characteristic in saturation, can be found a

$$R_0 = \frac{1}{|Y_{OS}|}$$

where Y_{OS} is the output admittance. For the 2N5462, R_0 is determined from Y_{OS} (75 μS max.) to be 13.3 kilohm.

f. $\underline{I_{DSSAT}, V_{DSSAT}}$

An estimate of the $V_{GS} = 0$ saturation drain current and voltage is available from the I_{DSS} parameter. For the 2N5462, I_{DSS} is listed between 4 and 16 mA at a drain voltage of 15 V.

5. Radiation Effects

a. Photocurrents

In the absence of complete information on geometry and doping, photocurrents produced in the JFET may be estimated by the techniques discussed for diodes in chapter II.B.8. The depletion regions which form C_{GD} and C_{GS} will also produce two photocurrents, I_{PGD} and I_{PGS}, shown in figure V-10.

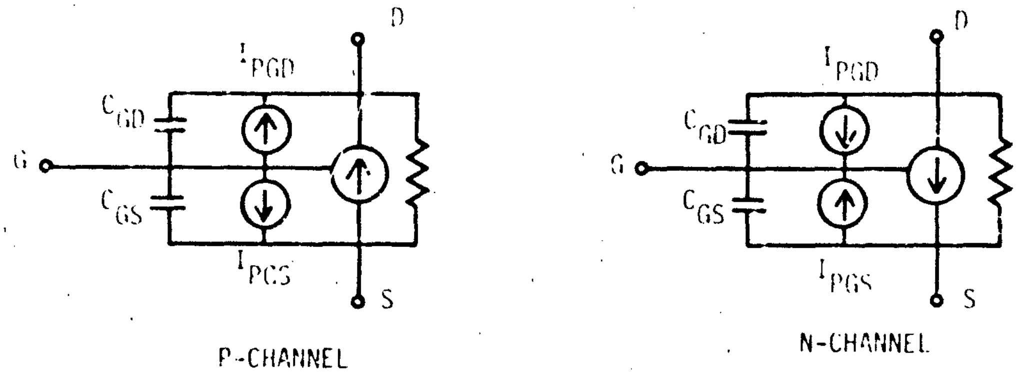


Figure V-10. Photocurrent Generators

The accuracy of photocurrent predictions from terminal measurements for the JFET is questionable since the one dimensional approximation no longer holds. The experimental determination of photocurrent generators is the usual method.

The transient drain photocurrent has been found to be fairly independent of drain-to-source voltage. If the device is operated in the linear region, transient drain photocurrent is also relatively independent of gate-to-source voltage.

b. Neutron Damage

Displacement damage as caused by neutron irradiation alters several JFET parameters. The characteristics of the JFET are sensitive to any changes in the conductivity properties of the channel. Neutron damage will alter the conductivity of the channel through carrier removal, mobility changes, etc. Parameters which are altered include the pinchoff voltage, pinchoff current, and transconductance, all of which decrease.

JFET's appear to be slightly harder to neutron damage than bipolar transistors, because JFET's are affected mainly by bulk resistivity changes, and bipolar transistors are affected by bulk resistivity changes and the increase in recombination center density.

6. <u>Computer Example</u>

The 2N5462 junction field effect transistor was modeled and simulated using the SCEPTRE network analysis code. A FORTRAN subroutine defined I_{DS} (ref. V-1). A curve tracer output was obtained using the RERUN feature of SCEPTRE. The output data were then graphed to obtain a more easily interpreted display. The SCEPTRE circuit used to test the JFET is illustrated in figure V-11. The SCEPTRE input data for the JFET characteristic are given in figure V-12. The model characteristic, figure V-13, may be compared to the photograph shown in figure V-4.

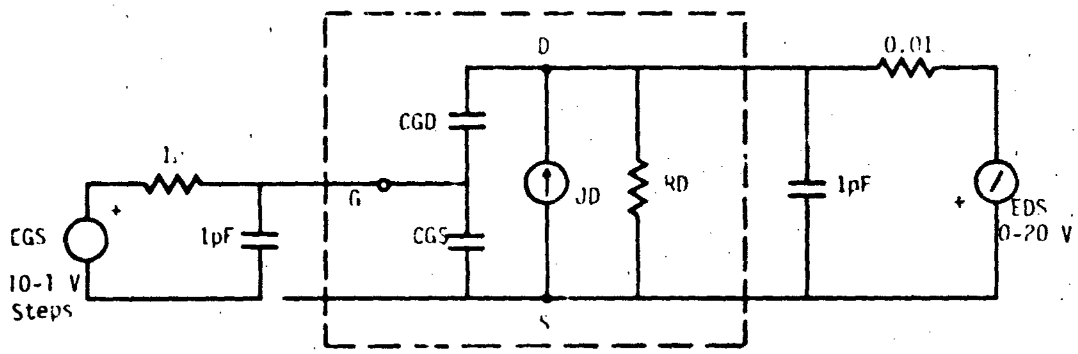


Figure V-11. JFET Test Circuit

The agreement between the characteristic of figure V-13 and the characteristic of figure V-4 is good in the saturation region. In the linear region, however, the model does not agree as well because it fails to take into account the effects of graded doping and varying charge distribution. More complex models may handle these effects. The simulation shown in figure V-13 is based on parameters derived from measurements taken in the saturation region; hence, good agreement is expected in saturation. When dealing with large signal characteristics, the saturation region dominates, so it is important to model it well.

```
S C E P T R E   NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2       5/76
 12/14/77    14.48.15.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD  "DOCUMENT"  AS THE FIRST CARD
OF THE INPUT TEXT



COMPUTER TIME ENTERING SETUP PHASE-
         CPA       .482 SEC.
         PP        0.000 SEC.
         IO        0.000 SEC.


SUBPROGRAM
      FUNCTION FJFET (VGS,VGD,VP,GC,PHI)
C     JFET SUBROUTINE
C     STEP JUNCTION AT GATE TO CHANNEL INTERFACE
C     CHANNEL CURRENT IS SET TO ZERO UPON FORWARD BIAS OF THE GATE TO
C     SOURCE OR GATE TO DRAIN JUNCTIONS GREATER THAN THE BUILT IN
C     POTENTIAL --PHI.
      VT=PHI-VP
      XK=2./(3.*SQRT(VP))
C     CHECK FOR FORWARD BIAS GREATER THAN PHI.
      IF (VGD.GT.PHI.OR.VGS.GT.PHI) GO TO 10
C     CHECK FOR CUTOFF
      IF (VGD.EQ.VGS.OR.(VGD.LT.VT.AND.VGS.LT.VT)) GO TO 10
C     CHECK FOR CHANNEL PINCHOFF.
      IF (VGD.GT.VT.AND.VGS.GT.VT) GO TO 20
C     CHANNEL IS PINCHED-OFF
C     DETERMINE IF THE JFET IS IN THE NORMAL OR INVERTED MODE
      IF (VGS.LT.VT) GO TO 30
C     JFET IS IN THE NORMAL MODE.
      FJFET=GC*(VGS+VP/3.-PHI+XK*(-VGS+PHI)**1.5)
      RETURN
C     GATE TO SOURCE OR GATE TO DRAIN JUNCTION FORWARD BIASED OR CUTOFF.
   10 FJFET=0
      RETURN
C     CHANNEL IS NOT PINCHED-OFF
   20 FJFET=GC*(VGS-VGD+XK*((-VGS+PHI)**1.5-(-VGD+PHI)**1.5))
      RETURN
C     JFET IS IN THE INVERTED MODE.
   30 FJFET=-GC*(VGD+VP/3.-PHI+XK*(-VGD+PHI)**1.5)
      RETURN
      END
```

Figure V-12. JFET Characteristic Input Data

```
MODEL DESCRIPTION
MODEL 2N5462 (G-S-D)
ELEMENTS
CGS,S-G=Q1(3.31E-12,1.,VCGS,.167)
CGD,D-G=Q1(4.16E-12,1.,VCGD,.226)
JD,S-D=FJFET(VCGS,VCGD,14.,1.53E-3,1.0)
RD,S-D=Q2(5.E4,5.9E-3,JD,.1E-6)
FUNCTIONS
Q1(A,B,C,D)=(A/(B-C)**D)
Q2(A,B,C,D)=((A*B)/(C+D))
CIRCUIT DESCRIPTION
ELEMENTS
T1,G-S-D=MODEL 2N5462
EDS,5-S=TABLE 1(TIME)
RS,D-S=0.01
CS,D-S=1.E-12
EGS,S-X=0.
RGS,X-G=1.
CGS,G-S=1.E-12
FUNCTIONS
TABLE 1
0,0,11.E-3,20
OUTPUTS
IEDS,EDS,EGS
RUN CONTROLS
MAXIMUM PRINT POINTS=100
STOP TIME=11.E-3
MINIMUM STEP SIZE=1.E-39
RERUN DESCRIPTION (10)
ELEMENTS
EGS=1,2,3,4,5,6,7,8,9,10
END

SYSTEM NOW ENTERING SIMULATION

COMPUTER TIME AT TERMINATION OF SETUP PHASE-
          CPA      2.793 SEC.
          PP       0.000 SEC.
          IO       0.000 SEC.
```

Figure V-12. JFET Characteristic Input Data (Concluded)

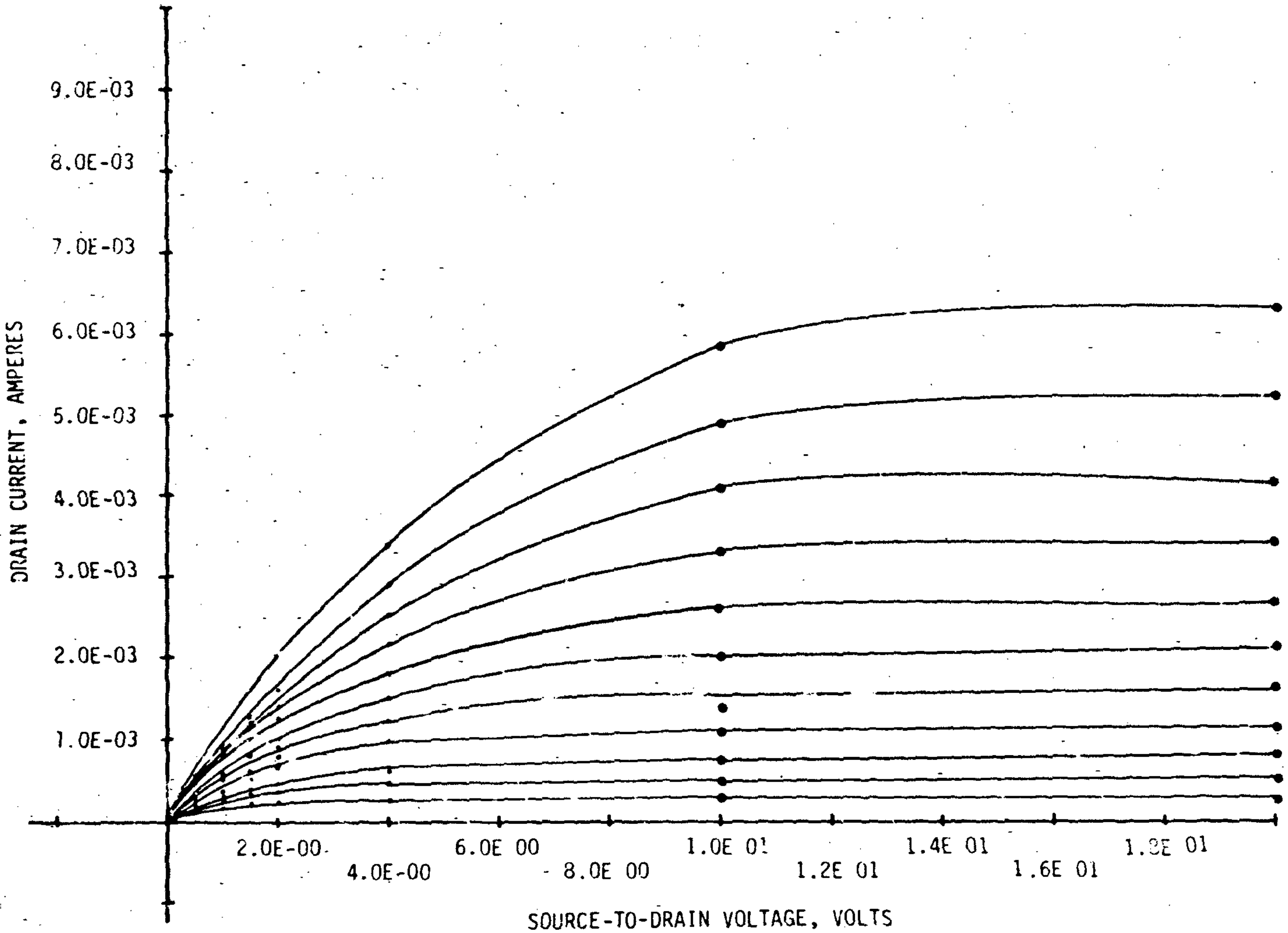


Figure V-13. JFET Model Characteristics

B. UJT MODELING

1. Introduction

The UJT (unijunction transistor) is a bipolar transistor, having one emitter junction and two base contacts. The behavior of the UJT is dependent on modulation of the conductivity between the emitter and base one contact. The UJT topology is shown in figure V-14.

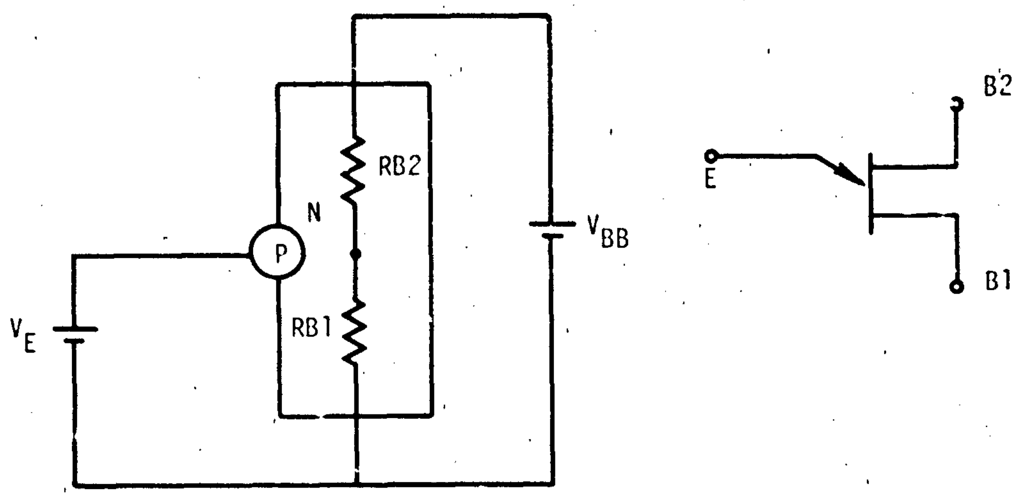


Figure V-14. UJT Topology

The introduction of V_{BB} produces an intermediate voltage between RB2 and RB1 (which forms a voltage divider). When V_E reaches a voltage sufficient to forward bias the P-N junction (which is ηV_{BB} where η is the intrinsic standoff ratio), holes will be injected into the high resistivity N region. The result of these extra carriers will be a reduction of the resistance value of RB1 which lowers the voltage between RB1 and RB2. The P-N junction becomes regeneratively forward biased, and switching occurs.

Two approaches to modeling the UJT are available, the equivalent circuit and the hybrid circuit analytical description. The hybrid

approach yields the superior model, but the analysis code must have a mathematical function capability. The equivalent circuit is shown in figure V-15. The two transistors form a regenerative switching pair. The hybrid model is discussed in detail in the following sections.

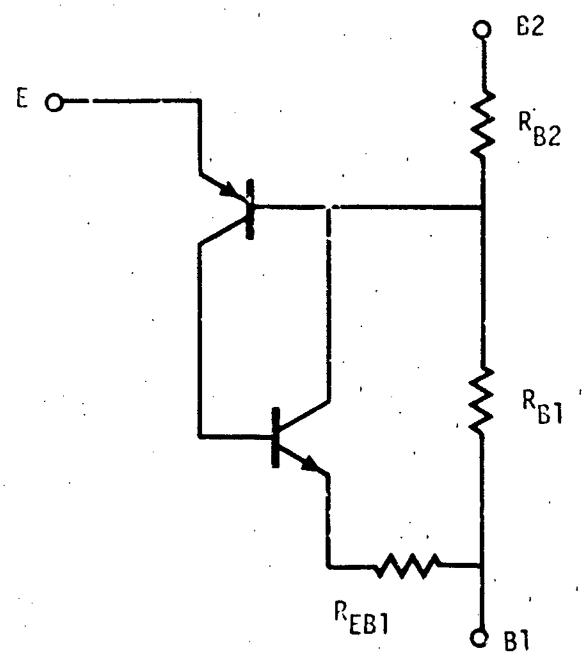


Figure V-15. UJT Equivalent Circuit

2. General Purpose UJT Model

a. Description

The UJT model presented is a practical, functional, all-purpose model of the unijunction transistor.

b. Advantages

The general purpose UJT model is sophisticated enough for almost any need, yet simple enough to allow easy parameterization and implementation.

c. Cautions

Implementation requires a computer code with a mathematical function capability.

d. <u>Characteristics</u>

The topology for the UJT model is given in figure V-16.

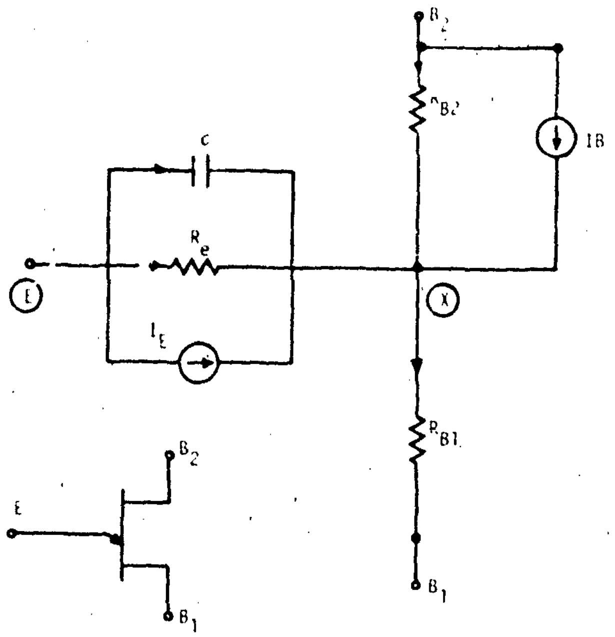


Figure V-16. UJT Model

The switching characteristics for the UJT are illustrated in figure V-17.

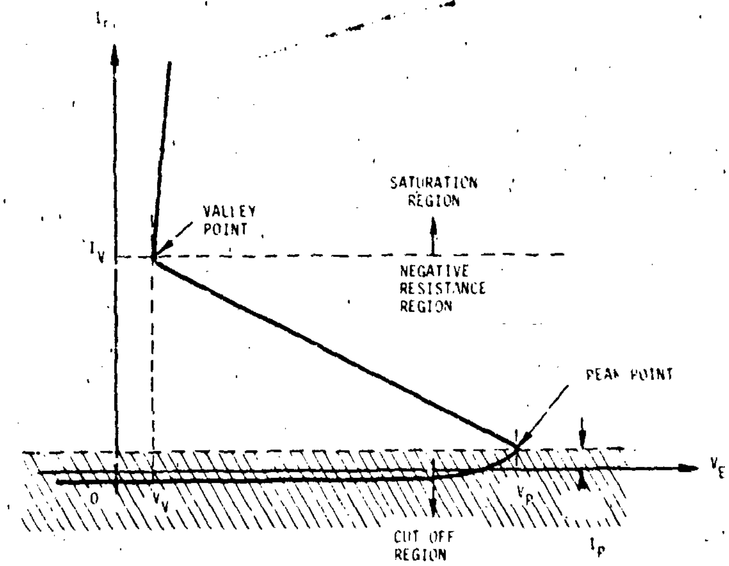


Figure V-17. UJT Characteristics

e. Defining Equations

$$I_B = \alpha I_E$$

$$I_E = I_S \left(e^{\theta V_{C1}} - 1\right)$$

$$R_{B1} = \frac{\left[\eta_{VK} - a(V_{BB} - V_K)\right]\left[R_{BBVK} + b(V_{BB} - V_K)\right]}{(I_E/I_{E1})}$$

$$R_{B2} = \left\{1 - \left[\eta_{VK} - a(V_{BB} - V_K)\right]\right\}\left[R_{BBVK} + b(V_{BB} - V_K)\right]$$

$$C_1 = K_D (I_E + I_S) + C_X$$

f. Parameter List

η_{VK} = the intrinsic standoff ratio measured at $V_{BB} = V_K$

V_{BB} = the voltage between base two and base one (B_2 and B_1)

V_K = the test value of V_{BB} at which R_{BBVK} and η_{VK} are specified

R_{B1} = the base one resistance

R_{B2} = the base two resistance

R_{BBVK} = R_{BB}, the interbase resistance measured at $V_{BB} = V_K$

C_1 = the sum of the emitter base one diode diffusion capacitance and C_X, a capacitor to keep C_1 from going to zero

α = a constant relating current generator I_B to I_E

I_E = a current source representing the emitter base one diode

I_B = a current source representing the modulation of the base two region by the emitter current

I_{E1} = a constant determined from measurements

C_X = a small arbitrary value of capacitance

I_S = the diode saturation current

a = an empirical constant

b = an empirical constant

θ = the constant of the emitter base one diode equation

K_D = the diffusion capacitance constant

g. <u>Parameterization</u>

1) <u>θ</u>

a) <u>Definition</u>

θ is the constant of the emitter base one diode

b) <u>Typical Value</u>

θ is ideally 38.61 at room temperature. Decreases in the ideal θ of over a factor of two are common.

c) <u>Measurement</u>

Two I-V points on the emitter base one diode characteristic are required for the determination of θ. A test setup for the measurement is shown in figure V-18.

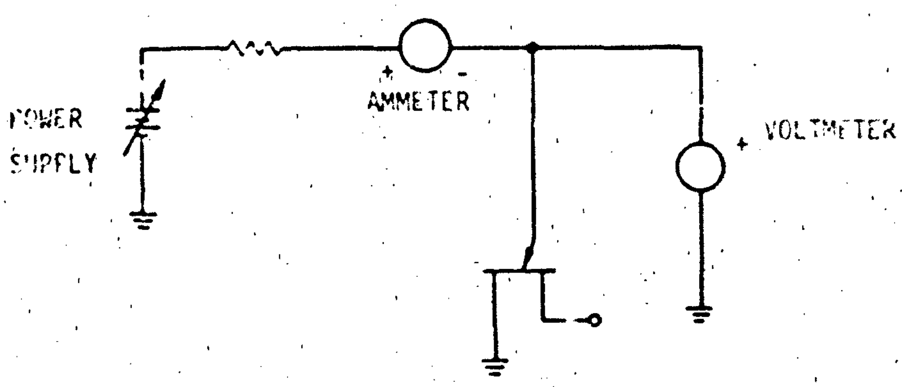


Figure V-18. UJT Diode Test Circuit

θ can be determined from (V_1, I_1), (V_2, I_2) as:

$$\theta = \frac{\ln\left(\frac{I_2}{I_1}\right)}{V_2 - V_1}$$

The currents used to perform the measurement should be kept under 1 μA due to the high value of bulk resistance.

d) <u>Example - 2N4894</u>

Two points measured on the emitter-base one characteristic were:

(0.3 μA, 0.345 V)

(1 μA, 0.390 V)

$$\theta = \frac{\ln\left(\frac{1\ \mu A}{0.3\ \mu A}\right)}{(0.390\ V - 0.345\ V)} = 26.8$$

2) <u>I_S</u>

a) <u>Definition</u>

I_S is the saturation current of the diode and is necessary to define the behavior of the diode.

b) <u>Typical Value</u>

I_S varies widely. A typical value is 1×10^{-14} A.

c) <u>Measurement</u>

The diode saturation current is determined by choosing a single I-V point from the forward bias region. Either point used to obtain θ may be used by substituting into:

$$I_S = \frac{I}{e^{\theta V} - 1}$$

d) Example - 2N4894

Choosing the bias point (0.3 μA, 0.345 V):

$$i_S = \frac{0.3\ \mu A}{\exp\ [(26.8)(0.345\ V)]\ -1}$$

$$I_S = 2.9 \times 10^{-11} \text{ amperes}$$

3) η_{VK}, a

a) Definition

η_{VK} is the intrinsic standoff ratio at $V_{BB} = V_K$. The constant which relates η to V_{BB} is "a".

b) Typical Values

A typical value for η_{VK} is 0.7. A typical value for a is 0.001/volt.

c) Measurement

Values of η at various values of V_{BB} are obtained using a test circuit such as the one shown in figure V-19. The "test" switch is then released and η is read directly from the meter where 1.0 = full scale. This procedure is repeated for each value of V_{BB}. The meter must be recalibrated for each new value. Diode D1 should be picked to have a characteristic similar to the emitter base one diode. The values of η versus V_{BB} are then plotted. V_K is arbitrarily chosen near the center of the V_{BB} range. η_{VK} is the value of η at V_K.

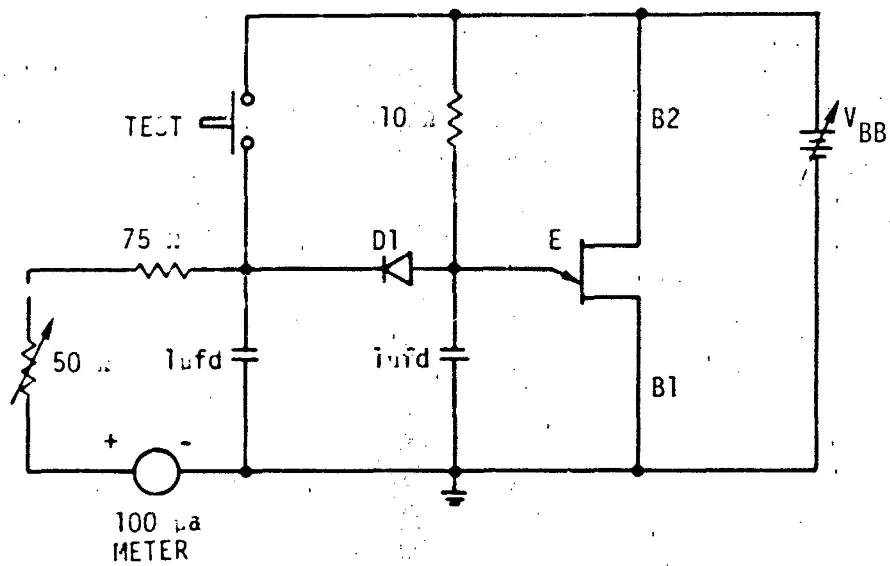


Figure V-19. η Test Circuit

The constant "a" is the negative of the slope on the η versus V_{BB} curve. A straight line approximation may be required. a is calculated from:

$$a = \frac{(\eta_2 - \eta_1)}{(V_2 - V_1)}$$

d) Example - 2N4894

1 From Measurement

The values of η as a function of V_{BB} are shown in table V-4. The data are plotted in figure V-20. One surprising result of this plot is the positive slope of the line formed. It is believed this may be due to the limitations of the test setup. Therefore, η will be considered a constant and "a" will be considered to be zero for this model. Choosing V_K as 10 V, η_{VK} is about 0.82.

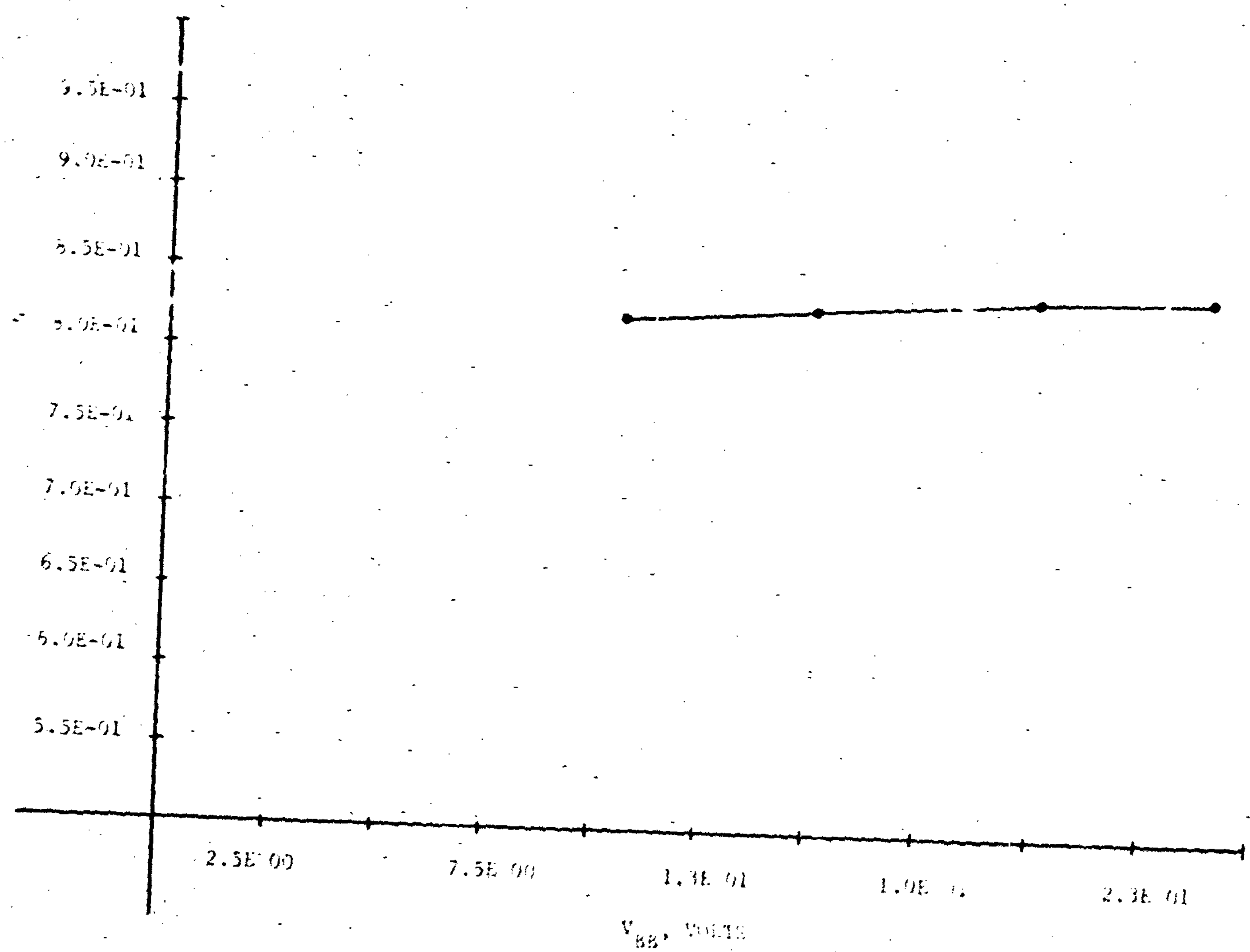


Figure V-20. Intrinsic Standoff Ratio as a Function of V_{BB}

TABLE V-4. η DETERMINATION

V_{BB}	η
5.0 V	0.820
10.5	0.822
15.0	0.830
20.0	0.838
23.9	0.840

2 From Data Sheets

The manufacturer specification sheets presented in figure V-21 list η at 10 V (V_K) between 0.74 and 0.86. A guess at η_{VK} from data sheets might be the midpoint which is 0.8.

4) R_{BBVK}, b

a) Definition

R_{BBVK} is the interbase resistance at $V_{BB} = V_K$. The constant which relates R_{BB} to V_{BB} is b.

b) Typical Value

Typical values for R_{BBVK} and b are 5 kilohms and 0.05 kilohms/volt, respectively.

c) Measurement

R_{BB} may be obtained at several values of V_{BB} from a test setup such as the one shown in figure V-22.

TYPES 2N4891 THRU 2N4894
P-N PLANAR UNIJUNCTION SILICON TRANSISTORS

TYPES 2N4891 THRU 2N4894
BULLETIN NO DL-S 6797[illegible], JANUARY 1967
REVISED MAY 1968

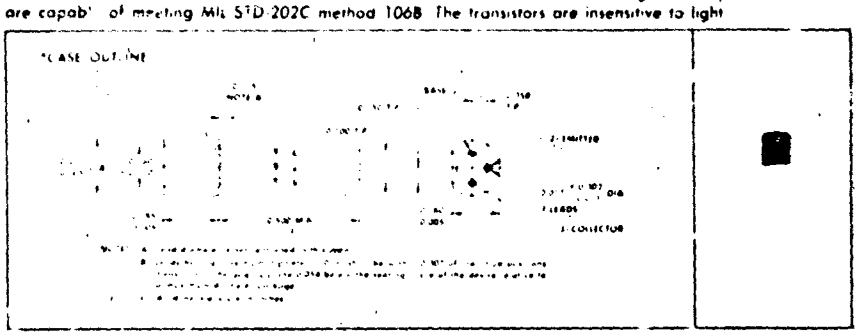
P'ANAR UNIJUNCTION SILECT' TRANSISTORS SPECIFICALLY CHARACTERIZED FOR A WIDE RANGE OF MILITARY, SPACE AND INDUSTRIAL APPLICATIONS:

2N4891 for General Purpose UJT Applications (Replaces TIS43)
2N4892 for High-Frequency Relaxation-Oscillator Circuits
2N4893 for Thyristor (SCR) Trigger Circuits
2N4894 for Long-Time-Delay Circuits

- **Planar Process Provides Extremely Low Leakage, High Performance at Low Driving Currents, and Greatly Improved Reliability**
- **Rugged, One-Piece Construction Features Standard 100-mil TO-18 Pin-Circle**

mechanical data

These transistors are encapsulated in a plastic compound specifically designed for this purpose, using a highly mechanized process developed by Texas Instruments. The case will withstand soldering temperatures without deformation. These devices exhibit stable characteristics under high humidity conditions and are capable of meeting MIL STD 202C method 106B. The transistors are insensitive to light.



*absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Emitter Base-Two Reverse Voltage	−30 V
Interbase Voltage	See Note 1
Continuous Emitter Current	50 mA
Peak Emitter Current (See Note 2)	1 A
Continuous Device Dissipation at (or below) 25°C Free Air Temperature (See Note 3)	360 mW
Storage Temperature Range	−65°C to 150°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	260°C

NOTES: 1. Interbase voltage is limited solely by power dissipation [illegible]
2. This value applies for [illegible] discharge through the emitter–base-one diode. Current must fall to 0.37 A within 3 ms and pulse repetition rate must not exceed 10 pps.
3. Derate linearly to 150°C free-air temperature at the rate of 2.88 mW/deg.

*Indicates JEDEC registered data
†Trademark of Texas Instruments
‡Patent Pending

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

7391

Figure V-21. 2N4891-2N4894 Manufacturer Specification Sheets (ref. V-2)

TYPICAL CHARACTERISTICS

STATIC INTERBASE RESISTANCE
vs
FREE-AIR TEMPERATURE

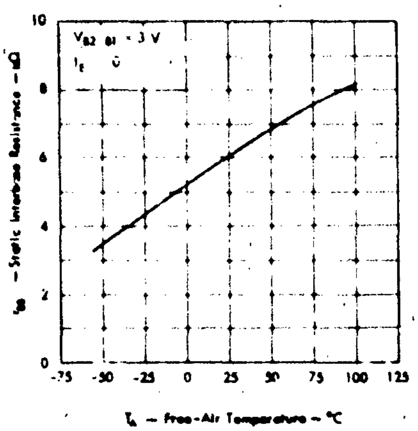


FIGURE 4

EMITTER REVERSE CURRENT
vs
FREE-AIR TEMPERATURE

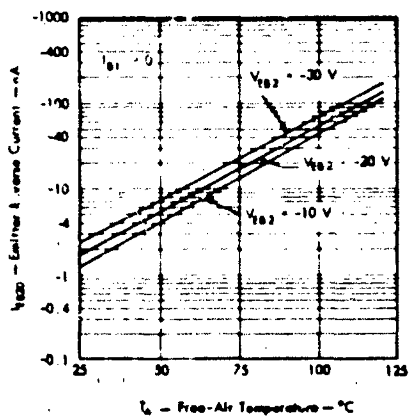


FIGURE 5

2N4893
BASE-ONE PEAK PULSE VOLTAGE
vs
FREE-AIR TEMPERATURE

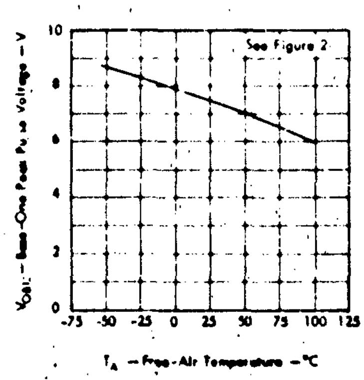


FIGURE 6

Figure V-21. 2N4891-2N4894 Manufacturer Specification Sheets (Continued)

TYPES 2N4891 THRU 2N4894
P-N PLANAR UNIJUNCTION SILICON TRANSISTORS

TYPICAL CHARACTERISTICS

MODULATED INTERBASE CURRENT
vs
INTERBASE VOLTAGE

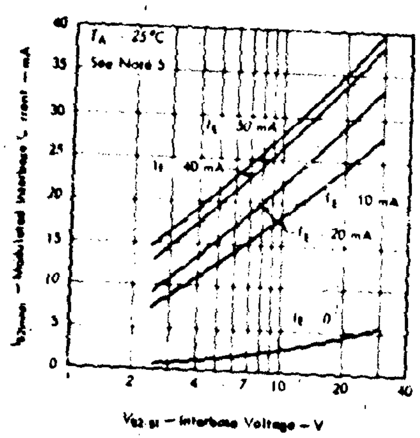


FIGURE 7

MODULATED INTERBASE CURRENT
vs
FREE-AIR TEMPERATURE

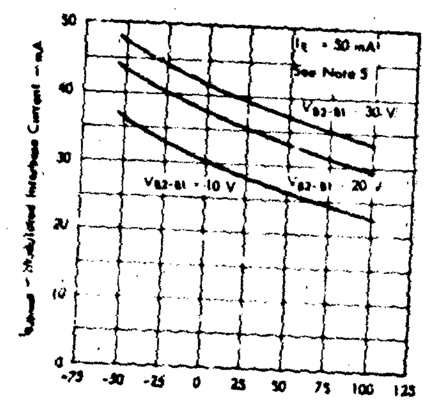


FIGURE 8

2N4894
PEAK-POINT EMITTER CURRENT
vs
FREE-AIR TEMPERATURE

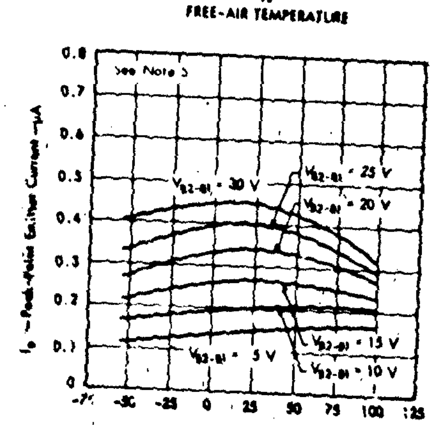


FIGURE 9

NOTE 5: This parameter is measured using pulse techniques. t_p = 300 μs, duty cycle ≤ 2%.

Figure V-21. 2N4891-2N4894 Manufacturer Specification Sheets (Continued)

TYPES 2N4891 THRU 2N4894
P-N PLANAR UNIJUNCTION SILICON TRANSISTORS

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		2N4891 MIN	2N4891 MAX	2N4892 MIN	2N4892 MAX	2N4893 MIN	2N4893 MAX	2N4894 MIN	2N4894 MAX	UNIT
r_{BB}	Static Interbase Resistance	V_{B2B1} = 3 V, I_E = 0		4	9.1	4	9.1	4	12	4	12	kΩ
$\alpha_{r_{BB}}$	Interbase Resistance Temperature Coefficient	V_{B2B1} = 3 V, I_E = 0, T_A = −55°C to 100°C	See Note 4	0.1	0.9	0.1	0.9	0.1	0.9	0.1	0.9	%/deg
η	Intrinsic Standoff Ratio	V_{B2B1} = 10 V,	See Figure 1	0.55	0.82	0.51	0.69	0.55	0.82	0.74	0.86	
$I_{B2(mod)}$	Modulated Interbase Current	V_{B2B1} = 10 V, I_E = 50 mA,	See Note 5	10		10		10		10		mA
I_{EB2O}	Emitter Reverse Current	V_{EB2} = −30 V, I_{B1} = 0			−10		−10		−10		−10	nA
I_P	Peak-Point Emitter Current	V_{B2B1} = 25 V			5		2		2		1	μA
$V_{EB1(sat)}$	Emitter – Base-One Saturation Voltage	V_{B2B1} = 10 V, I_E = 50 mA,	See Note 5		4		4		4		4	V
I_V	Valley Point Emitter Current	V_{B2B1} = 20 V		2		1		2		2		mA
V_{OB1}	Base-One Peak Pulse Voltage	See Figure 2		3		3		6		3		V

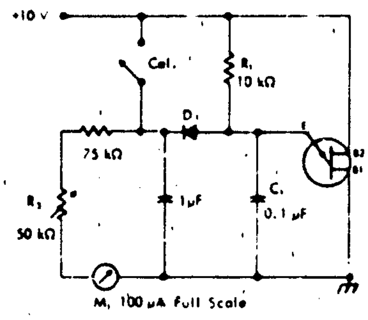
NOTES 4. Temperature coefficient, $\alpha_{r_{BB}}$, is determined by the following formula: $\alpha_{r_{BB}} = \left[\frac{(r_{BB} @ 100°C) - (r_{BB} @ -55°C)}{(r_{BB} @ 25°C)}\right] \frac{100\%}{155\ \deg}$

To obtain r_{BB} for a given temperature $T_{A(2)}$, use the following formula: $r_{BB(2)} = [r_{BB} @ 25°C] [1 + (\alpha_{r_{BB}}/100)(T_{A(2)} - 25°C)]$

5. These parameters must be measured using pulse techniques. t_p = 300 μs, duty cycle ≤ 2%.

*Indicates JEDEC registered data.

PARAMETER MEASUREMENT INFORMATION



η — Intrinsic Standoff Ratio — This parameter is defined in terms of the peak-point voltage, V_p, by means of the equation: $V_p = \eta V_{B2B1} + V_F$, where V_F is about 0.56 volt at 25°C and decreases with temperature at about 3 millivolts/deg.

The circuit used to measure η is shown in the figure. In this circuit, R_1, C_1 and the unijunction transistor form a relaxation oscillator, and the remainder of the circuit serves as a peak-voltage detector with the diode D_1 automatically subtracting the voltage V_F. To use the circuit, the "cal" button is pushed, and R_1 is adjusted to make the current meter M_1 read full scale. The "cal" button then is released and the value of η is read directly from the meter, with η = 1 corresponding to full-scale deflection of 100 μA.

D_1: 1N457, or equivalent, with the following characteristics:
V_F = 0.565 V at I_F = 50 μA,
$I_R \leq 2$ μA at V_R = 30 V

FIGURE 1 – TEST CIRCUIT FOR INTRINSIC STANDOFF RATIO (η)

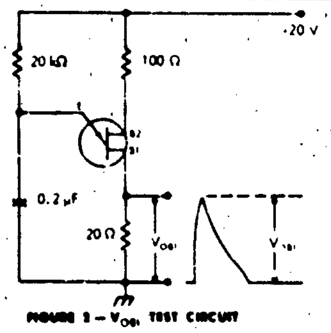


FIGURE 2 – V_{OB1} TEST CIRCUIT

EMITTER—BASE-ONE VOLTAGE
vs
EMITTER CURRENT

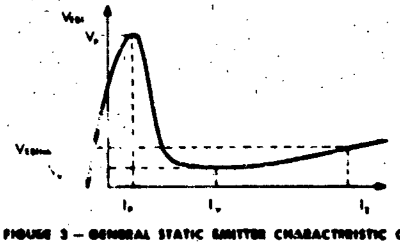


FIGURE 3 – GENERAL STATIC EMITTER CHARACTERISTIC CURVE

Figure V-21. 2N4891-2N4894 Manufacturer Specification Sheets (Continued)

TYPES 2N4891 THRU 2N4894
P-N PLANAR UNIJUNCTION SILICON TRANSISTORS

TYPICAL CHARACTERISTICS

EMITTER–BASE-ONE VOLTAGE
vs
EMITTER CURRENT

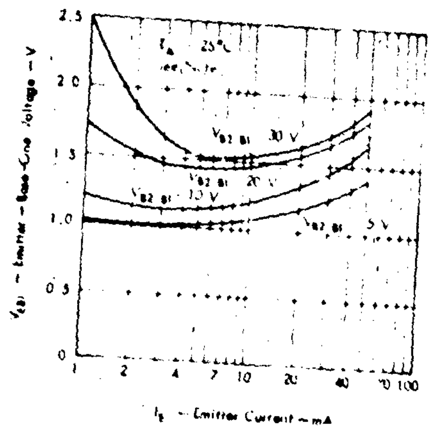


FIGURE 10

EMITTER–BASE-ONE SATURATION VOLTAGE
vs
FREE-AIR TEMPERATURE

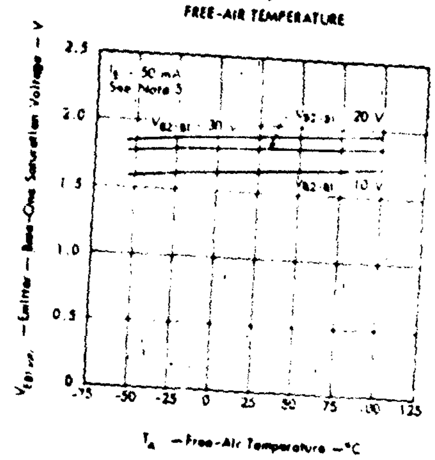


FIGURE 11

2N4892
VALLEY-POINT EMITTER CURRENT
vs
FREE-AIR TEMPERATURE

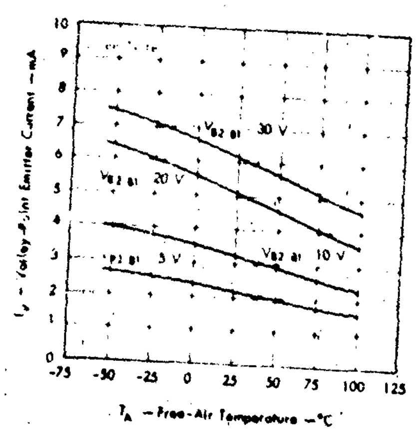


FIGURE 12

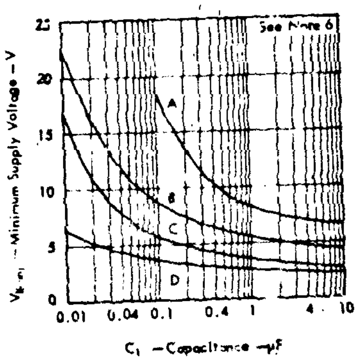
NOTE 5: This parameter is measured using pulse techniques. t_p = 300 μs, duty cycle ≤ 2%.

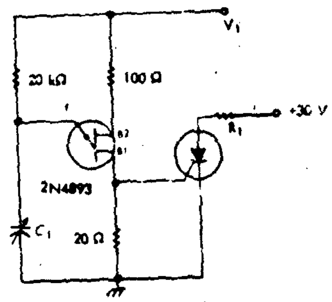
Figure V-21. 2N4891-2N4894 Manufacturer Specification Sheets (Continued)

TYPES 2N4891 THRU 2N4894
P-N PLANAR UNIJUNCTION SILICON TRANSISTORS

TYPICAL CHARACTERISTICS

TYPICAL MINIMUM SUPPLY VOLTAGE TO TRIGGER THYRISTOR
vs
CAPACITANCE





TEST CIRCUIT

INDEX OF THYRISTOR TYPES

CURVE	THYRISTOR TYPES	R_1
A	TI3037-42, 2N3936-40	35 Ω
B	2N681-88, 2N681A-89A, 2N1842B-50B	70 Ω
C	TI145A0 A4, 2N1595-99, TI40A0-A5, 2N1600-04, 2N1770 77, 2N2653, TI3010, TIC28-31	70 Ω
D	2N3001-08, 2N876-81, 2N884-88, 2N2687-90, 2N3555-62, TIC44-47	70 Ω

FIGURE 13 — OPERATING INFORMATION (2N4893)

NOTE 6 This chart shows typical observed values of minimum base-two supply voltage required to trigger individual thyristors of the types indicated.

Figure V-21. 2N4891-2N4894 Manufacturer Specification Sheets (Concluded)

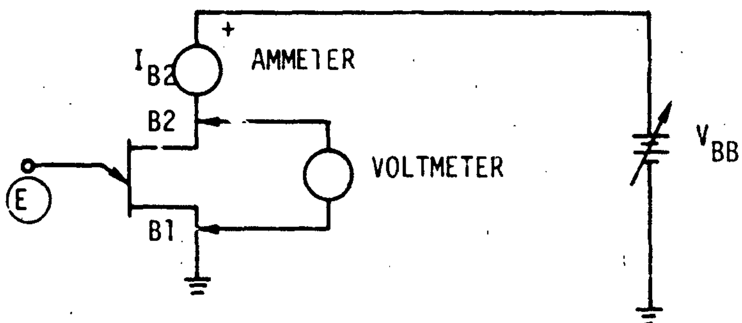


Figure V-22. R_{BB} Test Circuit

The base two current is recorded for each value of V_{BB} applied. R_{BB} at each value of V_{BB} is calculated as:

$$R_{BB} = \frac{V_{BB}}{I_{B2}}$$

R_{BB} is plotted as a function of V_{BB}. R_{BBVK} is the value of R_{BB} at V_K. "b" is the slope of the R_{BB} versus V_{BB} curve. A straight line approximation should be made. Choosing two points on the straight line approximation yields:

$$b = \frac{R_{BB2} - R_{BB1}}{V_{BB2} - V_{BB1}}$$

d) <u>Example - 2N4894</u>

<u>1</u> <u>From Measurement</u>

Data obtained from interbase resistance measurements are listed in table V-5. The data are plotted in figure V-23. R_{BBVK} is 6.58 kilohms and b is about:

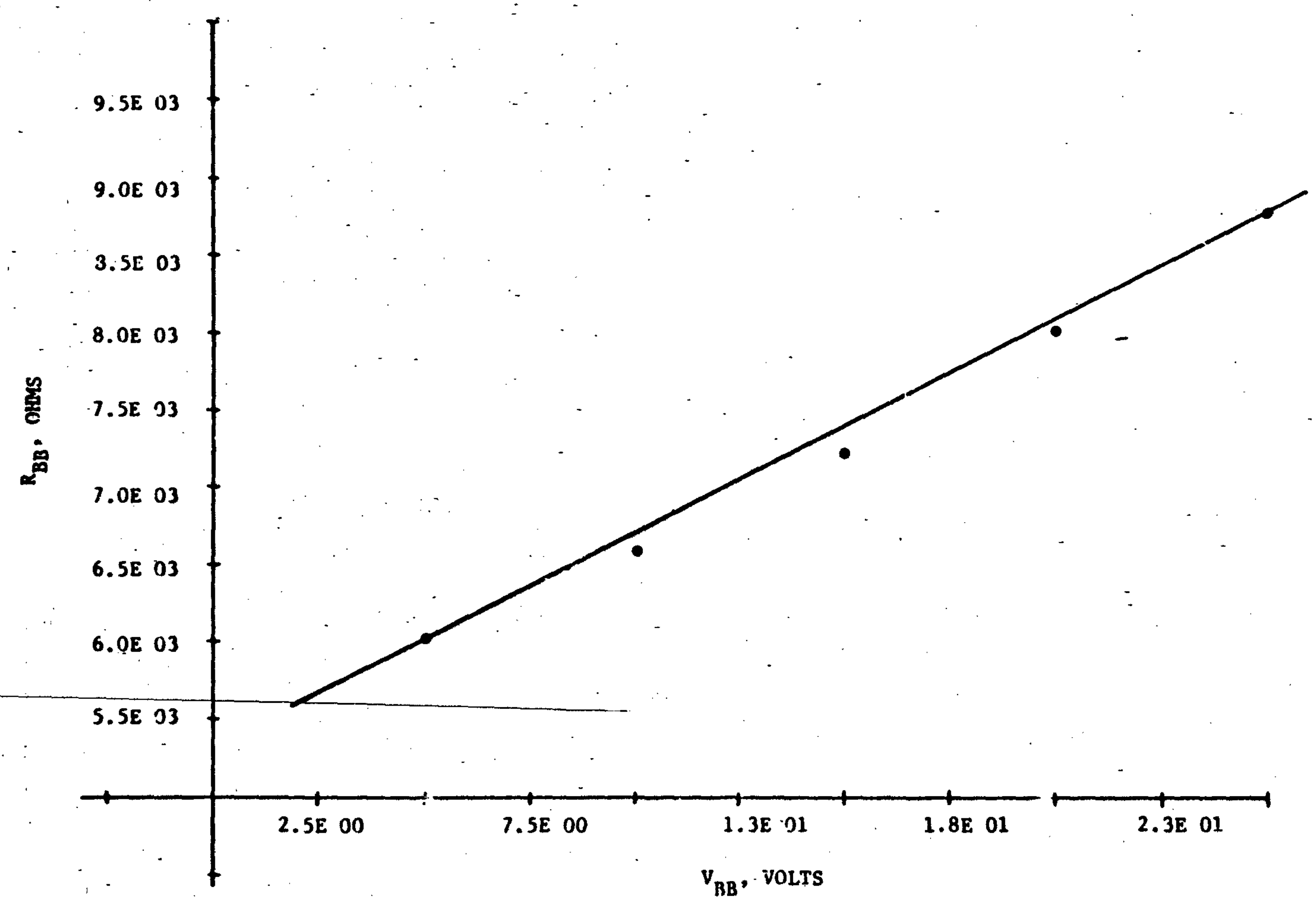


Figure V-23. Interbase Resistance as a Function of V_{BB}

$$b = \frac{(8.77 \times 10^3 \text{ ohms} - 6.02 \times 10^3 \text{ ohms})}{(25 \text{ V} - 5 \text{ V})}$$

$b = 138$ ohms/volt

TABLE V-5. R_{BB} MEASUREMENTS

V_{BB}	I_{BB}	R_{BB}
5 V	0.83 mA	$6.02 \times 10^3\ \Omega$
10	1.52	6.58×10^3
15	2.08	7.21×10^3
20	2.50	8.00×10^3
25	2.85	8.77×10^3

2 From Data Sheets

R_{BB} and b may be obtained from the plot of modulated interbase current as a function of V_{B2-B1} in figure V-21. The $I_E = 0$ curve is required. Taking points off of this curve yields the values listed in table V-6. The data show an R_{BBVK} of about 5 kilohms and a b of nearly zero.

TABLE V-6. R_{BB} FROM DATA SHEETS

V_{BB}	I_{BB}	R_{BB}
5 V	1.0 mA	$5 \times 10^3\ \Omega$
10	2.5	4×10^3
15	3.0	5×10^3
20	4.0	5×10^3
25	5.0	5×10^3

5) N

a) Definition

N is the exponent of the equation relating R_{B1} to I_E

b) Typical Value

A typical value of N is 0.5.

c) Measurement

N may be obtained from the I-V characteristic of the emitter base one diode in the saturation region (high emitter current). I_E and V_{EB1} are obtained at two points in the saturation region using a test setup such as the one shown in figure V-24.

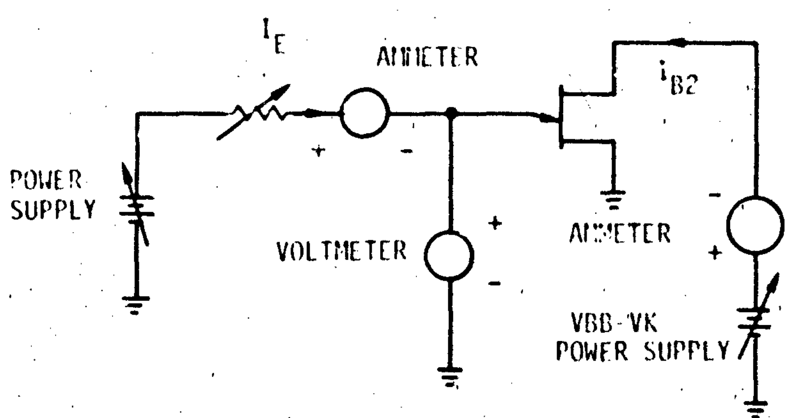


Figure V-24. Saturation Region Test Circuit

The value of V_{BB} applied is chosen to be equal to V_K. R_{B1} is:

$$R_{B1} = \frac{V_{EB1} - V_{jE}}{I_E + I_{B2}}$$

where:

$$V_{jE} = \frac{1}{\theta} \ln\left(\frac{I_E}{I_S}\right)$$

N can now be determined as:

$$N = \frac{\ln\left(\frac{R_{B1A}}{R_{B1B}}\right)}{\ln\left(\frac{I_{EB}}{I_{EA}}\right)}$$

where:

$R_{B1A} = R_{B1}$ at I_E = value 1
$R_{B1B} = R_{B1}$ at I_E = value 2
$I_{EA} = I_E$ at value 1
$I_{EB} = I_E$ at value 2

d) Example - 2N4894

The two bias points produced the following data:

Bias Point One

I_{EB1} = 3 mA
V_{EB1} = 1.85 V
V_{BB} = 10 V
I_{B2} = 8 mA

$$V_{jE} = \frac{1}{26.8} \ln\left(\frac{3 \text{ mA}}{2.9 \times 10^{-11} \text{ A}}\right) = 0.689 \text{ V}$$

$$R_{B1} = \frac{1.85 \text{ V} - 0.689 \text{ V}}{3 \text{ mA} + 8 \text{ mA}} = 106\ \Omega$$

Bias Point Two

$I_{EB1} = 5$ mA

$V_{EB1} = 1.75$ V

$V_{BB} = 10$ V

$I_{E2} = 9.8$ mA

$$V_{jE} = \frac{1}{26.8} \ln\left(\frac{5 \text{ mA}}{2.9 \times 10^{-11} \text{ A}}\right) = 0.708 \text{ V}$$

N can now be computed as:

$$N = \frac{\ln\left(\frac{106\ \Omega}{70.4\ \Omega}\right)}{\ln\left(\frac{5 \text{ mA}}{3 \text{ mA}}\right)} = 0.8$$

6) I_{E1}

a) Definition

I_{E1} is an empirically determined constant.

b) Typical Value

A typical value for $I_{E1} = 1$ mA.

c) Measurement

I_{E1} is determined from:

$$I_{E1} = \frac{I_E}{\left(\eta_{VK}\ R_{BBVK}/R_{B1}\right)^{1/N}}$$

d) Example - 2N4894

Choosing the previous result of $R_{B1} = 106\ \Omega$ at $I_E = 3$ mA, I_{E1} can be found as:

$$I_{E1} = \frac{3\ \text{mA}}{\left[(0.82)(6.58 \times 10^3\ \Omega)/(106\ \Omega)\right]^{1/0.8}}$$

$$I_{E1} = 2.21 \times 10^{-5} \text{ amperes}$$

7) $\underline{\alpha}$

a) <u>Definition</u>

α is the value of the constant relating the current generator I_B to I_E.

b) <u>Typical Value</u>

A typical value for α is 0.1.

c) <u>Measurement</u>

The value for α is determined from I_E, I_{B2}, R_{B1}, and R_{B2} at a bias point in the saturation region. α can be found as follows:

$$\alpha = \frac{1}{I_E}\left[I_{B2} - \frac{V_{BB} - (I_E + I_{B2})\ R_{B1}}{R_{B2}}\right]$$

At $V_{BB} = V_K$,

$$R_{B2} = (1 - \eta_{VK})\ R_{BBVK}$$

d) <u>Example - 2N4894</u>

Using the parameters obtained at "Bias Point One," α can be calculated as:

$$\alpha = \frac{1}{3\ \text{mA}}\left[8\ \text{mA} - \frac{10\ \text{V} - (3\ \text{mA} + 8\ \text{mA})\ 106\ \Omega}{(1 - 0.82)(6.58 \times 10^3\ \Omega)}\right]$$

$$\alpha = 0.18$$

8) K_D

a) <u>Definition</u>

K_D is the constant of the diffusion capacitance equation.

b) <u>Typical Value</u>

A typical value of K_D is 1×10^3 pF/mA.

c) <u>Measurement</u>

K_D is determined from storage time measurements for the emitter base one diode. Base two is left open. A discussion of the details of this measurement can be found in chapter II.

d) <u>Example - 2N4894</u>

Measurement of the diffusion capacitance constant was obtained from the photograph shown in figure V-25 which shows the switching transient of the diode. The oscilloscope voltage is obtained by monitoring the diode current through a 1K resistor. From the photograph:

t_s = 500 ns
I_F = 4 mA
I_R = 1 mA

$$F = \frac{1}{2\pi} \; \frac{\ln\,(1 + 4\text{ mA}/1\text{ mA})}{500\text{ ns}}$$

$$F = 5.12 \times 10^5 \text{ Hz}$$

$$K_D = \frac{26.8}{2\pi\,(5.12 \times 10^5 \text{ Hz})}$$

$$K_D = 8.33 \times 10^{-6} \text{ farads/amp}$$

9) R_C

a) <u>Definition</u>

R_C is the emitter base one diode leakage resistance.

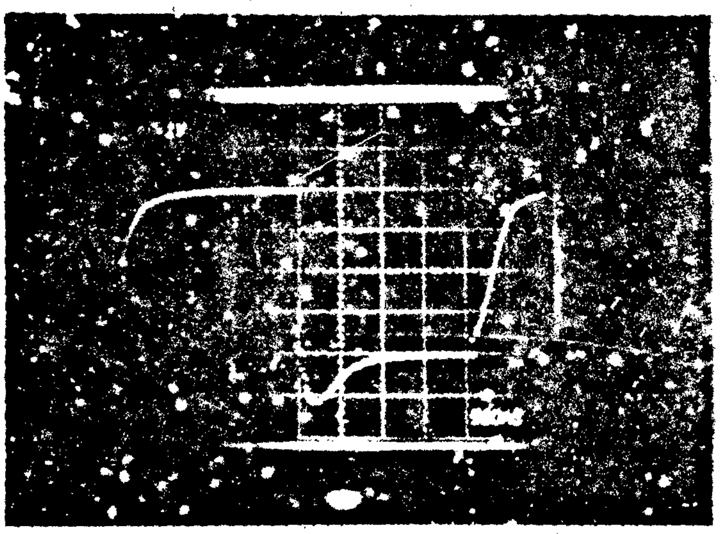


Figure V-25. Switching Transient of Emitter-Base One Diode

b) Typical Value

A typical value for R_C is 10 kilohms.

c) Measurement

R_C may be obtained by applying a reverse bias to the emitter base one diode with the base two lead open and measuring the current.

$$R_C = \frac{V_R}{I_R}$$

d) Example - 2N4894

The reverse leakage current of the emitter base one diode was found to be 0.68 nA at a reverse bias of 25 volts.

$$R_C = \frac{25\ \text{V}}{0.68\ \text{nA}} = 3.68 \times 10^{10}\ \text{ohms}$$

3. Radiation Effects

a. Photocurrent Effects

The characteristics of the unijunction transistor are critically dependent on the interbase resistance terms. Ionizing radiation will increase the number of charge carriers in the base region increasing the conductivity of this high resistance material. The decrease in interbase resistivity may result in sudden switching. This effect can be modeled by varying the interbase resistivity terms based on measurements.

b. Neutron Effects

Again, the characteristics of the UJT are linked to the behavior of the interbase resistance. Neutron irradiation will increase the resistivity of these regions. High resistivity semiconductor material is especially susceptible to this effect.

The reduction in minority carrier lifetime will affect the conductivity modulation process. The injected holes, which lower the

resistivity of the interbase element will disappear faster. An increase in emitter current will be required to produce an equivalent change in the resistivity of the interbase element.

The circuit operation of the UJT depends on the valley voltage and firing voltage. Neutron irradiation will leave the firing voltage unaffected, but will increase the valley voltage. Failure occurs when the valley voltage is about equal to the firing voltage. When this voltage equality occurs, the usefulness of the device is lost. The valley voltage has been seen to be a direct function of fluence level through experiments. Failure usually occurs at a fluence level between 10^{12} n/cm^2 and 10^{13} n/cm^2.

4. Computer Example

The 2N4894 model was verified by placing the UJT model within a relaxation oscillator circuit. The test circuit used to test the UJT oscillator is shown in figure V-26.

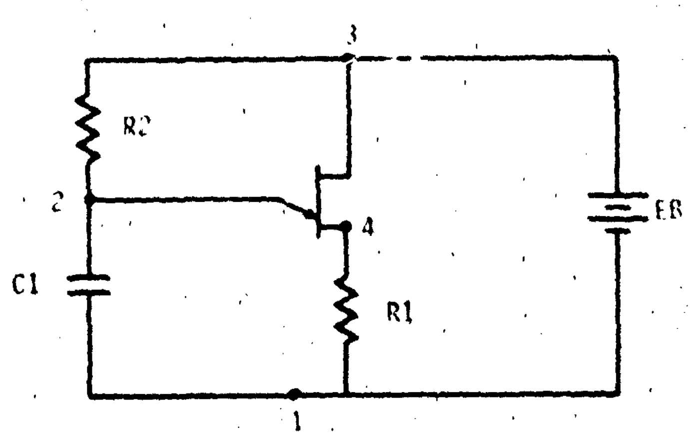


Figure V-26. UJT Test Circuit Schematic

Figure V-27 represents the input to SCEPTRE. The response of the simulated oscillator is shown in figure V-28. A verifying feature of this run is the voltage at which the UJT triggers. EB in the test circuit was set to 10 volts. The UJT should trigger at roughly the intrinsic

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S C E P T R E   NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2      5/76
 12/14/77     10.52.57.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD  "DOCUMENT"  AS THE FIRST CARD
OF THE INPUT TEXT


COMPUTER TIME ENTERING SETUP PHASE-
          CPA        .386 SEC.
          PP        0.000 SEC.
          IO        0.000 SEC.


MODEL DESCRIPTION
MODEL 2N4894 (B1-E-B2)
ELEMENTS
JB,B2-X=0.484*JE
JE,E-X=DIODE Q(2.9E-11,25.8)
J2,B2-B1=0
CE,E-X=Q1(2.E-9,4.33E-6,JE,2.9E-11)
RB1,X-B1=Q2(,B2,3,VJ2,10.,6.58E3,1.38,
1.,JE,PIE1,0.,8)
RB2,B2-X=Q3(1.,.32,0.,VJ2,10.,6.58E3,1.39)
RC,F-X=3.64E10
DEFINED PARAMETERS
PIE1=2.21E-5
FUNCTIONS
Q1(A,B,C,D)=(A+B*(C+D))
Q2(A,B,C,D,E,F,G,O,P,Q)=
(((A-B*(C-D))*(E+F*(C-D)))/((G+(O/P))**Q))
Q3(A,B,C,D,E,F,G)=((A-B*C*(D-E))*(F+G*(D-E)))
CIRCUIT DESCRIPTION
ELEMENTS
C1,2-1=0.0566E-6
R1,4-1=20.
R2,3-2=10.E3
T1,4-2-3=MODEL 2N4894
EA,1-3=10
OUTPUTS
VC1,VR1,JET1,PLOT
JET1,PLOT(VC1)
RUN CONTROLS
STOP TIME=5.E-3
END


THE TERM  VRRIT1  WILL CAUSE A COMPUTATIONAL DELAY.
```

Figure V-27. UJT Test Circuit

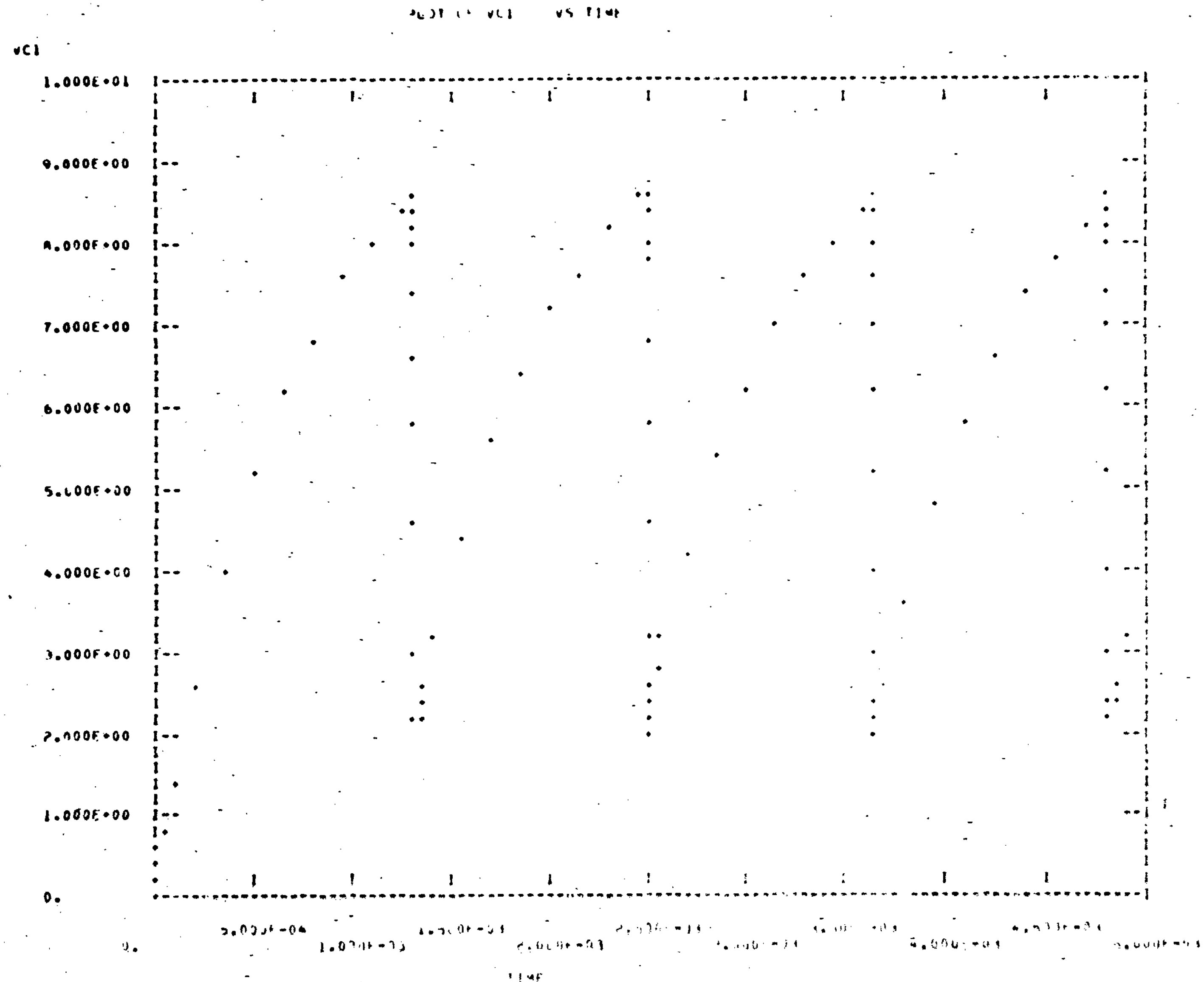


Figure V-28. UJT Oscillator

standoff ratio times EB. Since the intrinsic standoff ratio for the 2N4894 was determined experimentally as 0.82, the UJT should switch at 8.2 volts. The model 2N4894 can be observed to switch at 8.6 volts. The frequency of oscillations are determined by the external circuitry and cannot be used as a verifying test.

C. SCR MODELING

1. Introduction

The silicon controlled rectifier is a four layer (P-N-P-N) switch. The standard model of the SCR is the two transistor model illustrated in figure V-29.

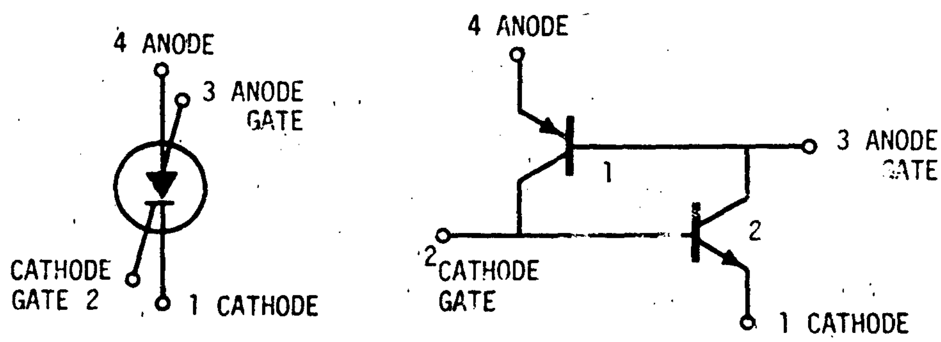


Figure V-29. Two Transistor Equivalent Model of the Thyristor

The anode gate is generally not accessible to terminal measurements, greatly complicating the modeling task. Simplifications, therefore, may be required.

Switching action occurs when the sum of the alphas (or the product of the betas) of the transistors exceeds unity. The alphas of each transistor are functions of anode current. At some value of anode current the sum of the two alphas will be unity and the SCR will switch from the blocking state to the on or conducting state. The switching is the result of regenerative feedback between the two transistors. Figure V-30 illustrates the characteristics of an SCR.

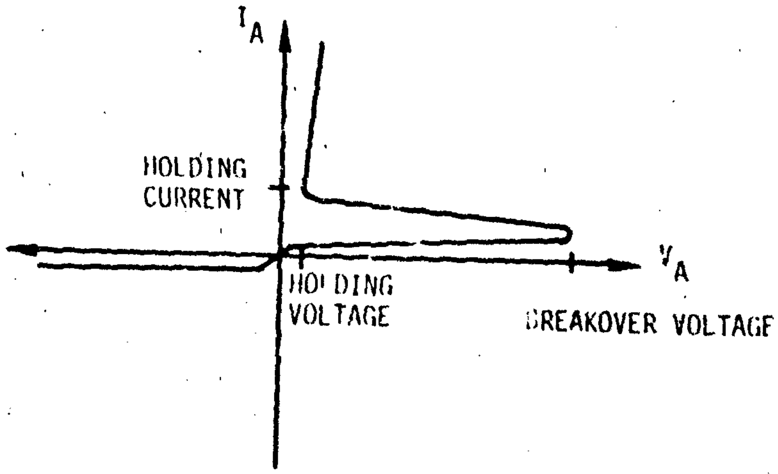


Figure V-30. SCR Characteristics

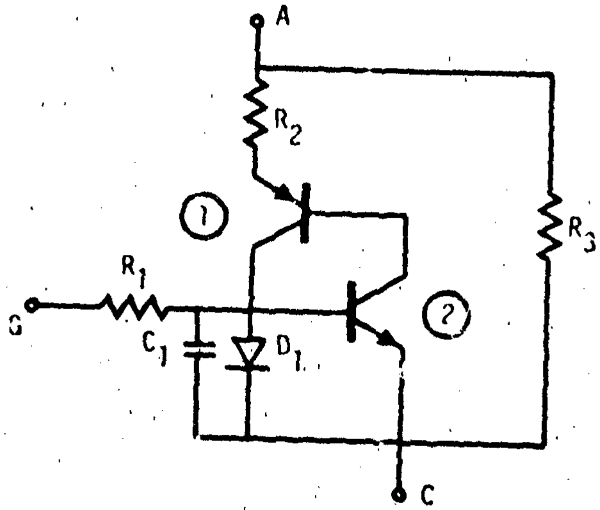


Figure V-31. SCR Model

As with the UJT, two modeling approaches exist, the equivalent circuit and a hybrid circuit-analytical function circuit. A third approach, which will not be discussed, treats the SCR as a logic element in one of two possible states.

To model the variable alpha in the equivalent circuit, a shunt diode is included as illustrated by figure V-31. R_1 represents the gate resistance and R_1C_1 determines turn-on delay time. R_3 is the anode to cathode leakage resistance. R_2 is the series resistance of the conducting state.

The constants of the shunt diode can be found by realizing that the diode behaves in an identical manner to the shunt diode discussed in chapter III.B.4 which models low current beta falloff.

An equivalent circuit model was developed in chapter VII.B.1 as an example. The gain of transistor 1 was chosen as unity. The gain of transistor 2 was chosen as 100. The parameters of the shunt diode were chosen such that at the anode trigger current of 2 microamperes, the low current gain of transistor 2 was also unity. Thus, at an anode current of 2 microamperes, the sum of the 2 alphas reaches unity and switching will occur.

The equivalent circuit of the SCR has the chief limitation of being unable to accurately model breakover. Breakover occurs due to leakage, avalanche multiplication, and base width modulation effects that occur when the reverse biased P-N junction of the SCR is subjected to further reverse bias. Breakover is illustrated in figure V-32. If higher simulation accuracy is desired, the describing equations for the SCR may be implemented through the hybrid approach. Such a model is discussed in more detail in the following section.

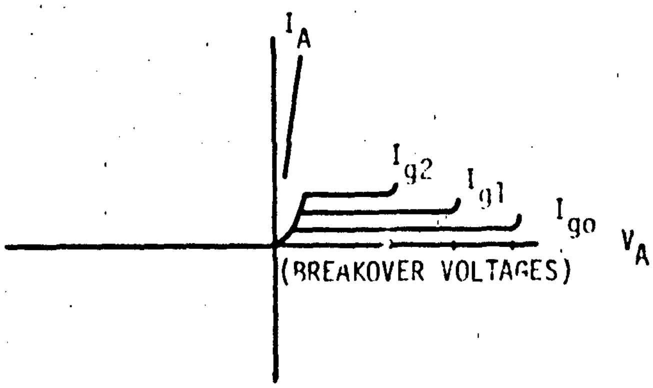


Figure V-32. Illustration of Breakover

2. SCR Model (Hybrid Approach)

   a. Description

The SCR model presented is a general purpose model developed from the equations which describe thyristor behavior up to turn-on.

   b. Advantages

The SCR model defines anode current as a function of gate current in the "off" region. The breakover voltage is simulated as a function of gate current in the "off" region.

   c. Cautions

The general SCR model only simulates device behavior to the extent of turn on. Many simplifications are made in the parameterization process. Implementation is difficult relative to the simpler models.

   d. Characteristics

The general SCR model is illustrated in figure V-33.

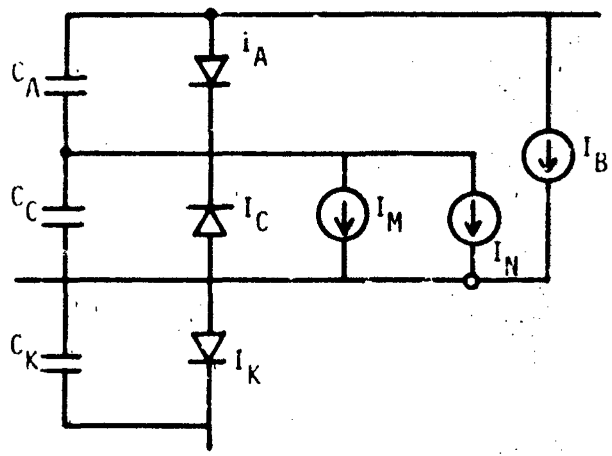


Figure V-33. SCR Model

The equation describing the off characteristic of a thyristor is:

$$I_A = \frac{\alpha_2 I_g}{1 - (\alpha_1 + \alpha_2)}$$

$$\alpha_1 = f(I_A)$$

$$\alpha_2 = f(I_A)$$

I_B is a voltage dependent current source whose function is to model the breakover condition illustrated in figure V-32. I_B would be more accurately placed in parallel with element I_C since I_B represents the leakage across junction I_C. I_B was placed at its present position to allow ease of parameterization.

e. Defining Equations

$$I_A = I_{SA} [\exp(\theta_A \cdot V_A) - 1]$$

$I_C = I_{SC} [\exp(\theta_C \cdot V_C) - 1]$

$I_K = I_{SK} [\exp(\theta_K \cdot V_K) - 1]$

$I_M = \alpha_2 (I_A) I_K = f(\phi)$

$I_N = \alpha_1 (I_A) I_A = f(\phi)$

I_B = the current necessary to increase the gate current to the trigger current when a breakdown condition is reached

C_A = application dependent capacitance

C_C = application dependent capacitance

C_K = application dependent capacitance

f. Parameterization

1) Determination of $\alpha_1 (I_A)$, $\alpha_2 (I_A)$

The characteristic of a 2N5061 SCR was obtained through application of the test circuit of figure V-34.

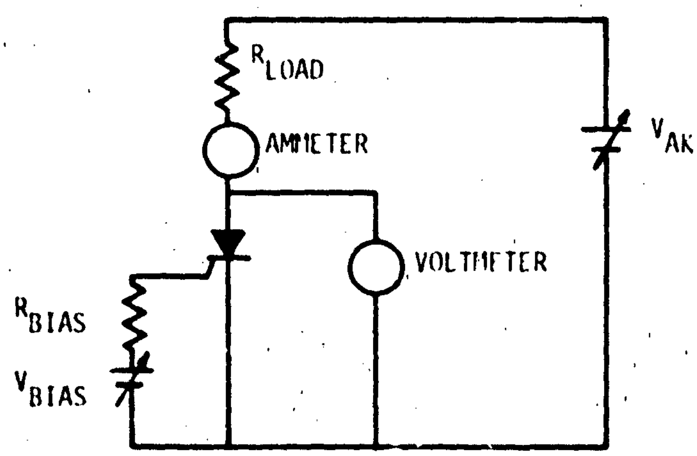


Figure V-34. Test Set for SCR

From the test circuit a set of anode currents at various values of gate currents for low anode voltages was obtained. The anode voltage was then increased to record breakover voltage. The results are listed in table V-7.

Alpha 1 was then chosen as 0.5. Solution of the equation describing the off characteristic of a thyristor for α_2 yields the values shown in table V-8. A plot of I_A and I_G as a function of α_2 is given in figure V-35. The value of gate current at which α_2 equals 0.5 was chosen as 30 microamperes.

Subsequent computer simulations established the exact gate trigger current as 0.97 μA. The experimental value of trigger current was about 1 μA. The current generator I_B was then described in a tabular fashion to supply current to the gate such that $I_G + I_B = 0.97$ μA at the breakover voltage.

2) Estimation of Other Parameters

From the accessible gate-cathode junction, two I-V points were measured as:

V_{GK}	I_{GK}
0.34 V	0.1 μA
0.50 V	1.0 μA

$$\theta = \frac{\ln\left(\frac{1\ \mu A}{0.1\ \mu A}\right)}{0.5\ V - 0.34\ V} = \frac{14.4}{V}$$

$$I_S = \frac{1\ \mu A}{\exp\left[\left(\frac{14.4}{V}\right)\left(0.5\ V\right)\right] - 1}$$

$$= 7.47 \times 10^{-10} \text{ amperes}$$

For simplicity, it was assumed:

TABLE V-7. MEASURED SCR PARAMETERS

I_A	I_G	V_{BO}
2 μA	0.41 μA	45.0 V
3	0.52	29.0
4	0.60	19.0
5	0.66	14.0
6	0.72	10.5
7	0.74	8.2

TABLE V-8. DETERMINATION OF α_2

I_A	α_2
2 μA	0.415
3	0.425
4	0.435
5	0.442
6	0.446
7	0.452

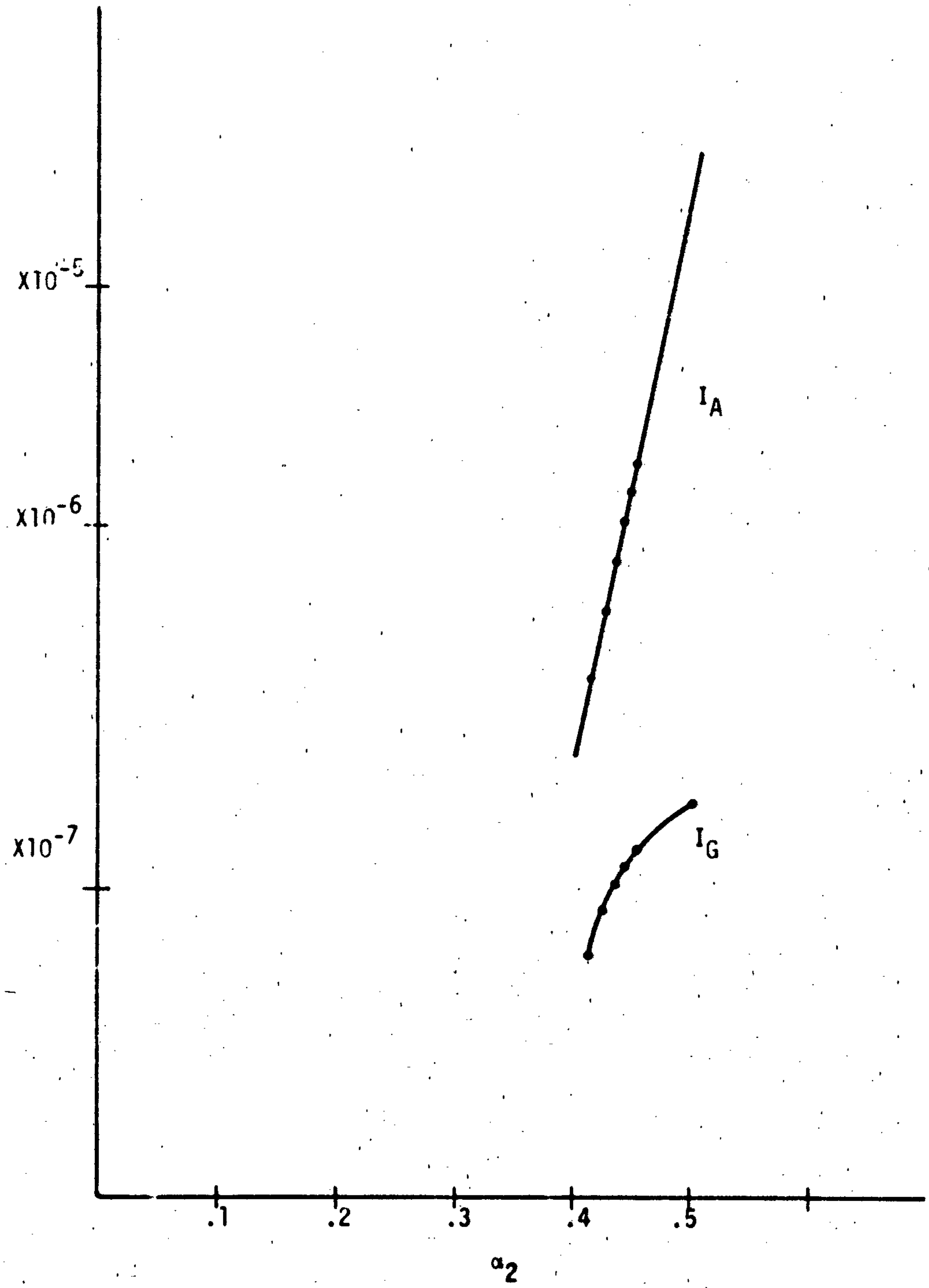


Figure V-35. Plot of SCR Measurements

$$\theta_K = \theta_A = \theta_C$$

$$I_{SK} = I_{SC} = I_{SA}$$

The junction capacitors were arbitrarily set to 1 pF for the desired application.

Manufacturer specification sheets for the 2N5061 are included in figure V-36.

3. Radiation Effects

a. Photocurrent Effects

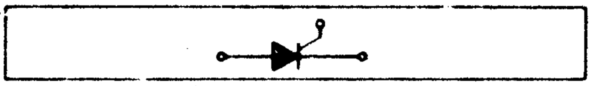
Thyristors are extremely susceptible to ionizing radiation when in the off state. Ionizing doses on the order of 10 rads delivered in a few microseconds are often sufficient to switch the thyristor to the on state.

The dominant photocurrent generator will be the reverse-biased junction between the anode gate and the cathode gate. The photocurrent may be represented by a current generator between the base of the twin transistors in the equivalent model. Photocurrents produced in this region will undergo some degree of avalanche multiplication. The exact photocurrent required to produce switching will be affected by bias, external circuitry, ionizing radiation waveform, and device parameters. The value of the photocurrent generator and the radiation levels which produce switching are best determined by experiment. The device behavior under irradiation may be described by:

$$I_A = \frac{\alpha_2 I_g + I_{pp}}{1 - (\alpha_1 + \alpha_2)}$$

where the alphas are current dependent and I_{pp} is the photocurrent produced across the reverse biased junction in the biased off state.

2N5060 (SILICON)
thru
2N5064



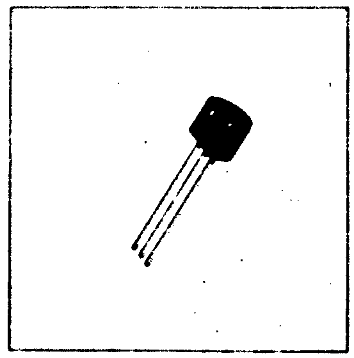
PLASTIC SILICON CONTROLLED RECTIFIERS

0.8 AMPERE RMS
30 thru 200 VOLTS

PLASTIC THYRISTORS

Annular PNPN devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

- Sensitive Gate Trigger Current – 200 μA Maximum
- Low Reverse and Forward Blocking Current – 50 μA Maximum, T_C = 125°C
- Low Holding Current – 5.0 mA Maximum
- Passivated Surface for Reliability and Uniformity

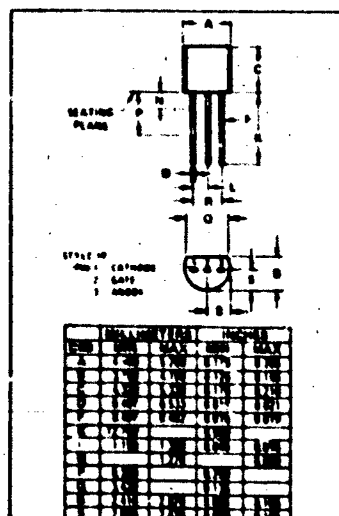


MAXIMUM RATINGS(1)

Rating	Symbol	Value	Unit
Peak Reverse Blocking Voltage	V_{RRM}		Volts
2N5060		30*	
2N5061		60*	
2N5062		100*	
2N5063		150*	
2N5064		200*	
Forward Current RMS (See Figures 4 & 5) (All Conduction Angles)	$I_{T(RMS)}$	0.8	Amp
Peak Forward Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	6.0*	Amp
Circuit Fusing Considerations, T_A = 25°C (t = 1.0 to 8.3 ms)	I^2t	0.15	A^2s
Peak Gate Power – Forward, T_A = 25°C	P_{GM}	0.1*	Watt
Average Gate Power – Forward, T_A = 25°C	$P_{GF(AV)}$	0.01*	Watt
Peak Gate Current – Forward, T_A = 25°C (300 μs, 120 PPS)	I_{GM}	1.0*	Amp
Peak Gate Voltage – Reverse	V_{GRM}	5.0*	Volts
Operating Junction Temperature Range @ Rated V_{RRM} and V_{DRM}	T_J	-65 to +125*	°C
Storage Temperature Range	T_{stg}	-65 to +150*	°C
Lead Solder Temperature (<1/16" from case, 10 s max)	–	+230*	°C

*Indicates JEDEC Registered Data

(1) Temperature reference point for all case temperatures is center of flat portion of package. (T_C = +125°C unless otherwise noted.)



CASE 29-02
TO-92

Figure V-36. 2N5061 Manufacturer Specification Sheets (ref. V-3)

2N5060 thru 2N5064 (continued)

ELECTRICAL CHARACTERISTICS (R_{GK} = 1000 Ohms)

Characteristic		Symbol	Min	Max	Unit
Peak Forward Blocking Voltage (Note 1)		V_{DRM}			Volts
(T_C = 125°C)	2N5060		30*	–	
	2N5061		60*	–	
	2N5062		100*	–	
	2N5063		150*	–	
	2N5064		200*	–	
Peak Forward Blocking Current (Rated V_{DRM} @ T_C = 125°C)		I_{DRM}		50*	µA
Peak Reverse Blocking Current (Rated V_{RRM} @ T_C = 125°C)		I_{RRM}		50*	µA
Forward "On" Voltage (Note 2) (I_{TM} = 1.2 A peak @ T_A = 25°C)		V_{TM}		1.7*	Volts
Gate Trigger Current (Continuous dc) (Note 3)	T_C = 25°C	I_{GT}		200	µA
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -65°C			350*	
Gate Trigger Voltage (Continuous dc)	T_C = 25°C	V_{GT}		0.8	Volts
(Anode Voltage = 7.0 Vdc, R_L = 100 Ohms)	T_C = -65°C			1.2*	
(Anode Voltage = Rated V_{DRM}, R_L = 100 Ohms)	T_C = 125°C	V_{GD}	0.1	–	
Holding Current	T_C = 25°C	I_H		5.0	mA
(Anode Voltage = 7.0 Vdc, initiating current = 20 mA)	T_C = -65°C			10*	
Thermal Resistance, Junction to Case (Note 4)		θ_{JC}		75*	°C/W
Thermal Resistance, Junction to Ambient		θ_{JA}		200	°C/W

*Indicates JEDEC Registered Data

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous dc basis without incurring damage. Ratings apply for zero or negative gate voltage but positive gate voltage shall not be applied concurrently with a negative potential on the anode. When checking forward or reverse blocking capability, thyristor devices should not be tested with a constant current source in a manner that the voltage applied exceeds the rated blocking voltage.
2. Forward current applied for 1.0 ms maximum duration, duty cycle ≤ 1.0%.
3. R_{GK} current is not included in measurement.
4. This measurement is made with the case mounted "flat side down" on a heat sink and held in position by means of a metal clamp over the curved surface.

FIGURE 1 – SURGE RATINGS

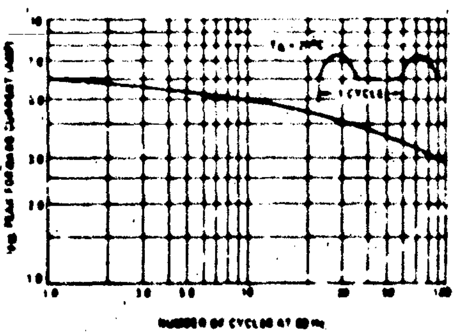


FIGURE 2 – POWER DISSIPATION

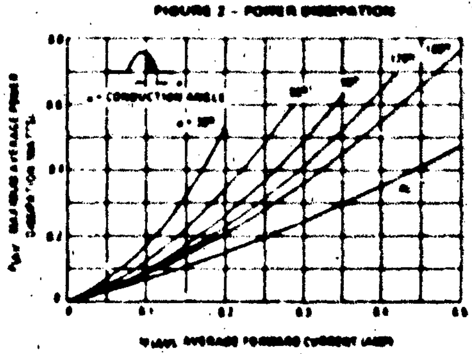


Figure V-36. 2N5061 Manufacturer Specification Sheets (Continued)

FIGURE 3 - FORWARD VOLTAGE

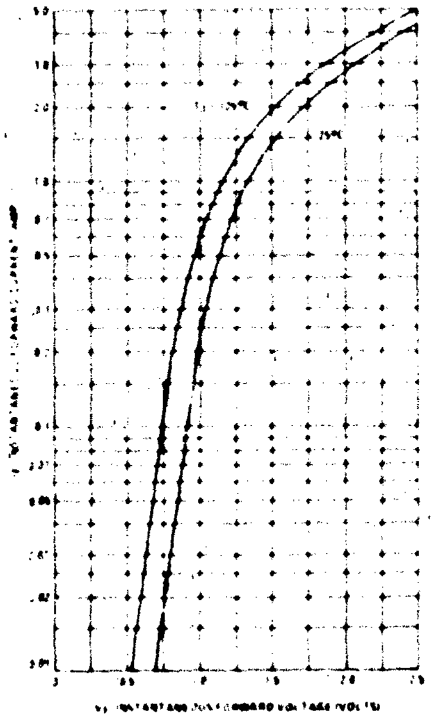


FIGURE 4 - CURRENT DERATING (REFERENCE: CASE TEMPERATURE)

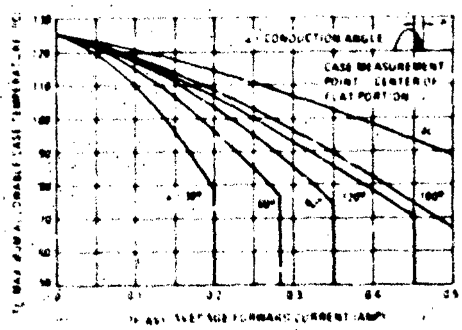


FIGURE 5 - CURRENT DERATING (REFERENCE: AMBIENT TEMPERATURE)

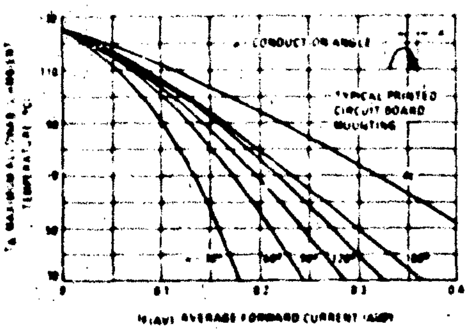


FIGURE 6 - THERMAL RESPONSE

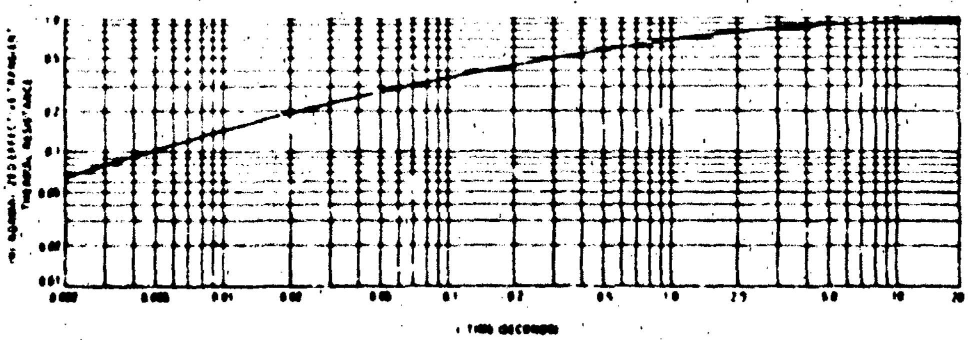


Figure V-36. 2N5061 Manufacturer Specification Sheets (Continued)

TYPICAL CHARACTERISTICS

FIGURE 7 — GATE TRIGGER VOLTAGE

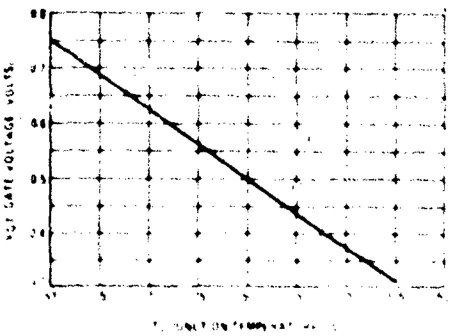


FIGURE 8 — GATE TRIGGER CURRENT

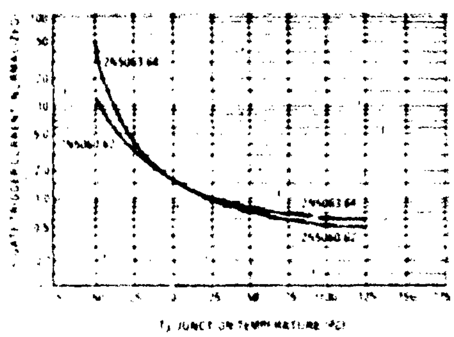


FIGURE 9 — HOLDING CURRENT

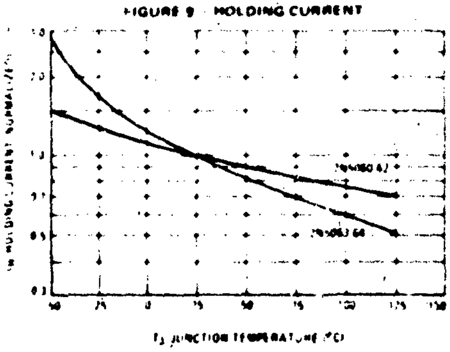
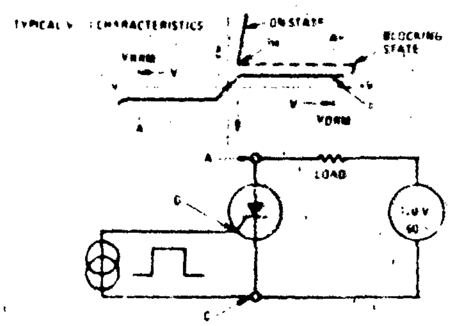


FIGURE 10 — CHARACTERISTICS AND SYMBOLS



SELECTED THYRISTOR TRIGGER APPLICATION NOTES

AN 240	SCR Power Control Fundamentals
AN 290B	Mounting Procedures for, and Thermal Aspects of, Thermopad Plastic Power Devices
AN 295	Suppressing RFI in Thyristor Circuits
AN 422	Testers for Thyristors and Trigger Devices
AN 453	Zero Point Switching Techniques

To obtain copies of these notes list the AN number(s) on your company letterhead and send your request to

Technical Information Center
Motorola Semiconductor Products, Inc
P.O. Box 20924
Phoenix, Arizona 85036

Figure V-36. 2N5061 Manufacturer Specification Sheets (Concluded)

b. Neutron Effects

Neutron damage will decrease the alphas of the model transistors. As a result, neutrons will make the thyristor harder to switch to the on state. As a result of the decrease in alpha, the breakover voltage will increase along with the holding current, and the saturation resistance. If the thyristor is not severely damaged, it will still show switching behavior.

The dominant physical mechanism of damage in SCR's is the lowering of minority carrier lifetime. This effect, and other neutron effects on the behavior of transistors, is discussed in more detail in chapter III.B.7.

Thyristors generally show switching behavior up to 10^{12} n/cm^2. Care must be taken in the circuit design to supply the increased requirement for gate trigger current.

4. Computer Example

The model for the 2N5061 was tested using SCEPTRE. SCEPTRE was chosen due to the high flexibility required by this thyristor model. This model did prove to be somewhat unwieldy during verification runs and certainly does not represent the easiest SCR model to use.

The test circuit for the SCR model is illustrated in figure V-37. The gate is driven by a constant 0.72 μA and the anode to cathode voltage is ramped to 20 V in 1 millisecond. Data obtained for the 2N5061 indicate that the SCR should switch when the anode to cathode voltage reaches 10.5 volts.

The test circuit, as input to SCEPTRE, is illustrated in figure V-38. The SCEPTRE output of figure V-39 produces a simulated breakover voltage of 9.6 volts.

D. TRANSFORMER MODELING

1. Introduction

There are two methods by which transformer models may be developed.

(1) An equivalent circuit developed through physical reasoning.

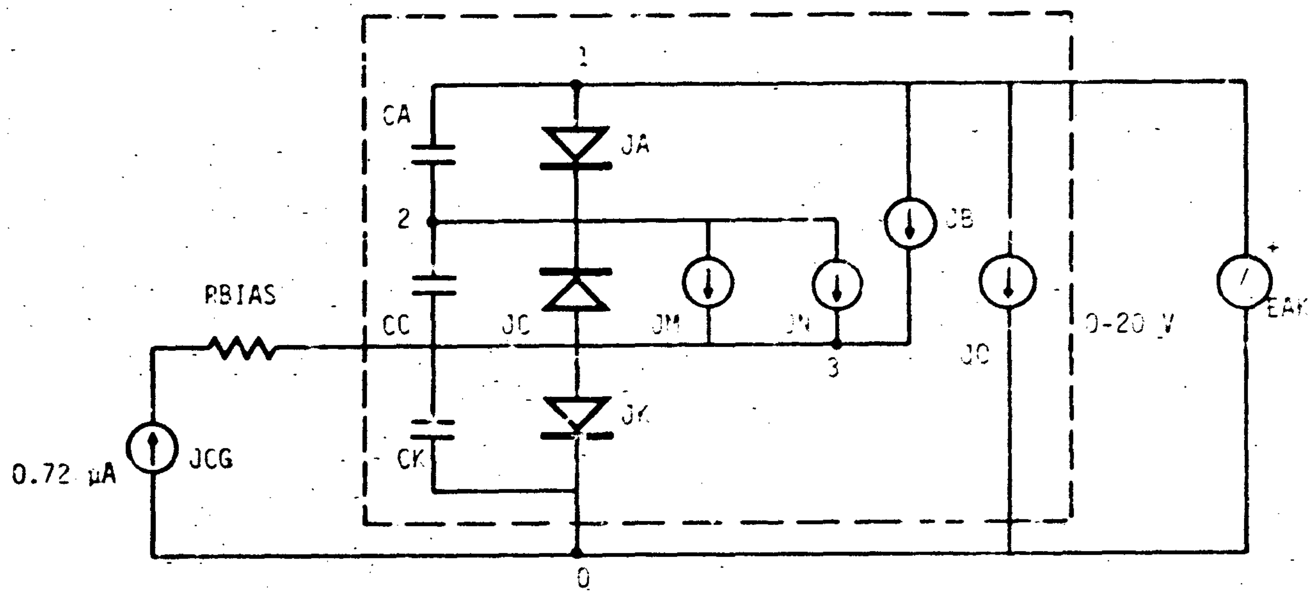


Figure V-37. SCR Test Circuit

```
S C E P T R E   NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2       5/76
 03/10/78    16.42.35.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD "DOCUMENT" AS THE FIRST CARD
OF THE INPUT TEXT


COMPUTER TIME ENTERING SETUP PHASE-
          CPA        .095 SEC.
          PP        0.000 SEC.
          IO        0.000 SEC.


CIRCUIT DESCRIPTION
ELEMENTS
CA,1-2=1.E-12
JA,1-2=DIODE EQUATION(7.47E-10,14.4)
CC,2-3=1.E-12
JC,3-2=DIODE EQUATION(7.47E-10,14.4)
JM,2-3=Q1(P2,JK)
JN,2-3=Q1(P1,JA)
JB,1-3=TABLE 1(VJB)
CK,3-0  .E-12
JK,3-0=DIODE EQUATION(7.47E-10,14.4)
EAK,0-X=TABLE 2(TIME)
RBIAS,X-1=1
JCG,0-3=0.72E-6
J0,1-0=0
DEFINED PARAMETERS
P1=0.5
P2=TABLE 3(JA)
FUNCTIONS
Q1(A,B)=(A*B)
TABLE 1
0,0,7.5,2.3E-7,9.8,2.5E-7,13.3,3.1E-7,18.3,3.7E-7,28.3,4.5E-7,
44.3,5.6E-7
TABLE 2
0,0,1.E-3,20
TABLE 3
2.E-6,.415,3.E-6,.425,4.E-6,.435,5.E-6,.442,6.E-6,.446,7.E-6,.452,
30.E-6,0.5,100.E-3,.9,1,.9
OUTPUTS
JA,JC,JM,JN,JB,VJB,JK,EAK,IEAK,P1,P2
IEAK,PLOT(VJ0)
IEAK,PLOT(EAK)
IEAK,JCG,PLOT
RUN CONTROLS
STOP TIME=1.E-3
MAXIMUM PRINT POINTS=100
MINIMUM STEP SIZE=1.E-39
END

SYSTEM NOW ENTERING SIMULATION
```

Figure V-38. SCEPTRE Input for SCR Tests

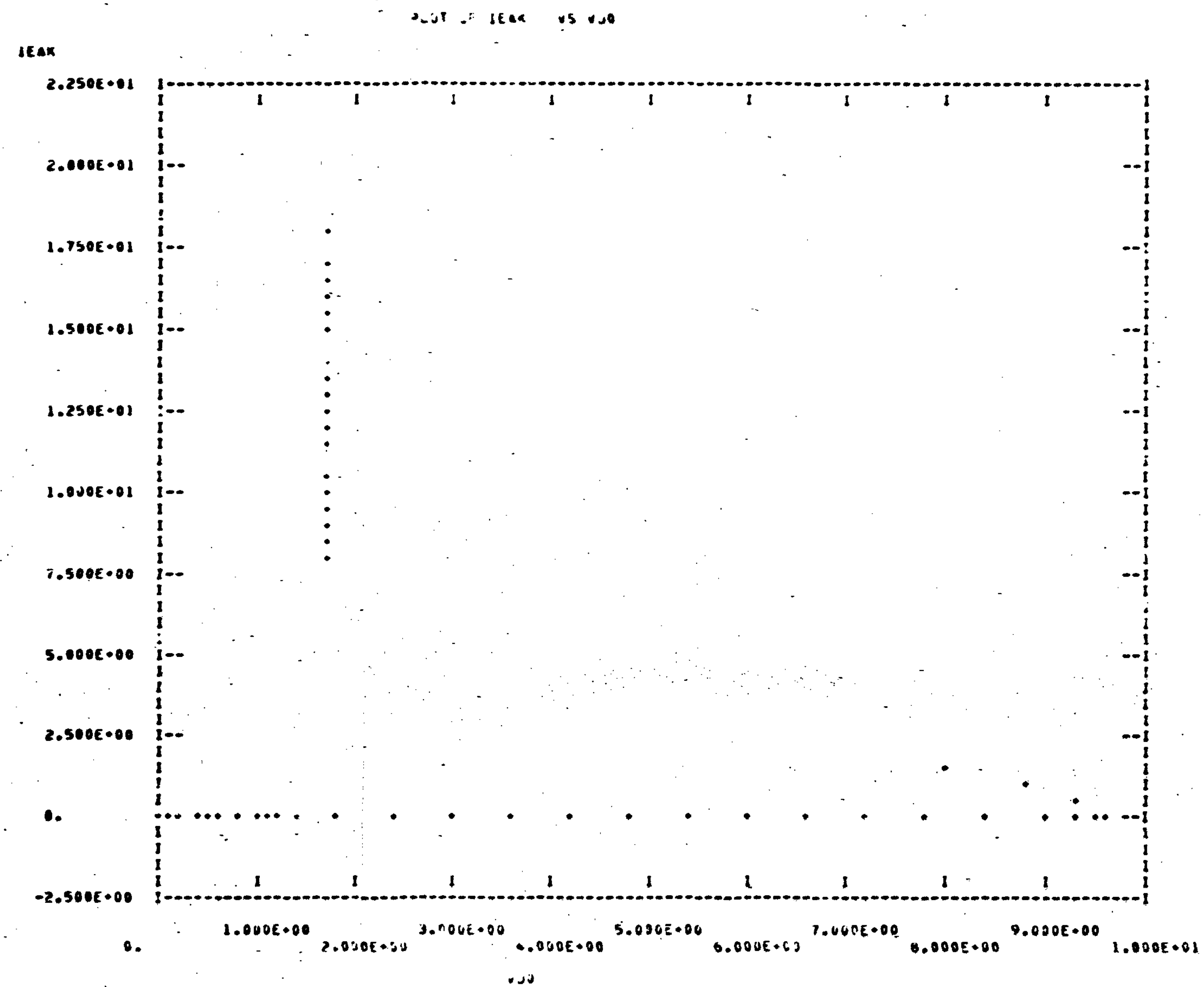


Figure V-39. SCR Characteristics

(2) An equivalent circuit based on the theory of magnetic circuits.

Method 1 yields the familiar textbook models for transformers. These models consist of an ideal transformer element and the associated parasitics. Any real transformer may be modeled as an ideal transformer by inclusion of the proper parasitic elements. The ideal transformer requires the following assumptions:

(1) No Losses

(2) Unity Coupling

(3) Infinite Inductance of the Primary and Secondary Coils

The relevant equations for the ideal transformer are:

$$V_p = \frac{N_p}{N_s} V_s$$

$$I_p = \frac{N_s}{N_p} I_s$$

$$Z_p = \left(\frac{N_p}{N_s}\right)^2 Z_s$$

Implementation of these equations requires knowledge of the driving point impedance of the circuit. The circuit shown in figure V-40 may be transformed to the equivalent circuit shown in figure V-41.

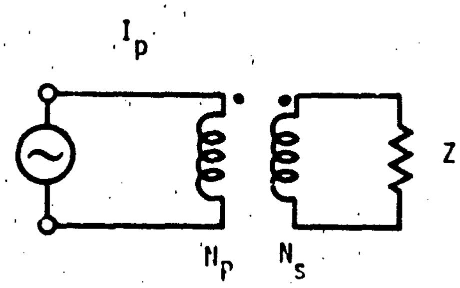


Figure V-40. Transformer Inclusive Circuit

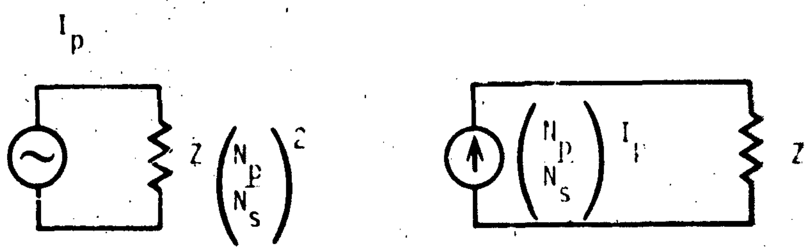


Figure V-41. Transformed Circuit for Analysis

The transformer "dot" convention is also important. The convention implies that a positive voltage applied to the primary "dot" will induce a positive voltage at the secondary "dot". Any real transformer may be modeled as an ideal transformer if the proper parasitic elements are included as part of the model. Techniques for determining the values and placement of the parasitic elements are discussed in reference V-4.

Difficulties are encountered when attempting to place the "physical reasoning" model in a computer simulated circuit. First, there are problems associated with impedance transformations and reflections. Second, there are difficulties in developing a model if a nonlinear, active, or frequency dependent load is being driven by the transformer.

Such problems are not encountered if a "magnetic circuit" model is applied. It is for this reason that the "magnetic circuit" model is developed in detail in the following sections.

2. Transformer Model

a. Description

The coupled coils model presented uses dependent voltage sources to model magnetic coupling effects.

b. Advantages

The model is a "drop-in" model requiring no impedance or voltage transformations It has been applied in very simple network analysis codes.

c. <u>Cautions</u>

Nonlinear and second order effects are not included in this model. The parasitic elements are modeled in a very simplistic manner.

d. <u>Characteristics</u>

The model for the coupled coils is illustrated in figure V-42.

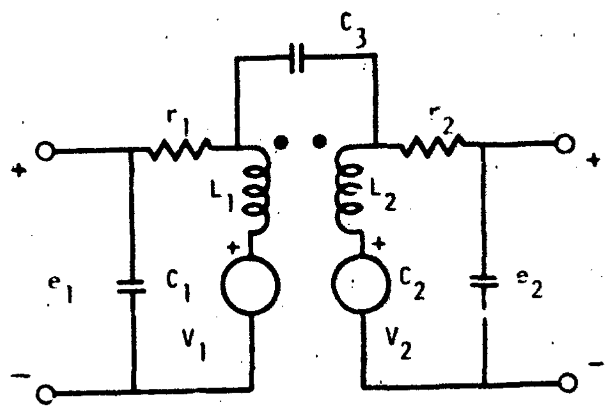


Figure V-42. Equivalent Circuit for Coupled Coils

e. <u>Defining Equations</u>

$$V_1 = \frac{M\,V_{L2}}{L_2}$$

$$V_2 = \frac{M\,V_{L1}}{L_1}$$

f. <u>Parameter List</u>

M = mutual inductance
L_1 = inductance of coil 1
L_2 = inductance of coil 2
V_1 = value of dependent voltage source 1

V_2 = value of dependent voltage source 2

V_{L1} = the voltage across L_1

V_{L2} = the voltage across L_2

r_1 = the primary winding resistance

r_2 = the secondary winding resistance

C_1 = the parasitic winding capacitance of the primary

C_2 = the parasitic winding capacitance of the secondary

C_3 = the interwinding capacitance

g. Parameterization

1) L_1, L_2

a) Definition

L_1 and L_2 are the small signal inductance values of the primary and secondary coils, respectively.

b) Typical Value

A large range of values for L_1 and L_2 are possible. Typical values range from 1 microhenry to 100 henries.

c) Measurement

L_1 can be measured by connecting an inductance bridge across the primary winding and leaving the secondary winding leads unconnected or open. To avoid the effects of capacitive parasitics, the inductance measurement should be made at the lowest frequency possible. Measurements made in the low kilohertz range are generally adequate.

L_2 is measured in the same manner as L_1. For the L_2 measurement, the primary winding leads are left open.

d) Example - S12X

L_1, the primary inductance, was determined to be 1.06 henry on a 1 kHz impedance bridge. L_2, the secondary inductance, was found to be 1.88 mH.

2) M

a) Definition

M is the value of mutual inductance for coupled coils.

b) Typical Value

M is defined as:

$$M = K\sqrt{L_1 L_2}$$

where K is the coupling coefficient and is unity for an ideally coupled circuit. M is therefore a strong function of coil inductance which may vary widely.

c) Measurement

Two coupled coils are connected in series and their total inductance is measured and recorded. This is done best at lower frequencies. The connections are reversed and the inductance of the two coils is again measured in series. The two measurements will produce a series aiding inductance, L_a, and a series opposing inductance, L_o. The higher inductance of the two measurements is the series aiding value. The mutual inductance can now be calculated as:

$$M = \frac{L_a - L_o}{4}$$

d) Example - S12X

Aiding inductance of the S12X transformer was measured as 1140 mH. Opposing inductance was measured at 980 mH. M was determined as:

$$M = \frac{1140\ \text{mH} - 980\ \text{mH}}{4}$$

$$M = 0.04\ \text{henries}$$

3) r_1, r_2

a) Definition

r_1 and r_2 are the ohmic resistance values of the primary and secondary windings, respectively. r_1 and r_2 are actually

frequency dependent due to such high frequency phenomenon as the skin effect. r_1 and r_2 are distributed in L_1 and L_2, respectively, but are treated as single elements for this model.

b) Typical Value

r_1 and r_2 can range from a negligible value of resistance to several kilohms.

c) Measurement

r_1 is measured by connecting a sensitive ohmeter across the primary leads and measuring the resistance value. r_2 is measured in a similar manner across the secondary leads.

d) Example - S12X

The resistance of the primary coil was measured as 140 ohms. The resistance of the secondary coil was found to be 0.58 ohms.

4) C_1, C_2

a) Definition

C_1 and C_2 represent the interwinding capacitance within the primary and secondary coils. C_1 and C_2 are actually distributed, but are assumed to be discrete elements connected across the primary and secondary inputs for this model.

b) Typical Values

C_1 and C_2 are typically several picofarads.

c) Measurement

Measurement of C_1 and C_2 is difficult. One procedure is to measure the capacitance of a winding with the other winding op . at a frequency at which the inductive impedance of the coil is much greater than the capacitive impedance.

d) Example - S12X

The intercoil capacitance was measured across the primary at 1 MHz as 0.6 pF. The capacitance across the secondary was measured as 0.5 pF.

5) C_3

a) Definition

C_3 is a capacitance value which represents the distributed capacitance between two closely wound coils.

b) Typical Value

The typical value of C_3 is several picofarads.

c) Measurement

A value for C_3 can be found by shorting the primary leads together and then shorting the secondary leads together. A capacitance bridge can then be used to determine the capacitance between the primary and secondary coils by connection across the primary and secondary leads.

d) Example - S12X

The coupling capacitance between the primary and secondary was measured at 1 MHz as 77 pF.

3. Higher Order Effects

a. Multiple Port Transformers

To model multiple-coupled coils, the mutual inductance between all the interacting coils must be defined. Consider the three port transformer of figure V-43. The relevant equations are:

$$e_1 = L_1 \frac{di_1}{dt} + \frac{M_{12}}{L_2} V_{L2} + \frac{M_{13}}{L_3} V_{L3} + r_1 i_1$$

$$e_2 = \frac{M_{12}}{L_1} V_{L1} + L_2 \frac{di_2}{dt} + \frac{M_{23}}{L_3} V_{L3} + i_2 r_2$$

$$e_3 = \frac{M_{13}}{L_1} V_{L1} + \frac{M_{23}}{L_2} V_{L2} + L_3 \frac{di_3}{dt} + i_3 r_3$$

Therefore, coil 1 would be modeled as shown in figure V-44. Similiar models hold for coils 2 and 3. The general rule is that if there are N

coupled coils, each coil will be modeled as above with (N-1) voltage sources (one voltage source for each of the other N-1 coils).

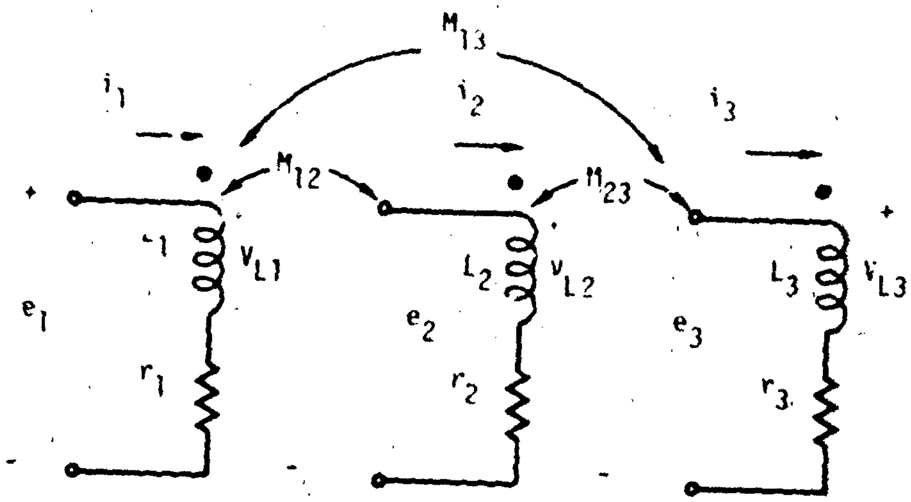


Figure V-43. Three Port Transformer

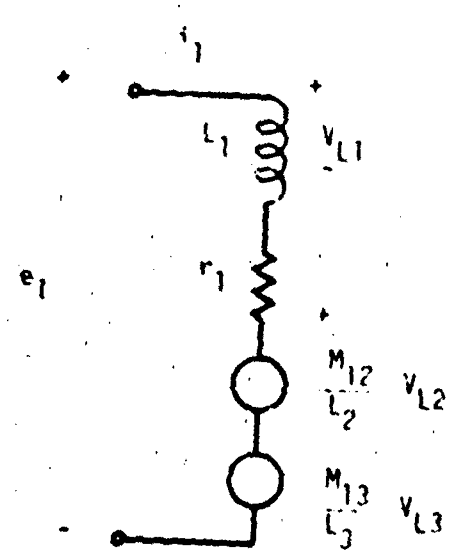


Figure V-44. Port Model

b. Saturation and Hysteresis

Special and fairly involved subprograms may be required to model nonlinear flux versus magnetic force characteristics. For single windings,

$$L = N \frac{d\phi}{dI}$$

where:

ϕ = magnetic flux as a function of I

L = coil inductance

I = coil current

N = coil turns

To model the nonlinear characteristic of a single inductor, a plot of flux as a function of inductor current is required. Taking the derivative of this plot yields $d\phi/dI$. Multiplying the derivative by N yields the inductor value as a function of current. The $d\phi/dI$ values may be expressed in a tabular manner or analytically.

Hysteresis may be modeled in a similar manner. Two flux versus current paths are now possible, a magnetizing path and a demagnetizing path.

The problem becomes more complex when a transformer is considered. The value of each winding inductance will be a function of the winding current and a function of every other winding current.

Further information on the computer-aided modeling of nonlinear magnetic effects may be found in reference V-5.

4. Model Development From Data Sheets

Useful models may be developed from the manufacturer specification sheets. Unfortunately, the data sheets vary widely in the format and type of information presented.

One widely-used format lists the primary and secondary impedances, the lower 3 dB frequency of the transfer function, f_L, and the

upper 3 dB frequency of the transfer function, f_H. The impedances are the rated source and load resistances between which the performance ratings are determined. Reductions or increases in the source or load resistance would alter the frequency performance limits. The model parameters can be determined from these specifications as:

$$G_0 = \frac{k\sqrt{\frac{L_1}{L_2}}}{\frac{L_1}{L_2} + \frac{Z_S}{Z_L}}$$

$$f_L = \frac{G_o Z_S}{2\pi k\sqrt{L_1 L_2}}$$

$$f_H = \frac{k\ Z_L}{2\pi(1 - k^2)\sqrt{L_1 L_2\ G_o}}$$

Under impedance matched conditions:

$$L_2 = \frac{Z_L}{4\pi f_L}$$

$$L_1 = \frac{Z_S}{4\pi f_L}$$

$$k = \sqrt{1 - 4\left(\frac{f_L}{f_H}\right)}$$

$$M = K\sqrt{L_1\ L_2}$$

The transformer transfer characteristic is shown in figure V-45.

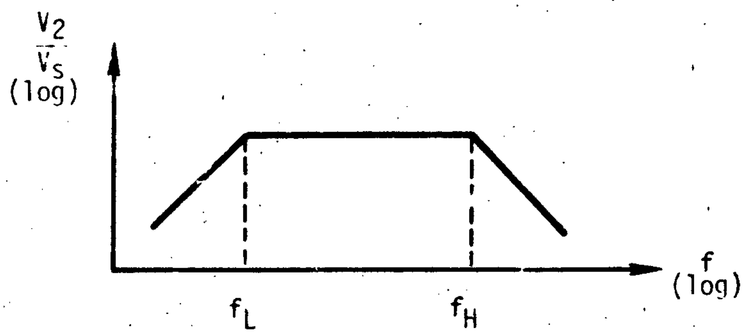


Figure V-45. Transformer Transfer Characteristic

Similar relations exist for the transformer input impedance:

$$f_o = \frac{r_1}{2\pi L_1}$$

$$f_1 = \frac{Z_L}{2\pi L_2}$$

$$f_2 = \frac{f_1}{(1 - k^2)L_2}$$

Under impedance matched conditions:

$$L_2 = \frac{Z_L}{2\pi f_1}$$

$$L_1 = \left(\frac{Z_o}{Z_L}\right) L_2$$

$$k = \sqrt{1 - \frac{f_1}{f_2}}$$

$$M = K\sqrt{L_1 L_2}$$

The transformer input impedance characteristic is shown in figure V-46.

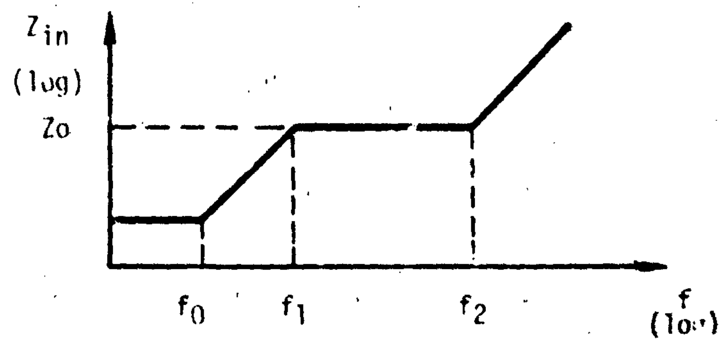


Figure V-46. Transformer Input Impedance Characteristic

5. Radiation Effects

Transformers are relatively resistant to radiation damage. Transformers and relays require doses of over 10^9 rads to produce damage. The damage is manifested as the degradation of insulating material and expansion of potting compounds.

Ionizing radiation does produce some transient leakage through insulators, but this effect is generally of no importance.

EMP may be a serious problem as overvoltage could be coupled through a transformer. Another possibility is arcing across adjacent wires in the winding. The arcing problem may require the monitoring of voltages across the transformer.

6. Computer Example

To verify the validity of the S12X model, a transfer characteristic was obtained from the SPICE code. This transfer function was then compared to the actual transfer function which was determined from data obtained using a vector voltmeter.

The test circuit input to SPICE to determine the transfer function to the transformer is illustrated in figure V-47. The SPICE listing shown in figure V-48 produces the transfer characteristic. The results of the simulation, together with the experimental data, are shown in figure V-49. At the normal operating frequencies of the transformer, good simulation results have been obtained. The model does predict the first resonance point but simulation ability is lost at higher frequencies due to the simplified modeling of the parasitic effects.

E. REFERENCES

V-1. Semiconductor Data Library, Motorola Semiconductor Products Inc., 1974.

V-2. Preferred Semiconductors and Components From Texas Instruments, Texas Instruments, 1968-1969 Catalog.

V-3. Semiconductor Data Library, Motorola Semiconductor Products Inc., 1974.

V-4. Fitzgerald, A. E., C. Kingsley, and K. Alexander. Electric Machinery, McGraw-Hill Book Company, 1971.

V-5. Bowers, J. C. and S. R. Sedore. SCEPTRE: A Computer Program for Circuit and Systems Analysis, Prentice Hall, Englewood Cliffs, New Jersey, 1971.

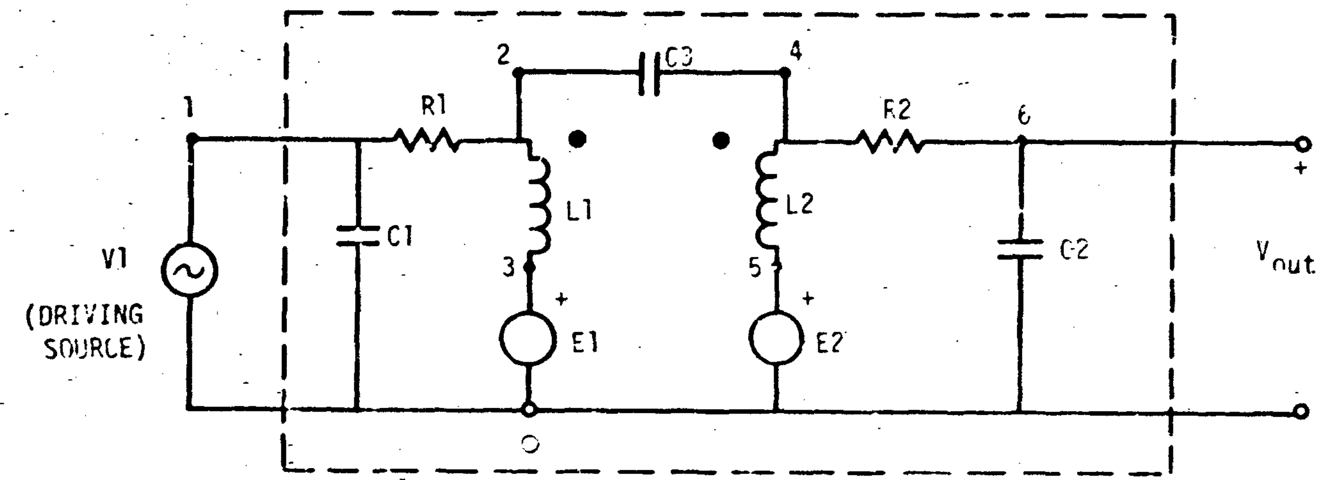


Figure V-47. Transformer Test Circuit

```
***** 01/22/78 ********  SPICE 2G.2 (26SEP76)  ******** 12.45.32.*****

*TRANSFORMER MODEL

     INPUT LISTING                          TEMPERATURE =   27.000 DEG C

**********************************************************************

V1 1 0 AC 1
C1 1 0 0.6E-12
R1 1 2 140
L1 2 3 1.06
E1 3 0 4 5 21.3
C3 2 4 77.E-12
L2 4 5 1.8HE-3
E2 5 0 2 3 3.77E-2
R2 4 6 0.52
C2 6 0 0.5E-12
.PLOT AC VDB(6)
.AC DEC 10 1KHZ 100MEGHZ
.END
```

Figure V-48. SPICE Input

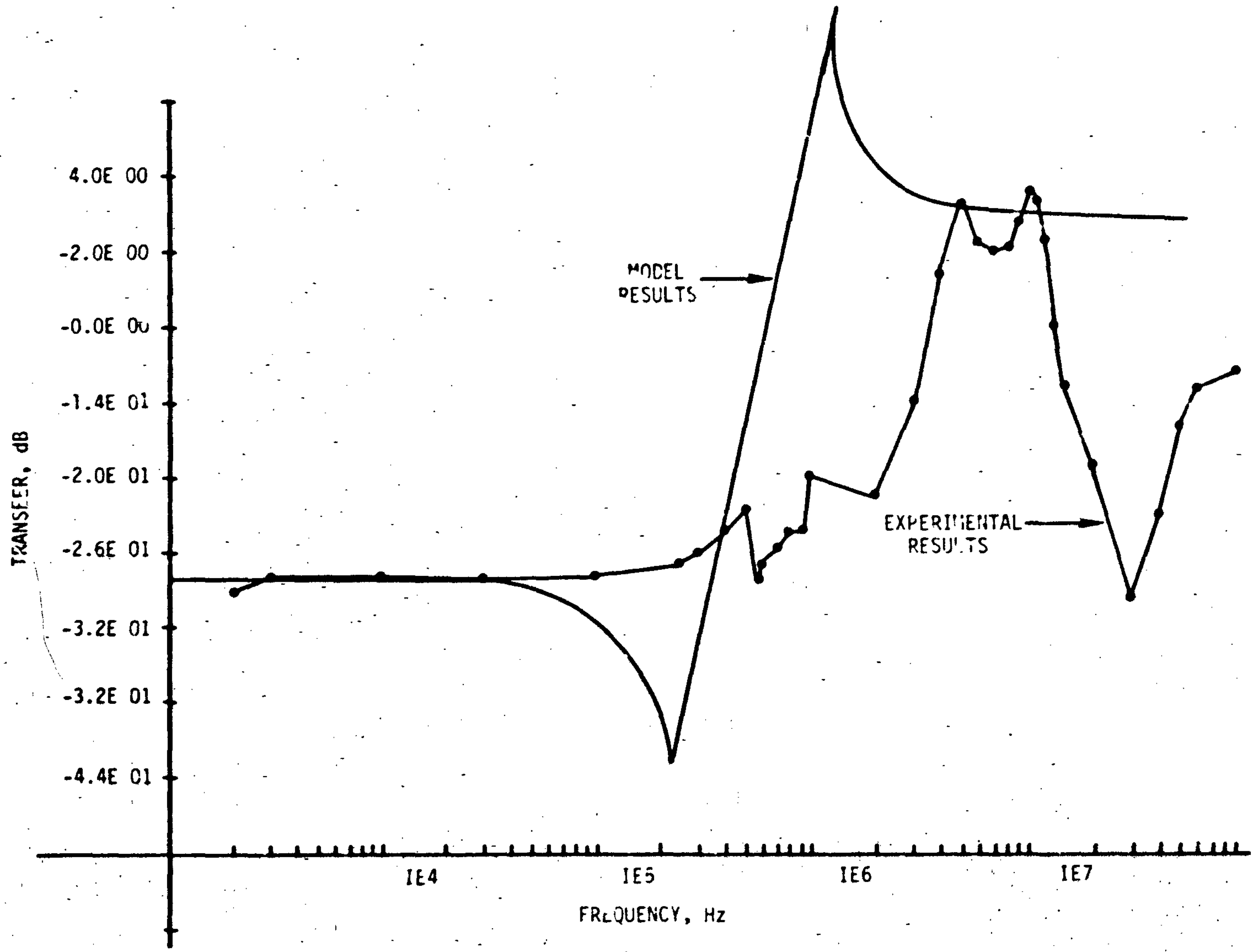


Figure V-49. Transformer Data

CHAPTER VI

SIMPLIFIED MODELING

CHAPTER VI

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CHAPTER VI
SIMPLIFIED MODELING

A. INTRODUCTION TO SIMPLIFIED MODELING

The analyst confronted with the problem of determining the vulnerability of systems containing IC's (integrated circuits) must decide just how to model the IC's. In some cases, he may be able to test the IC, find out where it fails, and set the system failure level equal to the lowest IC failure level. More often, however, a clear definition of IC failure may not be possible since IC's typically show gradual degradation due to neutron or total dose environments. Similarly, the short transients produced by $\dot{\gamma}$ radiation may or may not be important to system operation. Thus, computer-aided circuit analysis may be required to determine whether the IC response leads to system failure.

There are two possible approaches to modeling IC's. The first of these is detailed modeling of the elements that make up the IC. This requires knowledge of the actual structure of the IC, including knowledge of the parasitic devices. Such information is difficult to obtain since manufacturers are usually not willing to release it, and direct measurement of individual devices on the IC is usually not possible. Furthermore, such detailed IC models require large amounts of core storage and computing time, limiting the number of IC's that can be treated in any one simulation. Detailed modeling of IC's may be applicable to the study of IC response, but is not generally applicable to the study of system response.

The second approach to the modeling of IC's, simplified modeling, is the subject of this chapter. In simplified modeling, the response of the IC as measured at the terminals is simulated to provide the correct voltages and currents as a function of time and stimulus. This modeling is done without regard to the actual electronic devices within the IC which

produce that response, and simplified models frequently bear little resemblance to the physical properties of such devices. A simplified model is really only a mathematical description of the measured response of an IC to certain stimuli.

The analyst must remember that, while a detailed model might be used to predict IC response, a simplified model can only simulate IC response. If a simplified model is applied to regions where the simulation is not valid, the resulting predictions of system response can be grossly in error. Let the analyst beware!

The sophistication of the simplified model may be limited by the properties of the particular circuit analysis code used. SCEPTRE allows user-defined models, parameters, equations, tables, and FORTRAN subroutines, and can thus implement virtually any simplified model that can be described mathematically. In addition, SCEPTRE/LOGIC (to be discussed in section C) allows straightforward simulation of complex logic circuits such as those found in LSI (large scale integrated) circuits. NET-2 has capabilities similar to those of SCEPTRE, and the system elements available in Release 9 provide many of the capabilities of SCEPTRE/LOGIC. Other codes provide less flexibility, but still incorporate features such as controlled current and voltage sources, piecewise linear approximation, and other useful tools.

Increased model sophistication comes at the expense of increased memory requirements, increased running times, and increased chances for error. The analyst should always use the simplest model which will meet the required needs; however, a sophisticated model should not be used simply because it is familiar or because the code allows it, nor should the analyst model details of the response if those details will be swamped by data uncertainties

This chapter cannot be the definitive work on simplified modeling, and the analyst is referred to the many references (see references VI-1 through VI-6) on the subject for greater detail. It is the goal of this

chapter to introduce the analyst to the concept and philosophy of simplified modeling and to illustrate its implementation with concrete examples. It is hoped this will trigger a spark of inventiveness within the reader which will enable simplified modeling techniques to be applied to unique problems.

Since the requirements of simplified modeling of linear and digital integrated circuits differ, they are discussed separately. In section B, linear circuits are discussed and illustrated through actual modeling of a 741DC operational amplifier. In section C, simplified modeling of digital integrated circuits is discussed. Techniques for modeling input and output characteristics are presented along with techniques for modeling logic circuit response either through subroutines or through the use of SCEPTRE/LOGIC or NET-2 system elements. Examples are presented to illustrate the concepts involved.

B. SIMPLIFIED MODELING OF LINEAR CIRCUITS AND SYSTEMS

1. Introduction

The complexity involved in modeling large linear circuits generally requires techniques of simplified modeling. The technique of simplified modeling treats the complex circuit like a black box with only the terminal behavior considered important.

The simulation accuracy of a simplified model can be improved to any degree of accuracy required, but only at the expense of model complexity. Only the circuit characteristics required for the correct solution of the problem need be included in a simplified model. Some features which might be considered for inclusion into a simplified model are:

(1) The voltage gain, current gain, or other ideal function of the circuit.

(2) The input and output impedance.

(3) The frequency and transient response.

(4) The large signal characteristics.

(5) The radiation response.

Only the particular features needed should be included. These features are discussed in a modular fashion to facilitate inclusion of only necessary features.

An example of simplified modeling of a 741DC operational amplifier is presented here to help illustrate the concepts. This model is quite sophisticated and is used in example 3 of chapter VII. However, a much simpler model of a 741 is used in example 2 of chapter VII where a fully detailed model is not needed. These examples illustrate the range of simplifications in the model which might be used under differing circumstances.

The techniques illustrated here may be applied to linear circuits other than operational amplifiers.

2. Modeling Frequency Characteristics

One of the more difficult features to incorporate into a model is the frequency response of the circuit. One method of approaching this problem is to treat the circuit as a series of interconnected functional stages. Each stage can then model a particular characteristic. For example, an amplifier has the frequency characteristic of figure VI-1.

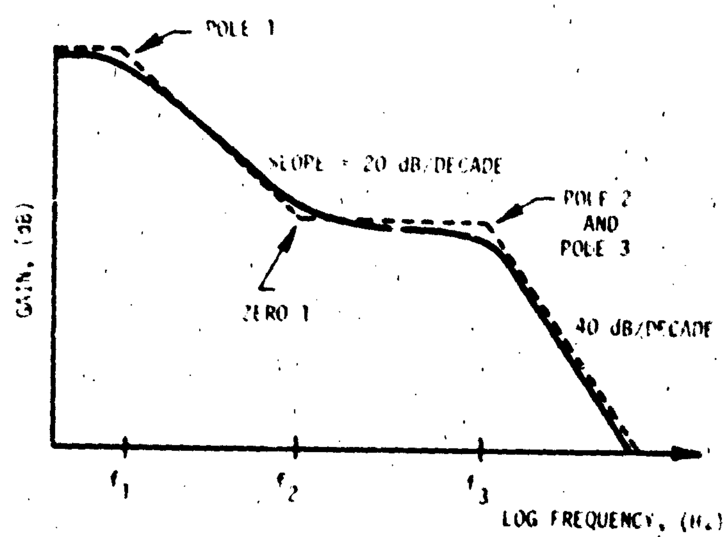


Figure VI-1. Frequency Characteristic

The frequency characteristic of figure VI-1 may be modeled by application of the two frequency shaping networks shown in figure VI-2.

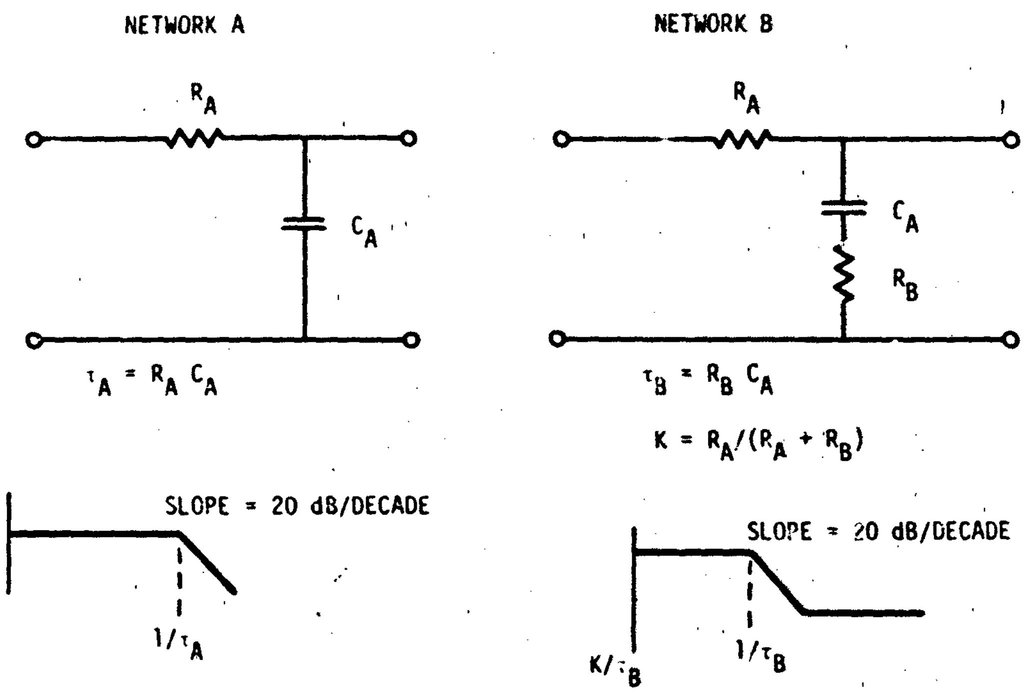


Figure VI-2. Frequency Networks

To model pole 1 and zero 1, choose R_A of network B to be any value. C_A is solved from:

$$f_1 = \frac{1}{2\pi\,(R_A\,C_A)}$$

R_B is now found as:

$$f_2 = \frac{1}{2\pi\,(R_B\,C_A)}$$

The double pole at f_3 can be modeled by application of network A.

$$f_3 = \frac{1}{2\pi\,(R_C\,C_L)}$$

To implement the frequency shaping networks in the amplifier model, it must be remembered that these networks cannot be loaded or their transfer characteristics will be altered, and network A must be included twice to simulate the double pole at frequency f_3. A dependent source may be used to conveniently implement each filter network as a separate stage to avoid any coupling problems. Such a staged network is illustrated in figure VI-3.

3. Example of Simplified Modeling

Simplified modeling is best explained through the use of an example. It is desired to generate a simplified model of a μA741DC op amp (operational amplifier). The following characteristics were chosen as being critical for obtaining the desired simulation results:

(1) Offset Voltage
(2) Open Loop Gain as a Function of Frequency
(3) CMRR (common mode rejection ratio)
(4) PSRR (power supply rejection ratio)
(5) Input Bias Current
(6) Offset Current
(7) Supply Current (no load)
(8) Input Capacitance
(9) Output Resistance
(10) Output Voltage Swing
(11) Slew Rate
(12) Radiation Effects

a. Definitions

i) Offset Voltage

Offset voltage is defined as the differential input voltage required to obtain zero volts at the amplifier output.

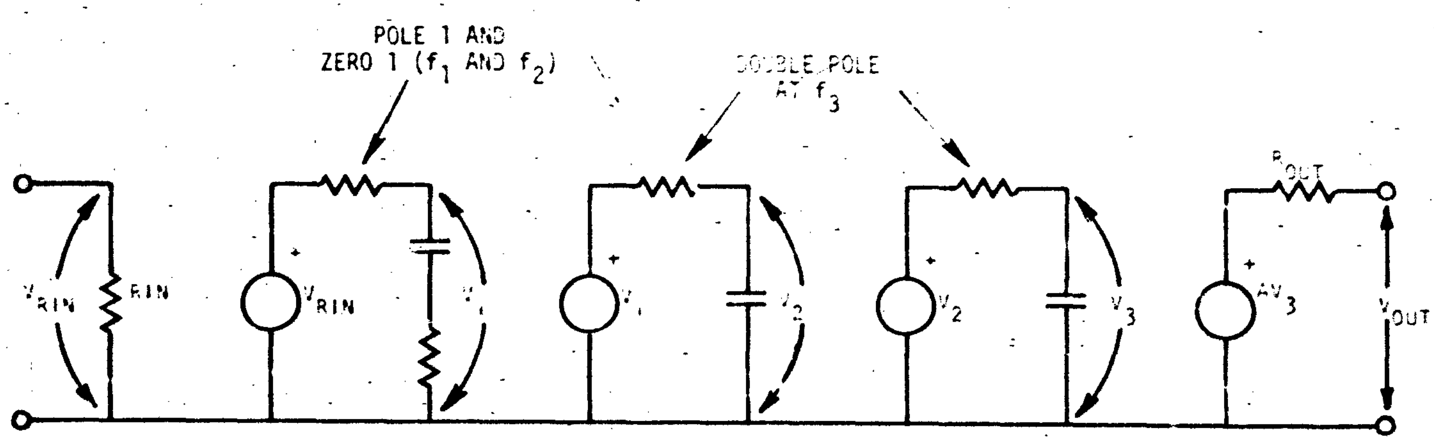


Figure VI-3. Example Amplifier with Frequency Response Network

2) Open Loop Gain

Op amp gain is defined as the change in output voltage divided by the change in the differential voltage at the input terminals for an amplifier with no external feedback applied.

3) Common Mode Rejection Ratio

CMRR is a measure of the ability of an op amp to ignore changes in the common mode voltage input. CMRR is obtained by dividing the change in common mode voltage by the change in differential input voltage required to hold the op amp output voltage constant.

4) Power Supply Rejection Ratio

PSRR is a measure of the ability of the op amp to ignore changes in the power supply voltages. PSRR is obtained by dividing the change in power supply voltage by the change in input voltage required to hold the output voltage constant.

5) Input Bias Current

Input bias current is that current flowing into either the inverting or noninverting input terminals.

6) Offset Current

The offset current is the difference between the two input bias currents.

7) Supply Current

Supply current is that current in the +V or -V supply terminals of the op amp.

8) Output Voltage Swing

The output voltage swing is the maximum amount that the output voltage may change for a given supply voltage.

b. Parameterization of μA741DC Operational Amplifier

In the following parameterization examples the measurements have been taken using a Tektronix 577 curve tracer with a 178 linear circuit tester option. This measurement tool provides a great deal more information about op amp performance than the usual linear circuit tests.

However, acceptable parameterization information can be obtained from other linear integrated circuit testers or from custom test apparatus such as described in appendix 3 of reference VI-7.

1) Offset Voltage

a) By Measurement

Offset voltage was measured by use of the Tektronix 577-178 curve tracer. The display used to determine offset voltage is illustrated in figure VI-4. The display shows the amplifier input voltage on the vertical axis and the output voltage on the horizontal axis. The offset voltage (3 mV) is the input voltage required to force the output voltage to 0.

b) From Data Sheets

The manufacturer specification sheets (figure VI-5) list a typical input offset voltage of 2 mV and a maximum input offset voltage of 6 mV.

2) Open Loop Gain

a) By Measurement

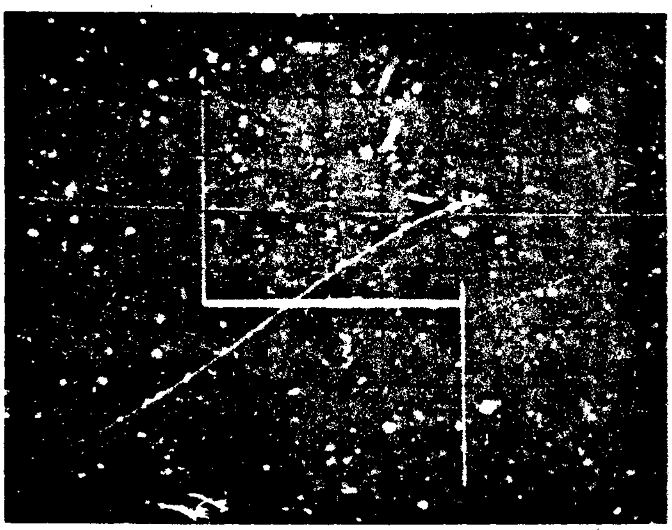
The photograph shown in figure VI-6 depicts the gain of the 741 op amp. The display shows the amplifier input voltage on the vertical axis and the output voltage on the horizontal axis with offset voltage nulled. The amplifiers' voltage gain can be seen to be fairly linear and have a value of about:

$$\frac{14\ V}{80\ \mu V} = 1.75 \times 10^5 \text{ or } 105\ dB$$

b) From Data Sheets

The manufacturer specification sheets (figure VI-5) list the typical large signal voltage gain as 200,000 and the minimum large signal voltage gain as 20,000.

A very important gain parameter is the open loop gain as a function of frequency. This is a difficult parameter to measure but is available in the data sheets (figure VI-5) in graphical form. The



VERT.
5 mV/div
HORIZ.
5 V/div

Figure VI-4. Determination of Offset Voltage

μA741

FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

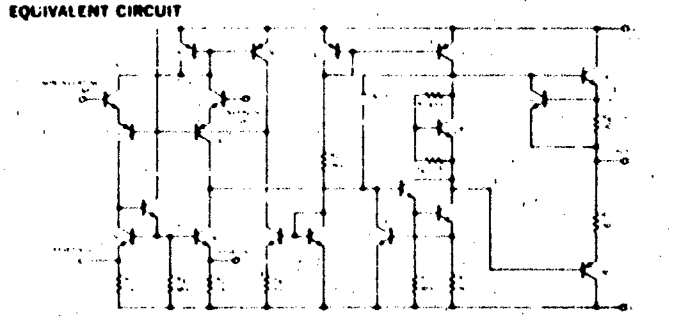
GENERAL DESCRIPTION The μA741 is a high performance monolithic Operational Amplifier constructed using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

ABSOLUTE MAXIMUM RATINGS

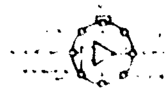
Supply Voltage	
Military (741)	±22 V
Commercial (741C)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, DIP, and Flatpak	−65°C to +150°C
Mini DIP	−55°C to +125°C
Operating Temperature Range	
Military (741)	−55°C to +125°C
Commercial (741C)	0°C to +70°C
Lead Temperature (Soldering)	
Metal Can, DIP, and Flatpak (60 seconds)	300°C
Mini DIP (10 seconds)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS

8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 5B

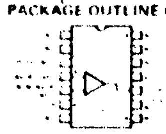


Note: Pin 4 connected to case

ORDER INFORMATION

TYPE	PART NO.
741	741HM
741C	741HC

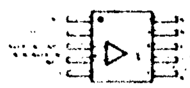
14-LEAD DIP
(TOP VIEW)
PACKAGE OUTLINE 6A



ORDER INFORMATION

TYPE	PART NO.
741	741DM
741C	741DC

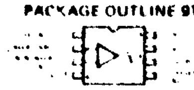
10-LEAD FLATPAK
(TOP VIEW)
PACKAGE OUTLINE 3F



ORDER INFORMATION

TYPE	PART NO.
741	741FM

8-LEAD MINIDIP
(TOP VIEW)
PACKAGE OUTLINE 9T



ORDER INFORMATION

TYPE	PART NO.
741C	741TC

Figure VI-5. Manufacturer Specification Sheets (ref. VI-8)

741C

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

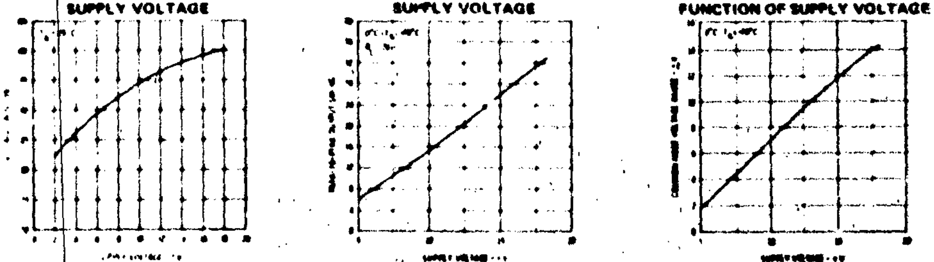
PARAMETERS (see definitions)		CONDITIONS	MIN	TYP.	MAX	UNITS
Input Offset Voltage		R_S ≤ 10 kΩ		2.0	6.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		R_S ≤ 10 kΩ	70	90		dB
Supply Voltage Rejection Ratio		R_S ≤ 10 kΩ		30	150	μV/V
Large Signal Voltage Gain		R_L ≥ 2 kΩ, V_{OUT} = ±10 V	20,000	200,000		
Output Voltage Swing		R_L ≥ 10 kΩ	±12	±14		V
		R_L ≥ 2 kΩ	±10	±13		V
Output Resistance				75		Ω
Output Short Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (Unity Gain)	Risetime	V_{IN} = 20 mV, R_L = 2 kΩ, C_L ≤ 100 pF		0.3		μs
	Overshoot			5.0		%
Slew Rate		R_L ≥ 2 kΩ		0.5		V/μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C						
Input Offset Voltage					7.5	mV
Input Offset Current					300	nA
Input Bias Current					800	nA
Large Signal Voltage Gain		R_L ≥ 2 kΩ, V_{OUT} = ±10 V	15,000			
Output Voltage Swing		R_L ≥ 2 kΩ	±10	±13		V

TYPICAL PERFORMANCE CURVES FOR 741C

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



NOTES

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the DIP, 5.6 mW/°C for the Mini DIP and 7.1 mW/°C for the Flatpak.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.

Figure VI-5. Manufacturer Specification Sheets (Continued)

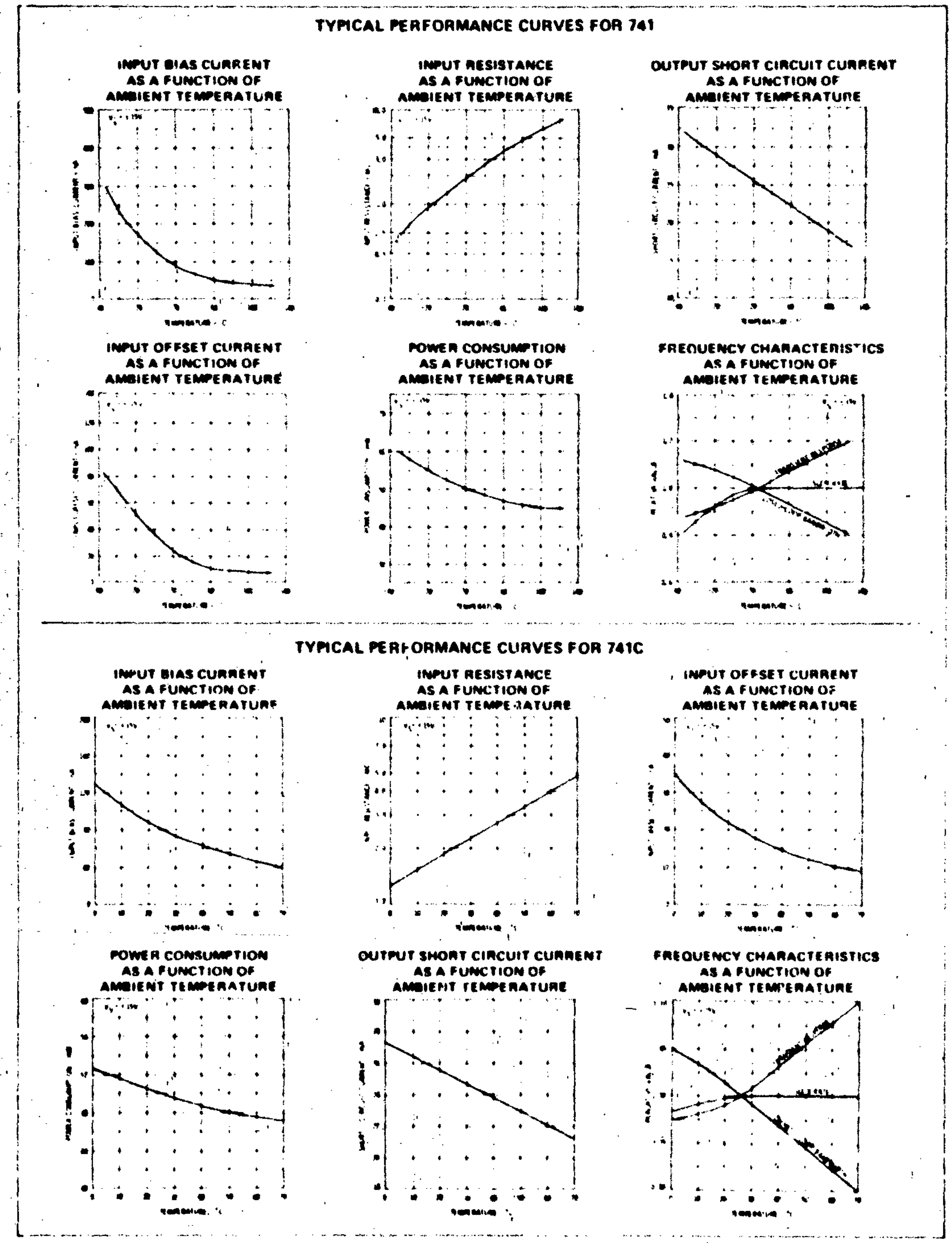


Figure VI-5. Manufacturer Specification Sheets (Continued)

741

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

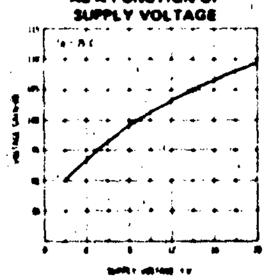
PARAMETERS (see definitions)		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current				20	200	nA
Input Bias Current				30	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				1.4		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	50,000	200,000		
Output Resistance				75		Ω
Output Short Circuit Current				25		mA
Supply Current				1.7	2.8	mA
Power Consumption				50	[illegible]	mW
Transient Response (Unity Gain)	Risetime	$V_{IN} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate		$R_L \geq 2$ kΩ		0.5		V/μs

The following specifications apply for $-55°C \leq T_A \leq +125°C$

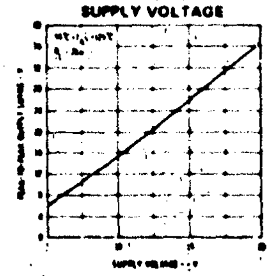
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current	$T_A = +125°C$		7.0	200	nA
	$T_A = -55°C$		85	500	nA
Input Bias Current	$T_A = +125°C$		0.03	0.5	μA
	$T_A = -55°C$		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	[illegible]	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current	$T_A = +125°C$		1.5	2.5	mA
	$T_A = -55°C$		2.0	3.3	mA
Power Consumption	$T_A = +125°C$		45	75	mW
	$T_A = -55°C$		60	100	mW

TYPICAL PERFORMANCE CURVES FOR 741

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

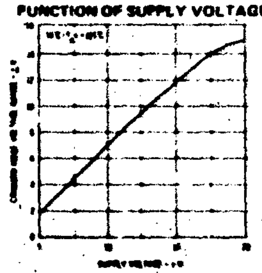


Figure VI-5. Manufacturer Specification Sheets (Continued)

FAIRCHILD LINEAR INTEGRATED CIRCUITS • μA741

TYPICAL PERFORMANCE CURVES FOR 741 AND 741C (Cont'd)

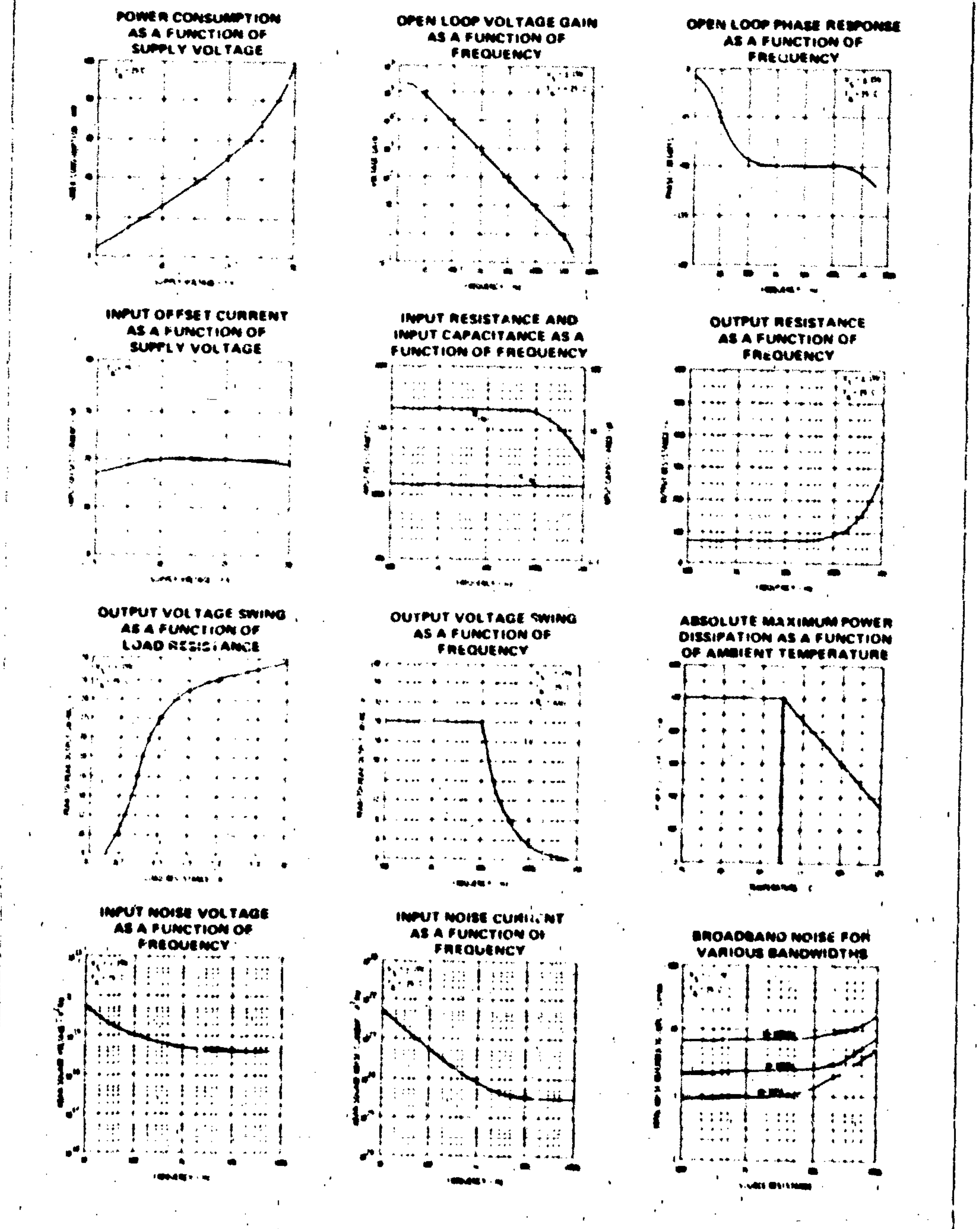
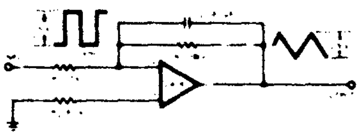


Figure VI-5. Manufacturer Specification Sheets (Continued)

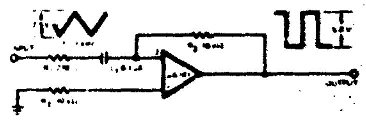
TYPICAL APPLICATIONS (Cont'd)

SIMPLE INTEGRATOR



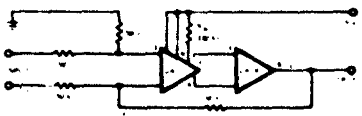
$E_{OUT} = -\frac{1}{R_1C_1}\int E_{IN}\,dt$

SIMPLE DIFFERENTIATOR



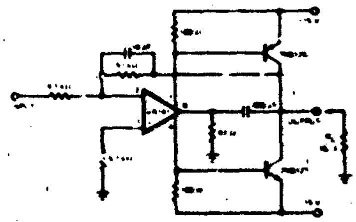
$E_{OUT} = -R_2C_1\frac{dE_{IN}}{dt}$

LOW DRIFT LOW NOISE AMPLIFIER

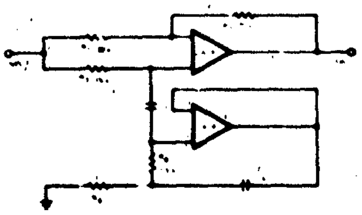


Voltage Gain = 10^3
Input Offset Voltage Drift = 0.6 μV/°C
Input Offset Current Drift = 2.0 pA/°C

HIGH SLEW RATE POWER AMPLIFIER



NOTCH FILTER USING THE μA741 AS A GYRATOR



Trim R such that
R R
R 2 R

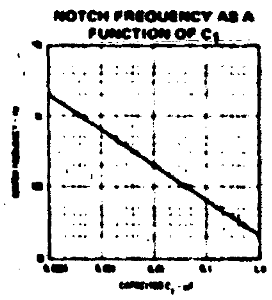
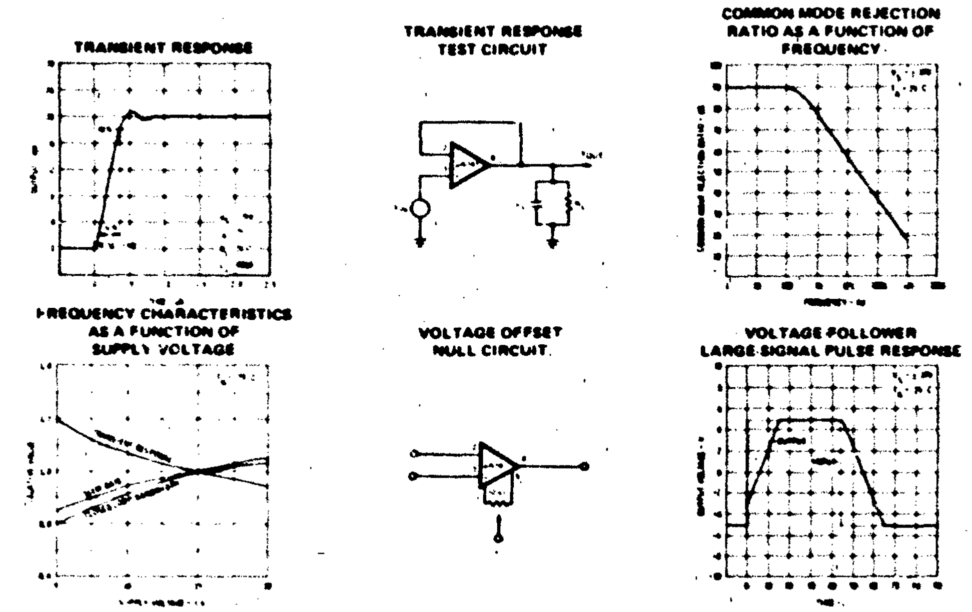
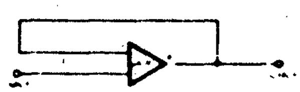


Figure VI-5. Manufacturer Specification Sheets (Continued)



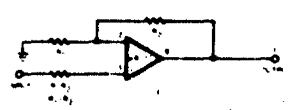
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



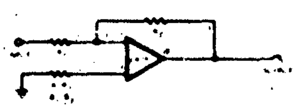
R_{IN} = 400 MΩ
C_{IN} = 1 pF
R_{OUT} < 1 Ω
BW = 1 MHz

NON-INVERTING AMPLIFIER



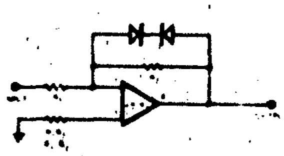
GAIN	R_1	R_2	BW	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R_1	R_2	BW	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

CLIPPING AMPLIFIER



$$\frac{e_{OUT}}{e_{IN}} = \frac{R_2}{R_1} \text{ if } |e_{OUT}| \leq V_Z + 0.7\text{ V}$$

where V_Z = Zener breakdown voltage

Figure VI-5. Manufacturer Specification Sheets (Concluded)

VERT:
50 [illegible]V/div
HORIZ:
5V/div

Figure VI-6. Determination of 741PC Gain

desired plot is "open loop voltage gain as function of frequency." Information from this plot is necessary to model the frequency characteristics of the amplifier.

3) Common Mode Rejection Ratio

a) From Measurement

The CMRR can be determined from the curve tracer photograph shown in figure VI-7. The vertical axis displays the change in input voltage between the input terminals. The horizontal deflection is the common mode voltage. The output of the op amp is held at zero volts. The CMRR is the change in common mode voltage (horizontal) divided by the change in input voltage (vertical). CMRR for this particular μ741 op amp can be seen to be about:

$$\text{CMRR} = \frac{16\ \text{V}}{0.4\ \text{mV}} = 4 \times 10^4 = 92\ \text{dB}$$

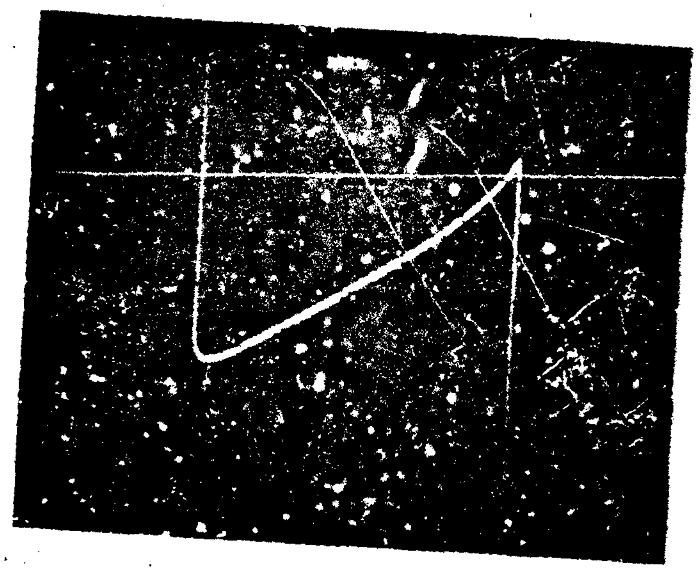
b) From Data Sheets

The manufacturer specification sheets shown in figure VI-5 yield a typical CMRR of 90 dB and a minimum CMRR of 70 dB.

4) Power Supply Rejection Ratio

a) From Measurement

Three measurements of PSRR may be made. PSRR can be measured from variations in the positive power supply (+PSRR), for variations in the negative power supply (-PSRR), or for variations in both power supplys (±PSRR). For all PSRR displays, the horizontal deflection is the power supply voltage. The vertical deflection is the change in the op amp input voltage with the output held at zero. The displays for +PSRR, -PSRR, and ±PSRR are given in figures VI-8, VI-9, and VI-10, respectively. Since +PSRR represents the dominant PSRR it will be modeled. PSRR is the change in power supply voltage (horizontal) divided by the change in input voltage.

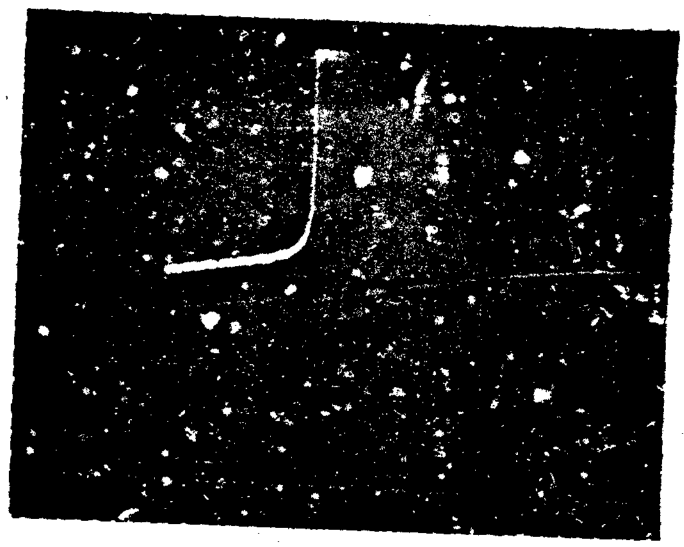


VERT:
0.2 mV/div
HORIZ:
5 V/div

Figure VI-7. Determination of CMRR.

VERT:
0.1 mV/div
HORIZ:
5 V/div

Figure VI-8. +PSRR



VERT:
0.1 mV/div
HORIZ:
5 V/div

Figure VI-9. -PSRR

VERT:
0.1 mV/div
HORIZ:
5 V/div

Figure VI-10. ±PSRR

$$+PSRR = \frac{10\ V}{0.3\ mV} = 3.33 \times 10^4 = 90\ dB$$

b) From Data Sheets

The manufacturer specification sheets (figure VI-5) list typical PSRR as:

$$\frac{1}{30\ \mu V/V} \approx 3.33 \times 10^4$$

and the maximum PSRR as:

$$\frac{1}{150\ \mu V/V} = 6.67 \times 10^3$$

5) Input Currents

a) From Measurement

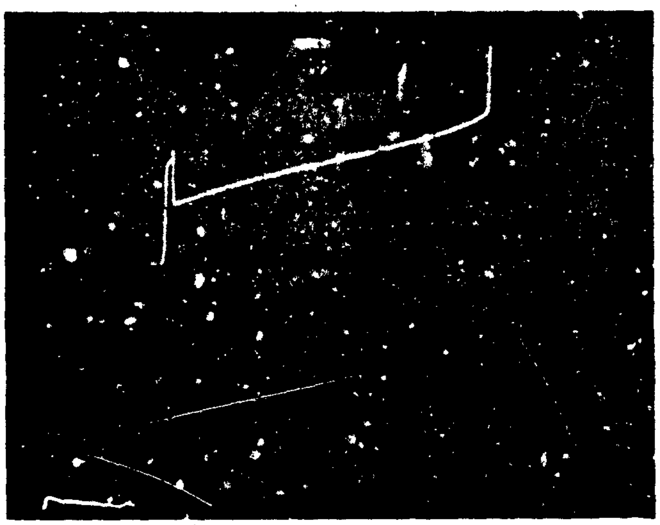
The Tektronix 577-1/8 displays input bias current of the op amp (vertical) as a function of common mode voltage (horizontal). Figure VI-11 yields the input current into the noninverting input and figure VI-12 yields the input current into the inverting input. At zero input voltage, both input currents are about 17 nA. The slopes of the input current lines suggest a linear resistance of about:

$$R_{IN} = \frac{15\ V}{8\ nA} = 1.875 \times 10^9\ ohms$$

Offset current may be obtained from the photograph shown in figure VI-13 which displays both input currents on an expanded scale with no zero reference voltage. The offset current is the vertical distance between the two traces or about 1.2 nA.

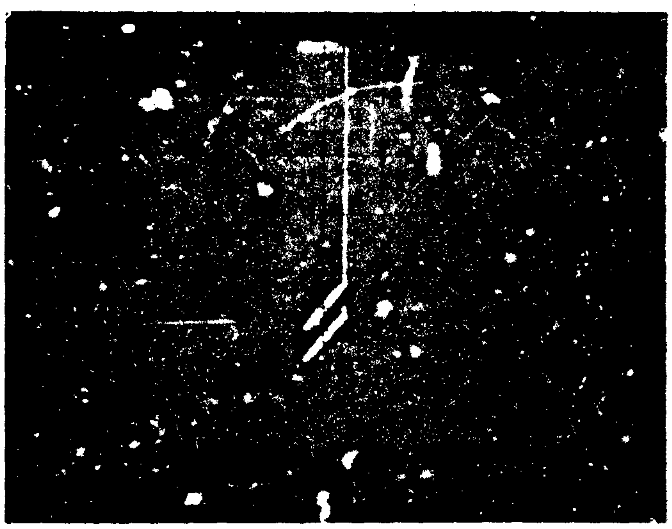
VERT:
10 nA/div
HORIZ:
5 V/div

Figure VI-11. Input Current into Noninverting Input



VERT:
10 nA/div
HORIZ:
5 V/div

Figure VI-12. Input Current of Inverting Input



VERT:
2 nA/div
HORIZ:
5 V/div

Figure VI-13. Measuring Offset Current (Inverting Input is Represented by Upper Trace)

b) From Data Sneets

The manufacturer specification sheets (figure VI-5) list input bias current as having a typical value of 80 nA and a maximum value of 500 nA. Input offset current has a typical value of 20 nA, and input resistance has a typical value of 2 megohms.

6) Supply Currents

a) From Measurements

Power supply current as a function power supply voltage for the + and - supply can be obtained from the photograph shown in figure VI-14. The trace suggests a resistance of

$$\frac{15\ V}{1.5\ mA} = 1 \times 10^4 \text{ ohms}$$

Supply current as a function of output voltage is demonstrated in the photograph shown in figure VI-15. This characteristic and supply current as a function of load were not chosen as aspects to be modeled.

b) From Data Sheets

The manufacturer specification sheets (figure VI-5) list a typical supply current of 1.7 mA.

7) Input Capacitance

The manufacturer specification sheets (figure VI-5) list a typical input capacitance of 1.4 pF.

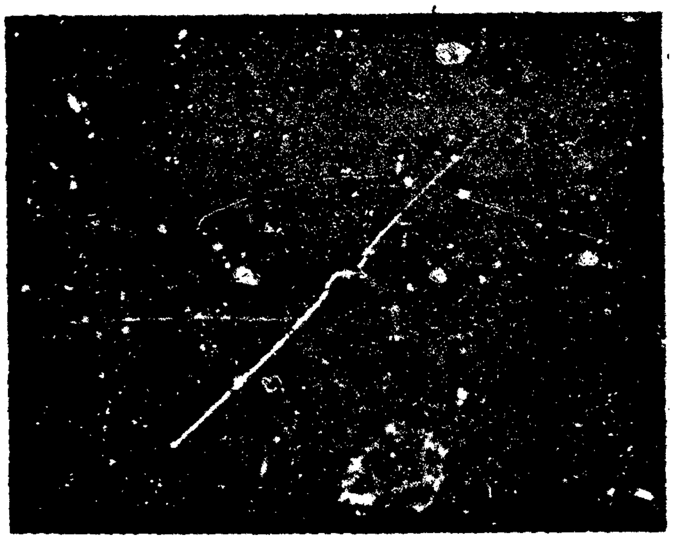
8) Output Resistance

The manufacturer specification sheets (figure VI-5) list a typical output resistance of 75 ohms.

9) Output Voltage Swing

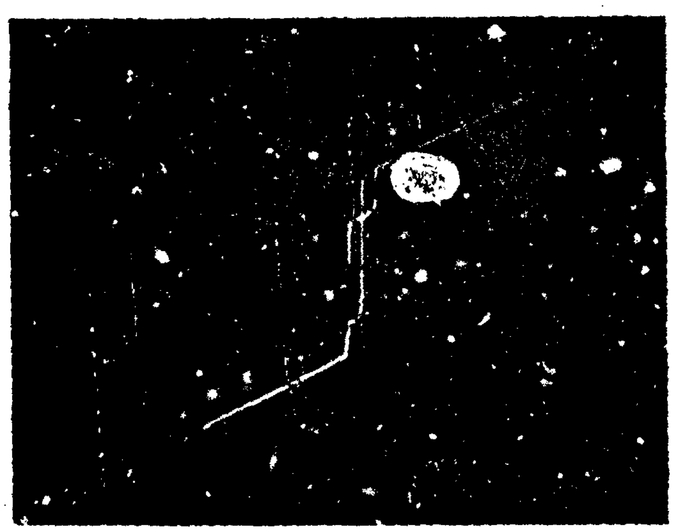
a) From Measurement

The output voltage limits for a supply voltage of ±15 volts can be obtained from the gain display shown in figure VI-6. It can be seen from this photograph that output voltage may swing from 14 volts



VERT:
0.5 mA/div
HORIZ:
5 V/div

Figure VI-14. Power Supply Current as a Function of Supply Voltage



VERT:
0.5 mA/div
HORIZ:
5 V/div

Figure VI-15. Supply Current as a Function of Output Voltage

to -12.5 volts. Therefore, it will be assumed that the output voltage can swing to within 1 volt of the + power supply and to within 2.5 volts of the - power supply.

b) From Data Sheets

An indication of how far voltage may swing for any supply voltage is given by the "output voltage swing as a function of supply voltage" plot in the manufacturer specification sheets. This plot indicates that the voltage swing is always about 4 volts less than the sum of the two power supply voltages.

10) Slew Rate

Slew rate is given in figure VI-5 as 0.5 volts per microsecond. Slew rate can be measured by setting up the op amp in an amplifier configuration, applying a large, fast rise pulse and measuring the response rate (in volts per microsecond) of the amplifier output using an oscilloscope.

c. Development of Model of μA741DC

1) Inclusion of Offset Voltage

Offset voltage may be included in the model by placing a voltage source in one of the input leads. The value of the voltage source is equal to the offset voltage and its polarity should be such as to produce the effects displayed in figure VI-4. The inclusion of offset voltage is illustrated in figure VI-16.

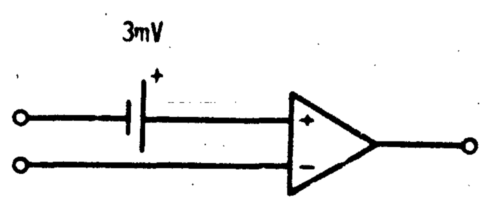


Figure VI-16. Inclusion of Offset Voltage

2) Inclusion of dc Gain

dc open loop gain can be included as a voltage controlled voltage source as illustrated in figure VI-17.

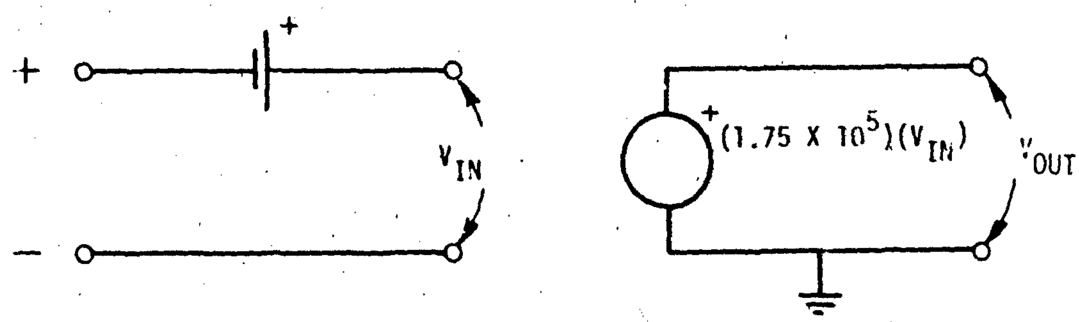


Figure VI-17. Ideal Gain Characteristic

3) Frequency Response of Gain

The frequency shaping network can be developed from the plot of "open loop voltage gain as a function of frequency" in figure VI-5. From this plot it can be seen that a pole exists at about 3 Hz and another at about 1 MHz. This characteristic can be simulated through a double application of network A of figure VI-2.

To model the first pole at 3 Hz, choose R_A = 5K.

Then,

$$3 \text{ Hz} = \frac{1}{2\pi(5 \times 10^3\ \Omega)(C_A)}$$

$$C_A = 1.06 \times 10^{-5} \text{ farads}$$

To model the second pole at 1 MHz, choose R_A = 5 kΩ.

Then,

$$1 \text{ MHz} = \frac{1}{2\pi\ (5 \times 10^3\ \Omega)\ (C_A')}$$

$$C_A' = 3.18 \times 10^{-11} \text{ farads}$$

The composite frequency shaping network can now be included into the model, taking care not to load individual stages as illustrated in figure VI-18.

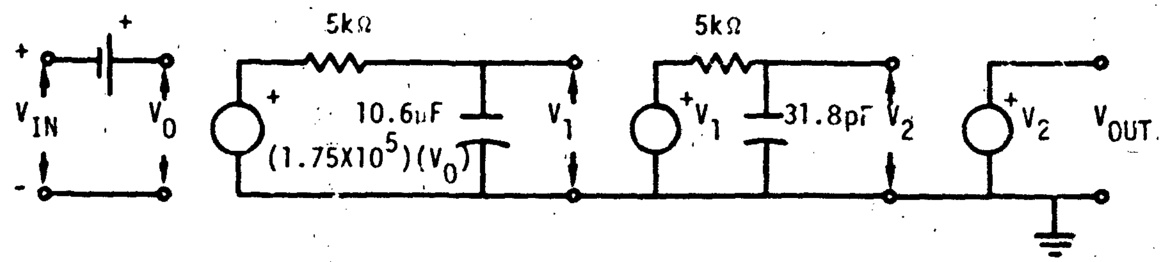


Figure VI-18. Op Amp With Frequency Shaping Network

4) Common Mode Rejection Ratio

CMRR can be modeled by modifying the offset voltage source. The modification is such as to add a voltage dependent voltage term to the source which will produce the results observed in figure VI-7. The additional term will be 0.4 mV for every 16 volts applied to the noninverting input. The input stage can now be represented as shown in figure VI-19.

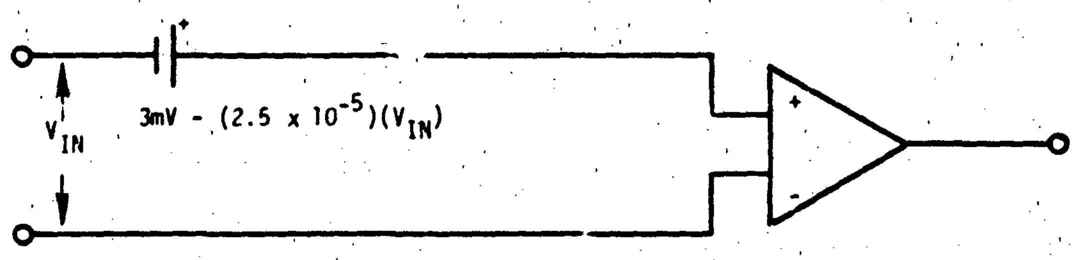


Figure VI-19. Modeling CMRR

5) <u>Power Supply Rejection Ratio</u>

PSRR may be modeled by adding a third term to the offset voltage source. Since +PSRR was determined to be the dominant component, a voltage increase of 0.3 mV for every 10 volts decrease in + power supply must be represented at the input as illustrated in figure VI-20.

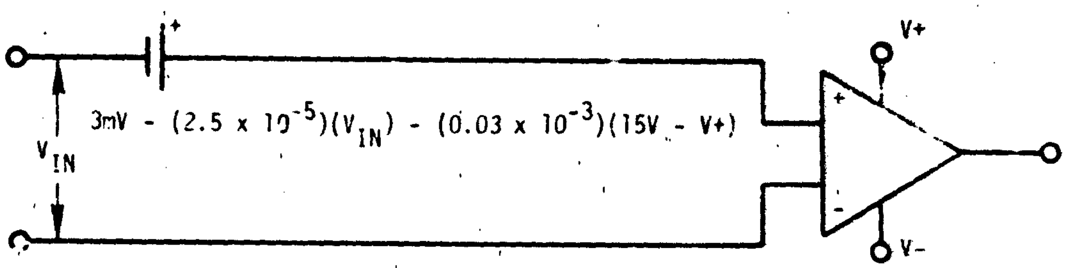


Figure VI-20. Modeling PSRR

6) <u>Input Bias Current</u>

The input bias currents may be represented by a constant current source of 17 nA in parallel with a resistor of value equal to 1.88×10^9 ohms. This is illustrated in figure VI-21.

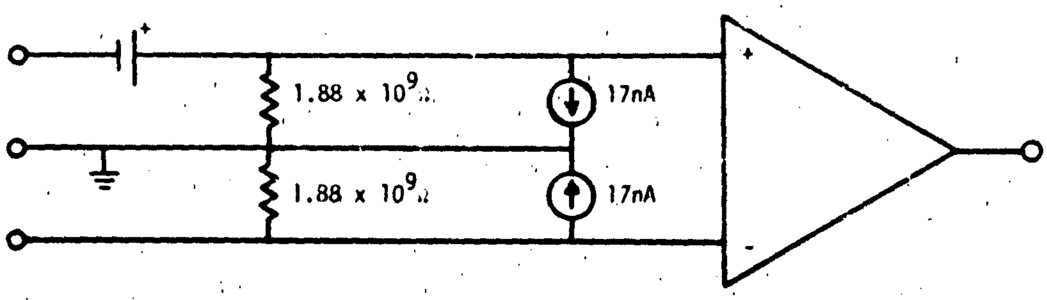


Figure VI-21. Addition of Input Bias Effects

7) Offset Current

Offset current is modeled by simply unbalancing the two constant current sources by the magnitude of the offset current. This is achieved by increasing the value of the current generator associated with the inverting input to 18.2 nA.

8) Supply Current

Supply current as a function of supply voltage may be modeled by two shunt resistors of value 10 kilohms. Supply current as a function of output voltage will not be modeled. The power supply current equivalent circuit is shown in figure VI-22.

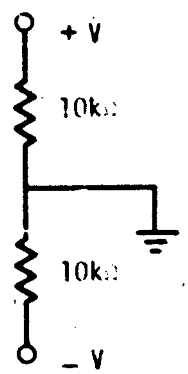


Figure VI-22. Modeling Power Supply Current

9) C_{IN}, R_{OUT}

The input capacitance should be placed across the inputs to ground. R_{OUT} will be placed in the output lead.

10) Output Voltage Swings

The output voltage will be limited through a logical function to a voltage 1 volt less than a V+ and 2.5 volts greater than V-. This can cause computation problems. A table or analytic function may be preferable.

11) Slew Rate

Slew rate is modeled by limiting the rate at which the 10.6 μF frequency response capacitor of the model could charge. This may be achieved by converting the 5 kΩ charging resistor to a nonlinear

voltage dependent current source. This current source will behave like a 5 kΩ resistor if output is not slew rate limited. If the output is slew rate limited, the current source will saturate to a constant value.

The following rules determine if the output response is slew rate limited:

(1) If the differential input voltage times the gain-bandwidth product is less than the slew rate the response is bandwidth limited.

(2) If the differential input voltage times the gain-bandwidth product is greater than the slew rate the output is slew rate-limited (see reference VI-9).

The gain-bandwidth product is the product of the dc gain times the 3-dB bandwidth (in radians) of the amplifier.

For the 741DC:

$$GB = (1.75 \times 10^5)(3\ \text{Hz})(2\pi) = 3.3 \times 10^6 \text{ radians/s}$$

The input step voltage at the boundary between slew or network dominated response is:

$$V = \frac{0.5\ \text{V}}{\mu\text{s}} \times \frac{\text{sec}}{3.3 \times 10^6 \text{ radians}} = 0.152\ \text{V}$$

The voltage breakpoint of the nonlinear current source is:

$$\pm\,(1.75 \times 10^5)(0.152\ \text{V}) = 2.66 \times 10^4\ \text{V}$$

The saturated current value of the dependent current source is:

$$I_{sat} = \frac{(0.5\ \text{V})(10.6\ \mu\text{F})}{1\ \mu\text{s}} = 5.3 \text{ amperes}$$

Thus the characteristic of the current source is shown in figure VI-23.

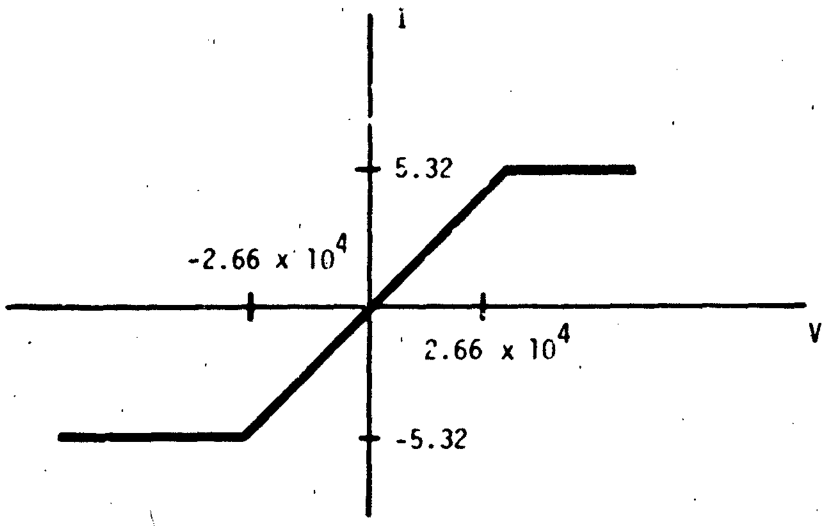


Figure VI-23. Conversion of 5 kΩ Resistor to Include Slew Limiting

12) Complete Electrical Model

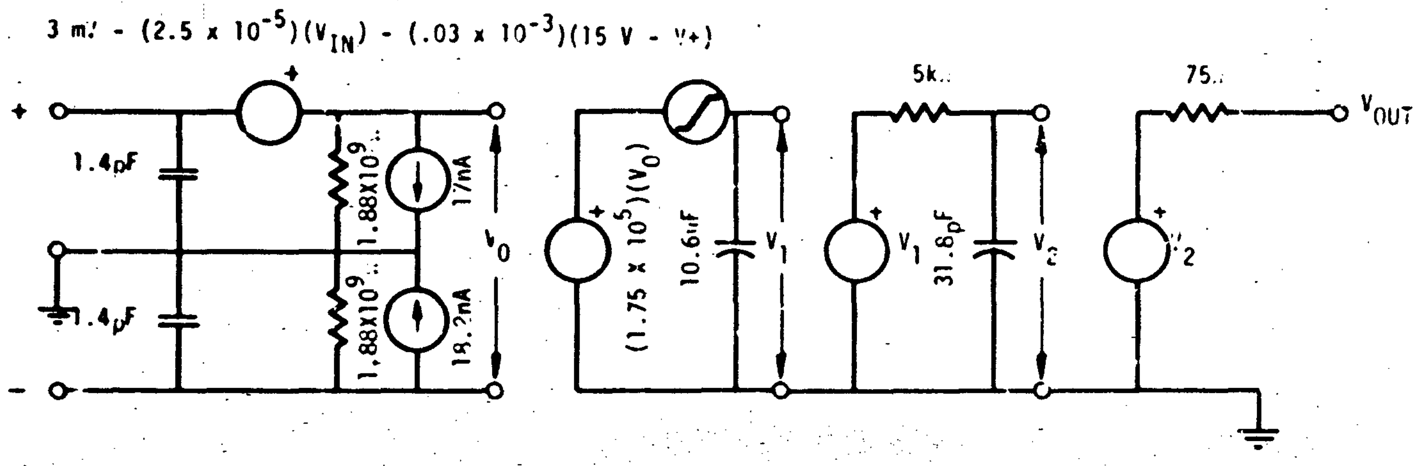
The completed electrical model of the μA741DC is illustrated in figure VI-24.

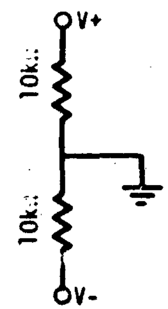
4. Computer Example

To demonstrate the behavior of the model μA741DC, the model was put through two verifying tests. One test involved the op amp configured in a unity-gain arrangement with an input voltage source which is overdriving the amplifier (overdriving would be one possible EMP transient upset effect). The other test has a high frequency voltage source driving the op amp in an open loop configuration. The decline in open loop gain was compared to the manufacturer specification sheets. SCEPTRE was used to test the models.

The first test consisted of the circuit shown in figure VI-25. The second test arrangement is illustrated in figure VI-26. For both tests, the output voltage of the op amp was monitored as a function of time.

The SCEPTRE input listing for test 1 is given in figure VI-27. The SCEPTRE output is shown in figure VI-28. A clipped sine wave is clearly visible. Removing the voltage limiting subroutine in the model





IF $V_{OUT} > V(+) - 1V$

THEN $V_{OUT} = V(+) - 1V$

IF $V_{OUT} < V(-) + 2.5V$

THEN $V_{OUT} = V(-) + 2.5V$

Figure VI-24. Completed Electrical Mode

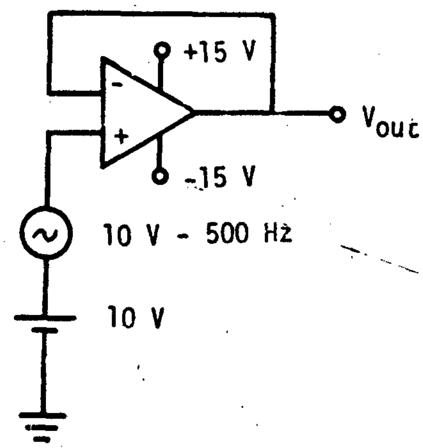


Figure VI-25. μA741 Test Circuit

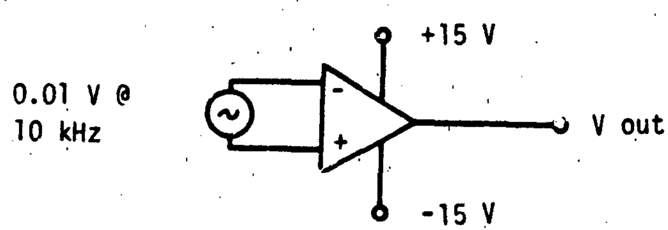


Figure VI-26. Test 2

```
SUBPROGRAM
       FUNCTION FOUT(VO,VP,VN)
       FOUT=VO
       VSP=VP-1.0
       VSN=2.5-VN
       IF (VO.GT.VSP) FOUT=VSP
       IF (VO.LT.VSN) FOUT=VSN
       IF (VO.GT.VSP.AND.VO.LT.VSN) FOUT=0
       RETURN
       END
CIRCUIT DESCRIPTION
ELEMENTS
RSS,1-0=10.E3
RPSS,0-2=10.E3
CINP,3-0=1.4E-12
CINN,0-4=1.4E-12
JIN,3-4=0
EINP,3-5=X1(3.E-3-2.5E-5*VJIN-30.E-6*(15.-VRSS))
RINP,5-0=1.88E9
RINN,0-4=1.88E9
JOFP,5-0=17.E-9
JOFN,4-0=18.2E-9
J0,5-4=0
E0,0-6=X2(1.75E5*VJ0)
R1,6-7=5.E3
C1,7-0=10.6E-6
E1,0-8=X3(VC1)
R2,8-9=5.E3
C2,9-0=31.8E-12
ROUT,10-11=75
EOUT,0-10=FOUT(VC2,VRSS,VRPSS)
EPPS,0-1=15
ENPS,2-0=15
JOUT,11-0=0
EINPUT,3-X=X4(.01*(SIN(6.28E4*TIME)))
RIN,X-4=50.
FUNCTIONS
OUTPUTS
VJOUT,PLOT
RUN CONTROLS
STOP TIME=5.E-4
END
```

Figure VI-27. Test 1 Input

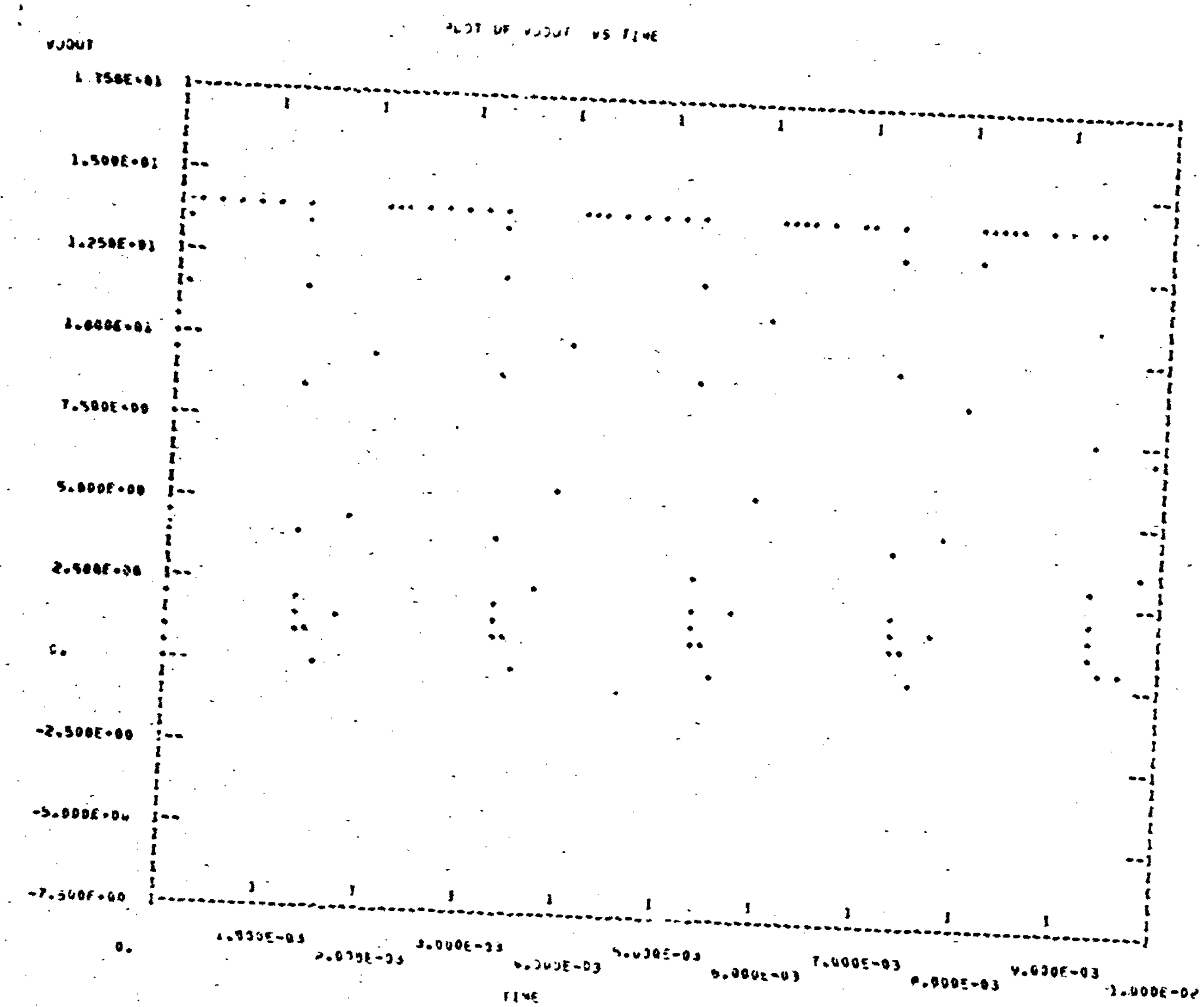


Figure VI-28. μA741 Output Voltage

will produce the output of figure VI-29. This plot demonstrates that the feedback loop did indeed produce unity gain, as required.

The SCEPTRE input listing for test 2 is given in figure VI-30. The SCEPTRE output for test 2 is shown in figure VI-31. The peak voltage swing of the output sine wave is desired. This can be seen to be just under a volt. Dividing output voltage by input voltage (0.01 volt) yields a voltage gain of about 100 at 10 kHz. The manufacturer specification sheets (Open Loop Voltage Gain as a Function of Frequency) indicate that gain is 100 at 10 kHz.

The ramping of the dc level in figure VI-31 is due to the effects of offset voltage and current in the open-loop analysis of the op amp. Such an instability would be expected if the same test were to be performed on a real device. The ability to see the behavior of the amplifier before it reaches saturation in about 1 ms is an example of the power which computer-aided modeling allows the analyst.

5. Radiation Effects

a. Photoresponse

Under ionizing radiation, photocurrents will act to alter the biases and saturate op-amp stages. Output voltage will become somewhat independent of the input voltage levels.

Experimental data are required to describe the transient behavior of the operational amplifier. This behavior may then be included as part of the model. Experimental data for the 741 indicates that at levels above 1×10^8 rads(si)/sec, the output voltage will rise at a rapid rate determined by the radiation response of the output stages of the operational amplifier. The output will then saturate for some time period. After the radiation pulse, the amplifier will come out of saturation and recover at the slew rate of the amplifier.

The photoresponse was modeled by the current generator, IRAD, as illustrated in figure VI-32. IRAD charges the dominant pole capacitor, C1, faster than the slew rate limited current source, J1, can discharge the capacitor. The result is a change in output voltage sensed as an error. In summary, to model the transient behavior of an operational

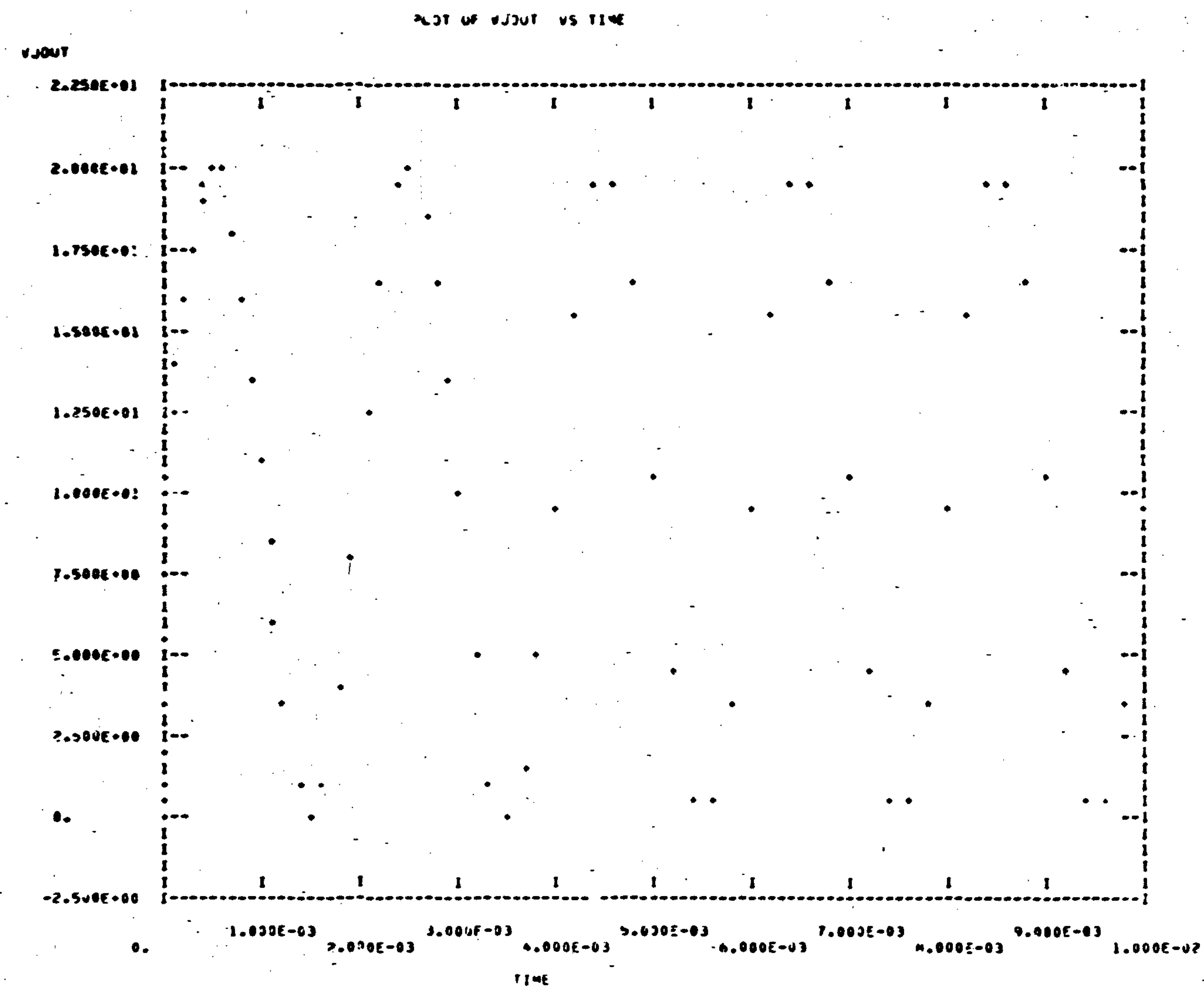


Figure VI-29. Unity Gain Ampli⁻.er

```
SUBPROGRAM
      FUNCTION FOUT(V0,VP,VN)
      FOUT=V0
      VSP=VP-1.0
      VSN=2.5-VN
      IF (V0.GT.VSP) FOUT=VSP
      IF (V0.LT.VSN) FOUT=VSN
      IF (V0.GT.VSP.AND.V0.LT.VSN) FOUT=0
      RETURN
      END
CIRCUIT DESCRIPTION
ELEMENTS
RSS,1-0=10.E3
RPSS,0-2=10.E3
CINP,3-0=1.4E-12
CINN,0-4=1.4E-12
JIN,3-4=0
EINP,3-5=X1(3.E-3-2.5E-5*VJIN-30.E-6*(15.-VRSS))
RINP,5-0=1.88E9
RINN,0-4=1.88E9
JOFP,5-0=17.E-9
JOFN,4-0=18.2E-9
J0,5-4=0
E0,0-6=X2(1.75E5*VJ0)
R1,6-7=5.E3
C1,7-0=10.6E-6
E1,0-8=X3(VC1)
R2,8-9=5.E3
C2,9-0=31.8E-12
ROUT,10-11=75
EOUT,0-10=FOUT(VC2,VRSS,VRPSS)
EPPS,0-1=15
ENPS,2-0=15
JOUT,11-0=0
RB1,11-4=.001
RB2,X-3=50.
EINPUT,0-X=X4(10.*(SIN(TIME*3.14E3))+10.)
FUNCTIONS
OUTPUTS
VJOUT,PLOT
RUN CONTROLS
STOP TIME=1.E-2
END
```

Figure VI-30. Test 2 Input

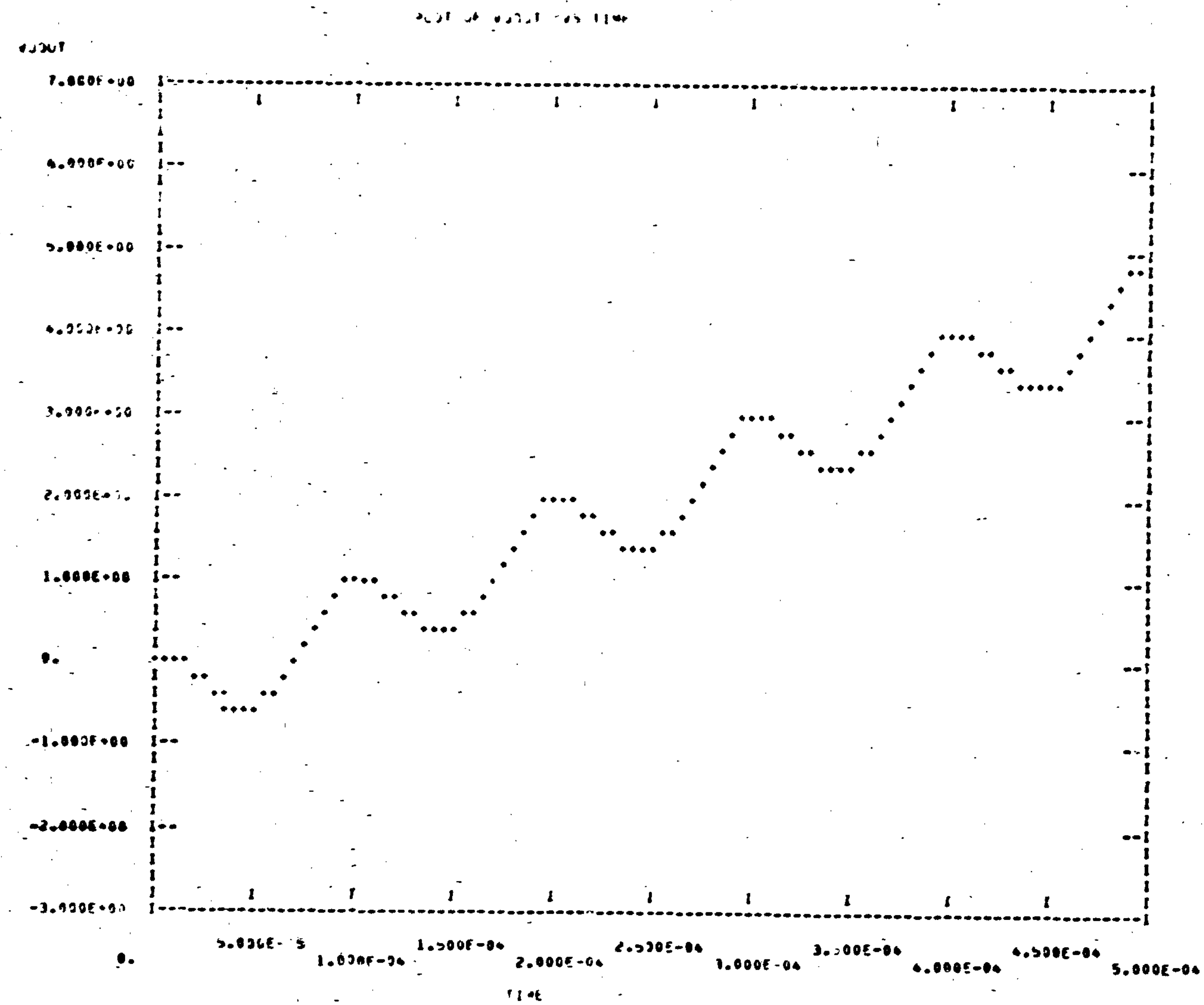
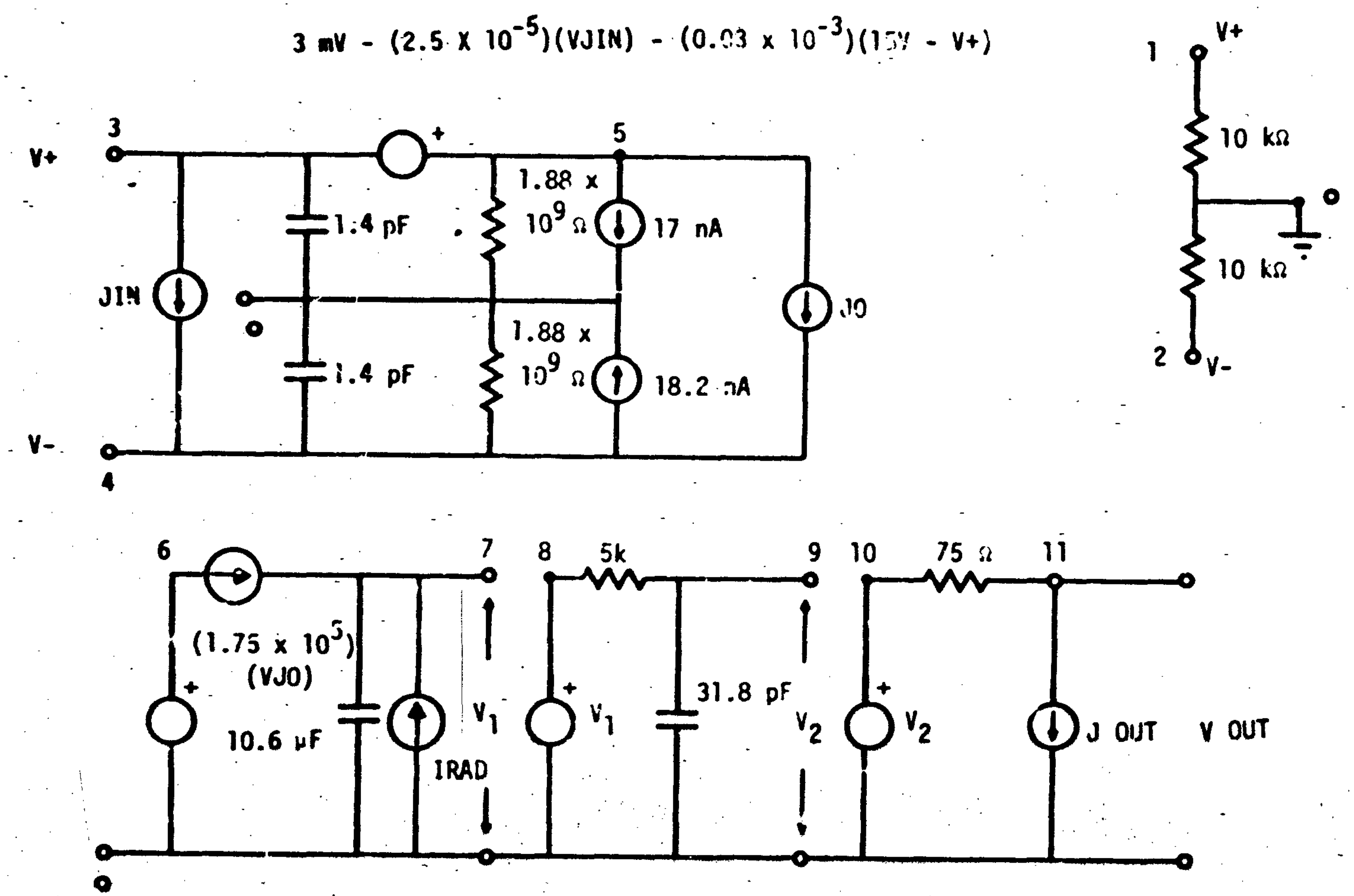


Figure VI-31. µA741 Frequency Response Test



IF V out > V(+)-1.0V, THEN Vout = V(+)-1V

IF V out < V(-)+2.5V, THEN Vout = V(-)+2.5V

Figure VI-32. Model μA741 with Photoresponse

amplifier, a method must be found to disable the ideal behavior of the amplifier to allow the output voltage to change independently of the input voltage. Manipulations of IRAD will produce the risetimes, saturation times, and falltimes required by the experimental data.

When a differential input voltage of over 0.152 V is applied across the op amp model input terminal, current source J1 saturates at 5.3 amps to model the slew rate. The transient rise rate of the op amp can therefore be defined by:

$$\frac{dV}{dt} = \frac{IRAD - 5.3A}{10.6\ \mu F}$$

Thus, the magnitude of IRAD will determine the rate of rise of the amplifier during an ionizing radiation pulse. By defining dv/dt as the experimentally determined transient rise rate, IRAD can be quantified.

When the output tries to rise above 15 V, saturation is simulated. The time in saturation can be controlled by proper definition of the IRAD pulse width. After IRAD is set to zero, the output will begin to recover at the slew rate as desired. For the 741DC, this is 0.5 V/μs. The output will remain in saturation until the voltage on C1 drops below 15 V. The output will then recover at the slew rate until normal operation is restored. Figure VI-33 shows the relationship of the IRAD current, the voltage on the capacitor, and the output voltage.

b. Burnout

Burnout may be simulated by placing a power monitoring element across the sensitive terminals. This element must be included in a manner such that circuit operation will not be affected until an overstress waveform is initiated. The power dissipated by the power sensing elements may then be monitored by the methods discussed for diodes in chapter II and burnout predicted. Due to the multiple current paths that can be produced by an overstress pulse, the Wunsch expression may not be valid for integrated circuits, and a form $P(FAIL) = At^{-B}$ where A and B

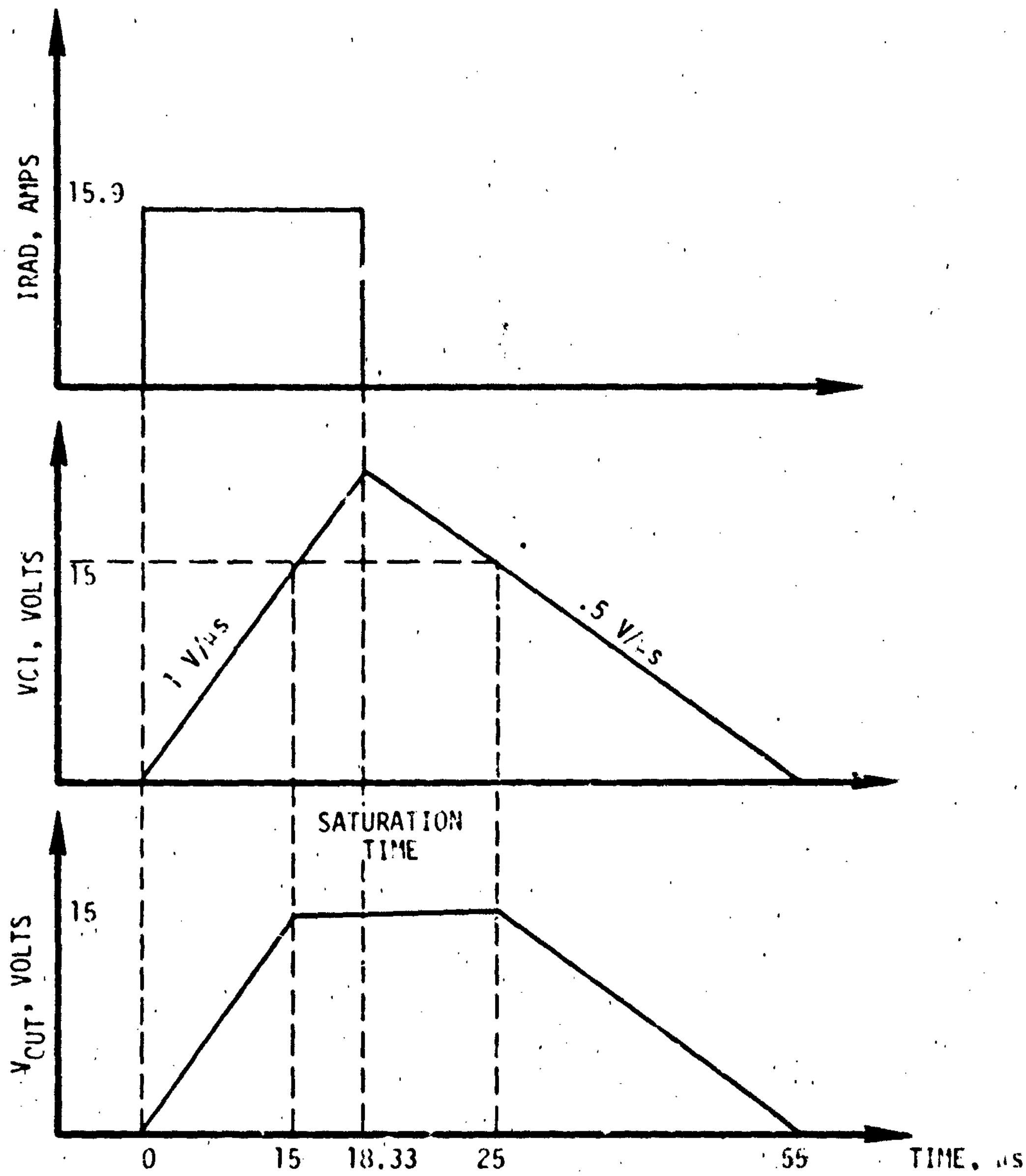


Figure VI-33. Photoresponse Simulation

are experimental constants may be more applicable. An example of a power sensing element and its placement across a circuit input is shown in figure VI-34.

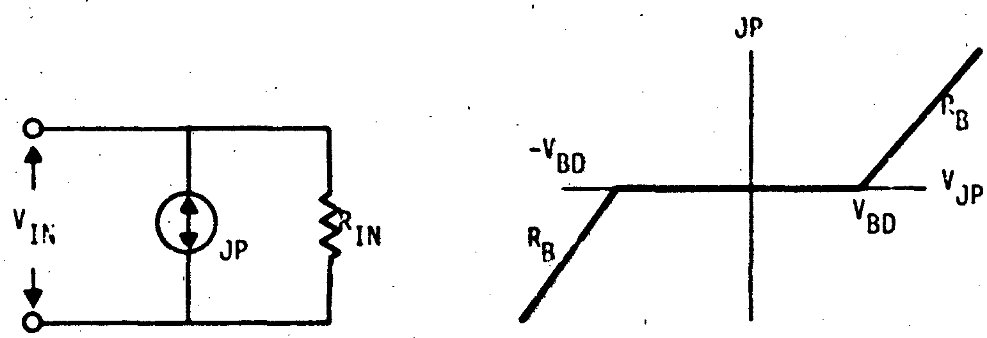


Figure VI-34. Use of Power Sensing Element

The current and voltage characteristics of the device subjected to an overstress are modeled by the breakdown voltage and resistance terms included in the power sensing element. This element then has no affect on normal electrical operation but simulates the correct current and voltage characteristics in breakdown.

Values for A, B, V_{BD}, and R_B may be determined experimentally by overstress testing sample devices to failure. Approximate values for these quantities may also be obtained from reference VI-10 for many integrated circuit technologies.

c. Neutron and Total Dose Effects

The effects of neutrons and total ionizing dose are to degrade various parameters of the integrated circuit. For instance, neutrons will primarily decrease open loop gain, increase bias current, increase offset current, and increase offset voltage while total ionizing dose will usually increase bias currents and offset current. Experimental data of parameter changes at given fluences and doses can be reflected in

the model by simply changing the appropriate parameter. Simulations with the new parameters will then indicate whether the parameter degradations lead to system failure.

C. SIMPLIFIED MODELING OF DIGITAL CIRCUITS AND SYSTEMS

1. Introduction to Simplified Digital Modeling

The goal of simplified digital modeling is to correctly simulate the terminal characteristics of a digital integrated circuit as a function of time and various stimuli including radiation. In general, the modeling is done without direct consideration of the physical processes involved. Correct simulation involves modeling the terminal current and voltage characteristics, the correct logic functioning of the device, the timing characteristics such as propagation delay of logic signals and the effects of radiation on these.

Modeling of the terminal current and voltage characteristics usually involves the current characteristics as a function of voltage for the input terminals and the voltage as a function of logic state and source or sink current for the output terminals. Proper current and voltage characteristics can be obtained by making a detailed model of the input and output circuitry. However, since the aim of simplified modeling is to reduce the number of elements, such detailed modeling is generally not done. Instead, elements such as nonlinear dependent current sources are used to approximate the desired current and voltage response of the terminal. For MOS circuitry, a single capacitor may accurately model device input characteristics while for many circuit types a simple Thevenin equivalent circuit (switched voltage source and constant output resistor) may provide an adequate model of the output characteristics. As always, the models chosen should be the simplest ones needed to give required results and should be consistent with the data available.

The correct logic functioning of a device can be simulated by making a detailed model of the internal circuitry (reference VI-11). Such a model can be extremely complex and can require large amounts of computer

memory and central processor time. Tremendous savings can be realized by simply modeling the internal logic functioning of a device by a Boolean algebra description of the logic. Computers are particularly efficient at handling logic operations. Of course, it is necessary to translate voltages and currents at the inputs into logic ones and zeros for internal processing and to convert them back to currents and voltages at the output.

Because a finite amount of time is required for signals to propagate through logic elements, logic circuits do not follow the laws of Boolean algebra instantaneously. Therefore, simulations should include the internal delay characteristics of a digital circuit. This can be done through the use of electrical elements such as RC networks, or through the use of special logic delay elements. Models may also simulate the rise- and falltime characteristics of a digital circuit's output terminals. This is usually done through use of appropriate electrical elements.

Radiation effects can be included in the simplified models by making appropriate modifications to the electrical model based on experimental data. Modifications may include transient or permanent changes in logic state, variations in propagation delay and output sink current capability, and transient photocurrents at device inputs. Power monitoring elements can also be included at the device terminals to monitor EMP-induced burnout.

Boolean algebra is not easily implemented in SPICE2 since the code does not allow user-defined equations or subroutines. For problems of moderate complexity, SPICE2 can still be used by making extremely simplified models of the internal logic gates. However, for more complex problems, a code which allows a Boolean processor to be implemented through methods such as FORTRAN subroutines is preferable. SCEPTRE and NET-2 are especially useful for logic simulations since they not only allow user-defined equations and subroutines, but they also incorporate logic elements as models. The advanced version of SCEPTRE, called SCEPTRE/LOGIC, includes a powerful Boolean processor. Logic networks can

be described in terms similar to normal SCEPTRE network descriptions. NET-2 incorporates logic elements among its system elements and can also describe logic networks in a fashion similar to normal electrical networks.

2. <u>Techniques for Simplified Modeling of Digital Circuits</u>

a. <u>Terminal Models</u>

Simplified models should correctly simulate the terminal current and voltage characteristics of the device being modeled so that the simplified model may be used with other elements in a circuit analysis code to predict system response. Terminal response can usually be simulated with very few elements. Of course, greater sophistication can be realized by including more elements or by using more complex elements. However, such sophistication increases memory and central processor time requirements.

The task of parameterizing terminal models can usually be performed from specification sheets which typically give detailed information about the terminal characteristics of integrated circuits. Manufacturing tolerances for IC's are generally better controlled than those for discrete components, so it is often acceptable to use the manufacturer's typical or worst case data in parameterizing terminal models.

Reference VI-12 indicates the kind of detailed information available on TTL integrated circuits. Figure VI-35 shows a plot of the input terminal voltage-current characterisitc of a typical TTL device. Superimposed on the same plot is a representation of a simplified model (dashed line) which can be implemented using a voltage controlled current source defined through a table or a subroutine. It has a value of -1 mA for terminal voltages below 1.75 volts and a value of 40 μA above 1.75 volts. Such a model will generally be sufficiently accurate for most applications. If such input curves were not available, they could be easily measured using a curve tracer as shown in figure VI-36.

Similar techniques can be used to model the output characteristics with one important difference. The output characteristics depend on the logic state of the output, which in turn depends on the

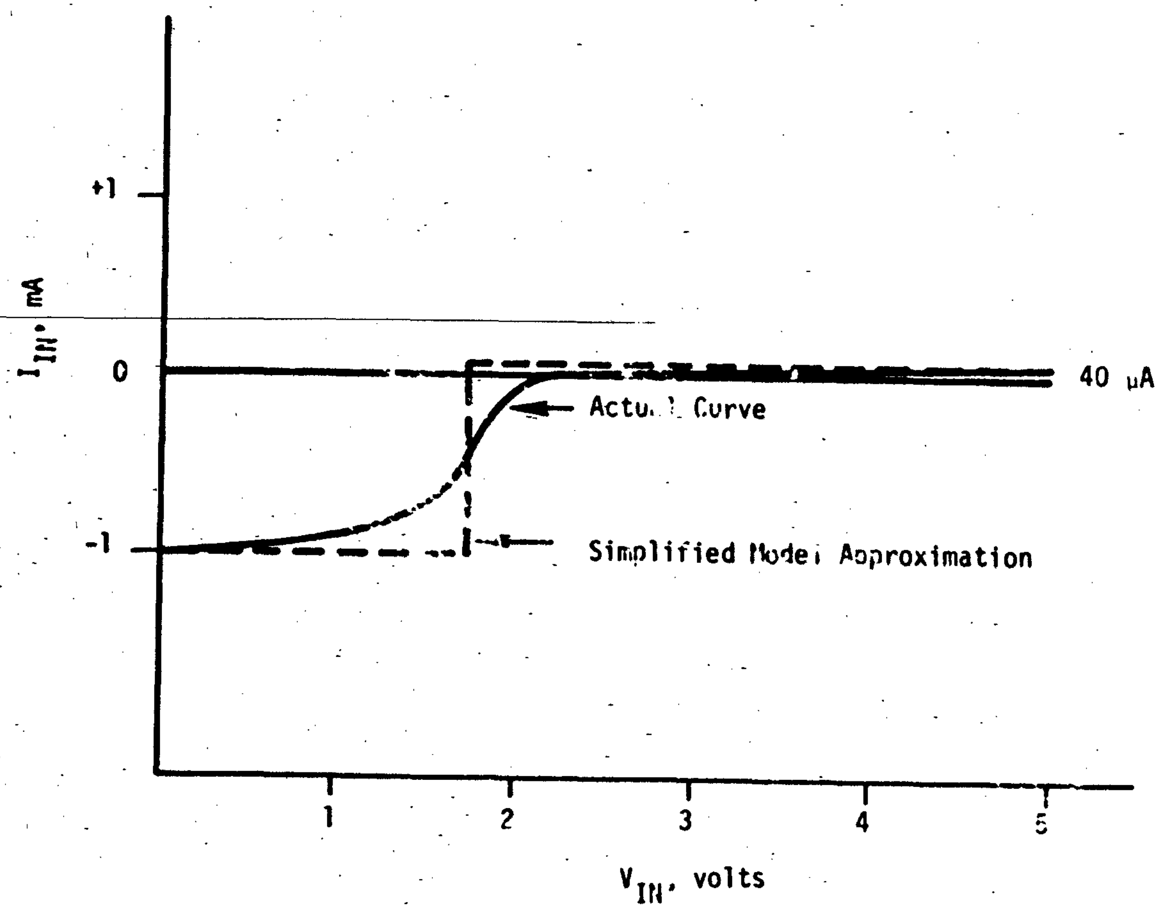


Figure VI-35. TTL Input Characteristics

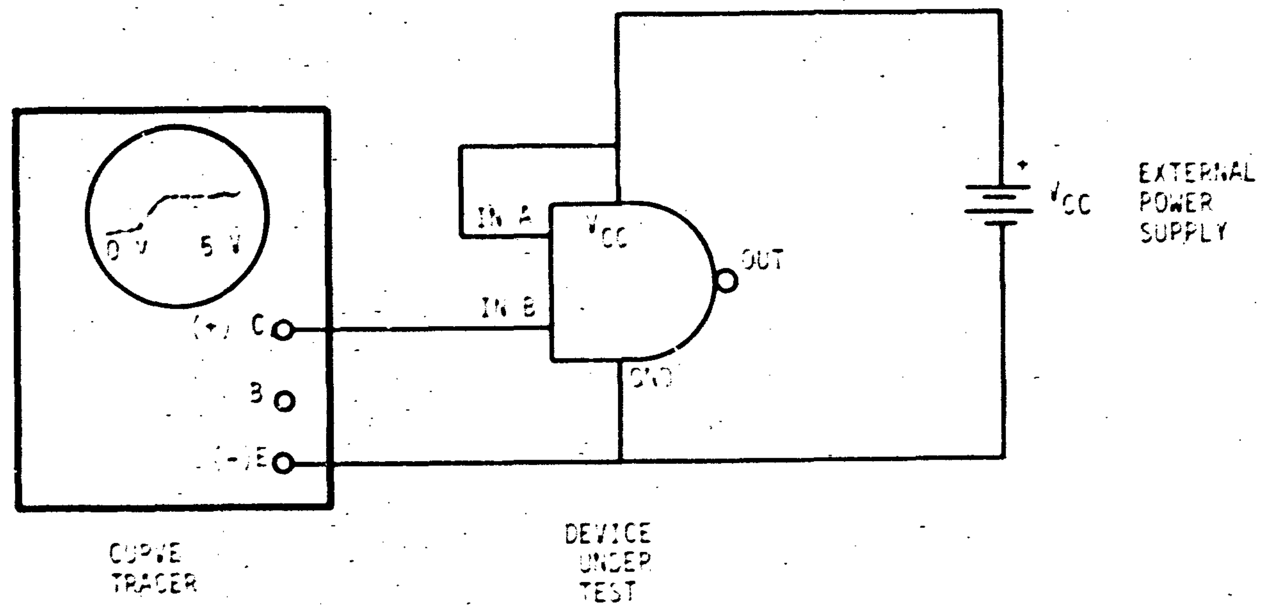


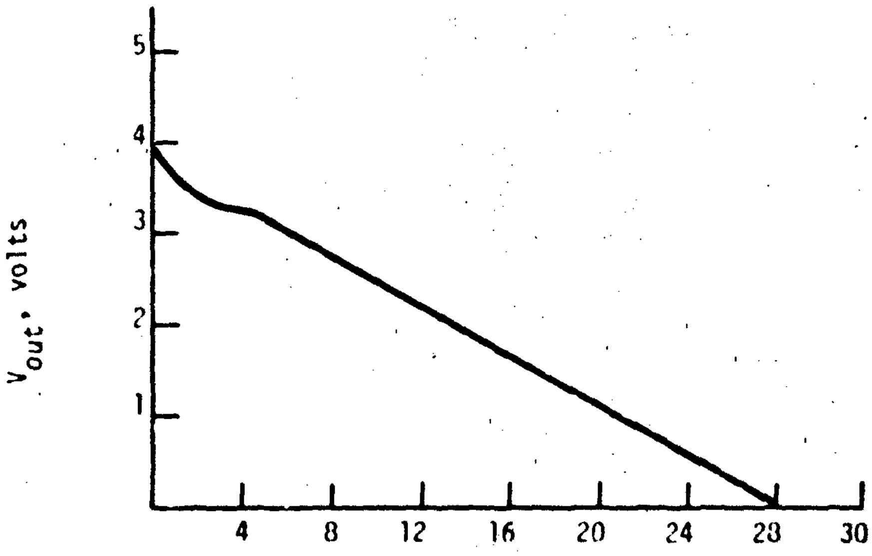
Figure VI-36. Measurement of Device Input Characteristics

internal logic states of the device. This generally means that the analyst must provide a means to switch the output characteristics as the state changes. Figure VI-37 shows the output characteristics of a typical TTL gate. It appears that the one state output characteristics can be modeled easily by a Thevenin equivalent circuit. The zero state characteristics can also be simulated by a Thevenin equivalent circuit up to the point where the voltage begins to rise rapidly (70 mA in figure VI-37(b)).

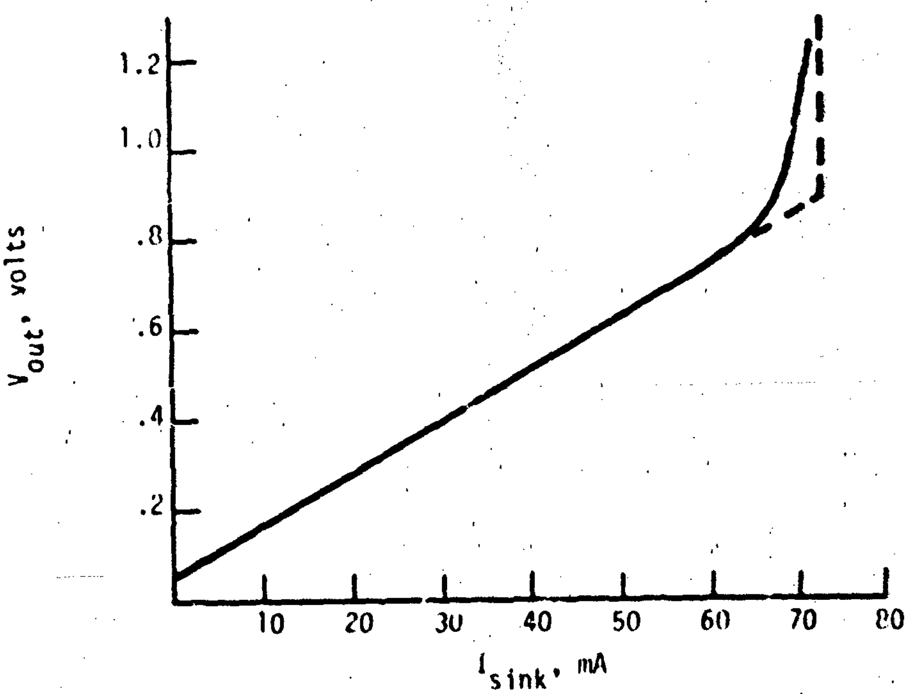
Depending on the degree of accuracy desired, the output characteristics can be modeled by a switched Thevenin voltage source (one state = 3.9 V, zero state = .05 V) plus a single Thevenin resistor, a switched resistor, or a voltage controlled current source to simulate a piecewise-linear resistor. These possibilities are shown in figure VI-38. In figure VI-38(a), the fixed resistor was chosen to simulate the low state current sink capability since this is usually more important in TTL than the high state current source capability. Both the high and low state impedances are simulated in the model of figure VI-38(b). Note that for both of these simple cases, the output low state characteristics are only valid for sink currents less than about 72 mA. In the third case, figure VI-38(c), the resistor is replaced by a voltage-controlled current source to get away from problems with nonconstant resistors. Note that for the zero state, the output current is limited to 72 mA.

If output curves are not available from manufacturer's data, they may be obtained using a curve tracer as shown in figure VI-39. If actual devices are not available, detailed models may be used to predict the terminal characteristics.

Device input and output capacitances are generally not modeled, and all capacitive effects are included in the propagation delay time. However, it may be necessary to include terminal capacitance to prevent computational delays in state-variable codes such as SCEPTRE. A nominal capacitance value of a few picofarads will generally be acceptable for this purpose. The effects of these capacitors should be accounted for when modeling propagation delay.

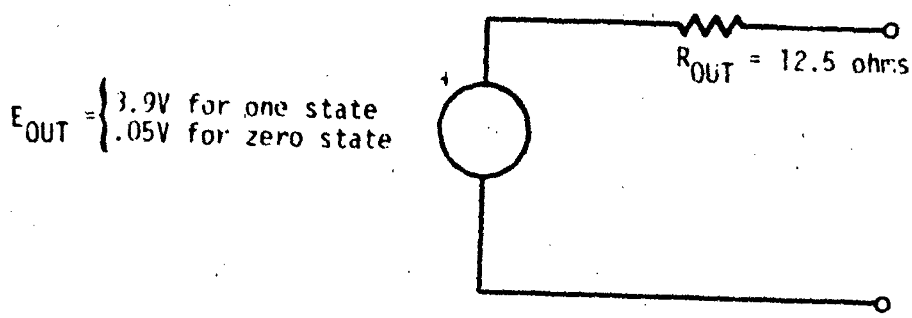


(a) One State Output Characteristics

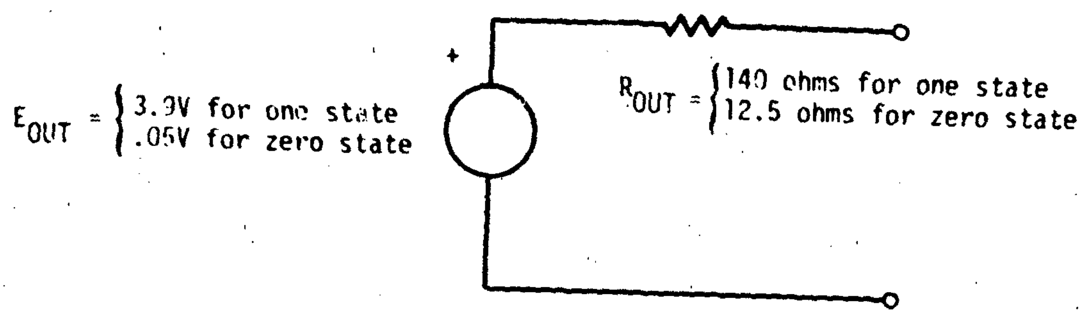


(b) Zero State Output Characteristics

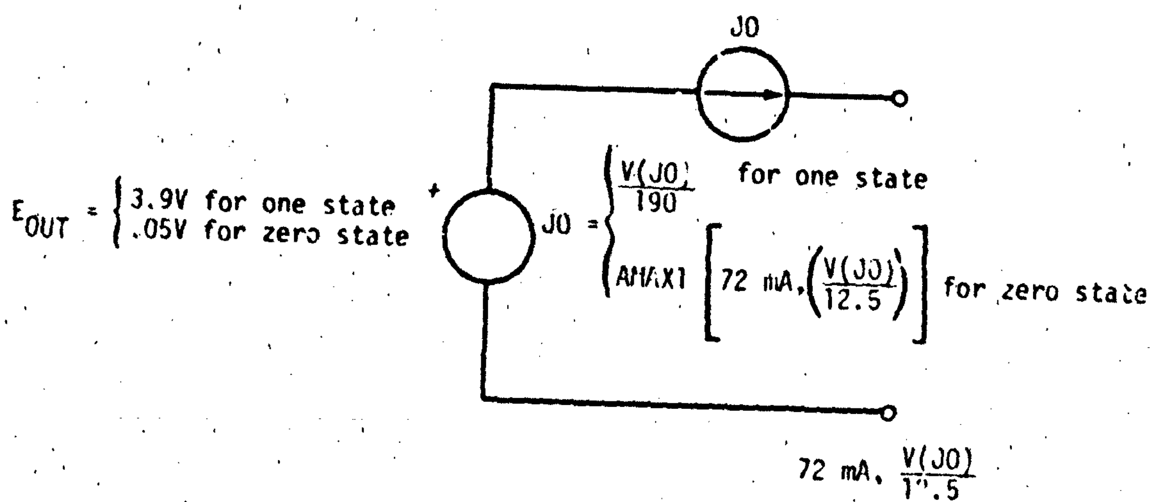
Figure VI-37. Typical TTL Output Characteristics



a) Single Resistor



b) Switched Resistor



c) Voltage Controlled Current Source to Simulate Piecewise Linear Resistor

Figure VI-38. Implementing Output Characteristics

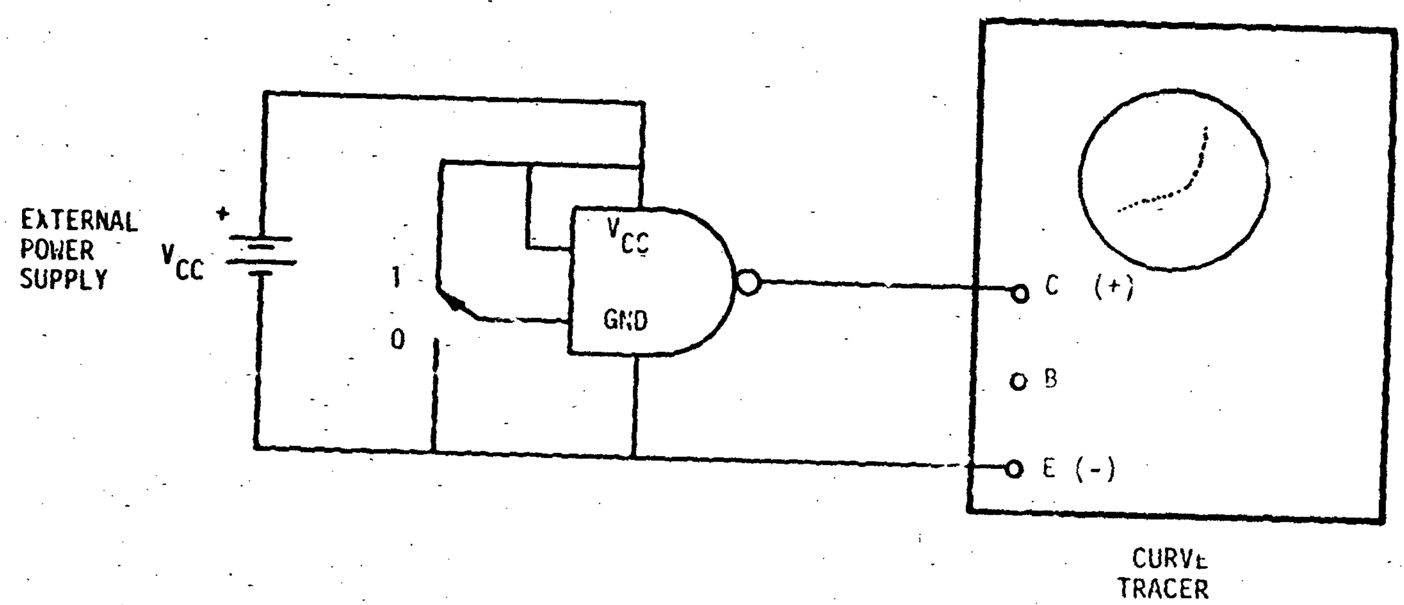


Figure VI-39. Measurement of Device Output Characteristics

b. Logic Models

1) Subroutines

Since the internal logic functions of digital integrated circuits follow the rules of Boolean algebra, the Boolean functions of computer languages such as FORTRAN can be used in subroutines to simulate proper logic operations. To do this, a thresholding function is required to convert input currents and voltages to Boolean variables. The logic function is then simulated and the Boolean result transformed back into currents and voltages at the outputs.

The input thresholding can be accomplished very simply in the subroutine by the use of conditional statements. For instance, if the input voltage is greater then 1.75 volts, a logic variable might be set to the one state. All such input variables thus defined as ones or zeros can be processed with logical operators to determine the correct output states. The values of the output elements can be determined once the proper output state is known. Propagation delay effects can be modeled by the use of RC timing elements in the output stage. Variable delay times can be simulated by varying the values of the RC elements according to the direction of the transitions.

Functions such as flip-flops and edge detectors can be simulated in the subroutines by retaining previous values of parameters and using them in a new subroutine call. Either positive or negative edge detection can be accomplished by looking for increasing or decreasing values of the parameter in question. A thresholding function usually must be included along with edge detection to prevent false triggering on "glitches."

Examples later in the chapter help illustrate the process of logic modeling using subroutines.

2) Logic Elements

Writing subroutines for logic descriptions of large digital networks becomes a difficult and error-prone task. Two codes offer a way around this problem, SCEPTRE and NET-2. Both of the codes allow the inclusion of logic elements (gates, flip-flops, etc.) in a form

close to the normal electrical network modeling. This capability allows the analyst to describe the electrical and logic networks in the most familiar way.

The concept of a combination of current and voltage modeling and Boolean algebra modeling is referred to as composite modeling. Figure VI-40 helps illustrate this concept. Two models are actually shown in this figure. To the left of the solid line is a detailed current-voltage (I/V) model of the device's input protection network. It is included to emphasize that the composite model must interface with normal I/V models and circuit elements. To the right of the solid line is a composite model of a portion of the CD4051, a CMOS analog multiplexer.

The first element of the composite model is capacitor CA. It represents the gate capacitance of the input MOS devices. The voltage across CA represents the I/V value which will serve as the input to the Boolean simulation. The dashed line box bounds the Boolean model. The dashed connecting line from CA to NOR gate NA indicates a thresholding operation takes place there, converting from I/V space to Boolean space. A radiation input also crosses the boundary into Boolean space indicating that a thresholding operation can also take place there. For example, dose rates greater than 1×10^9 rads (Si)/sec might be used to produce a one state input to a given gate.

Once the thresholds are established, the Boolean processor performs the operation indicated by the various gates and delay elements. The results at the output are transformed back into currents and voltage through a controlled current source. In this case, the output is a CMOS transmission gate. The current value is controlled by the output voltage and the logic state. For a one state, the output resistance is effectively 145 ohms while it is 500 megohms for a zero state.

Figure VI-41 lists the types of logic elements available in SCEPTRE/LOGIC. The AND, OR, NAND, and NOR elements allow multiple inputs while the EXCLUSIVE OR allows only two and the INVERTER only one. Any Boolean expression (an adder for example) with or without feedback

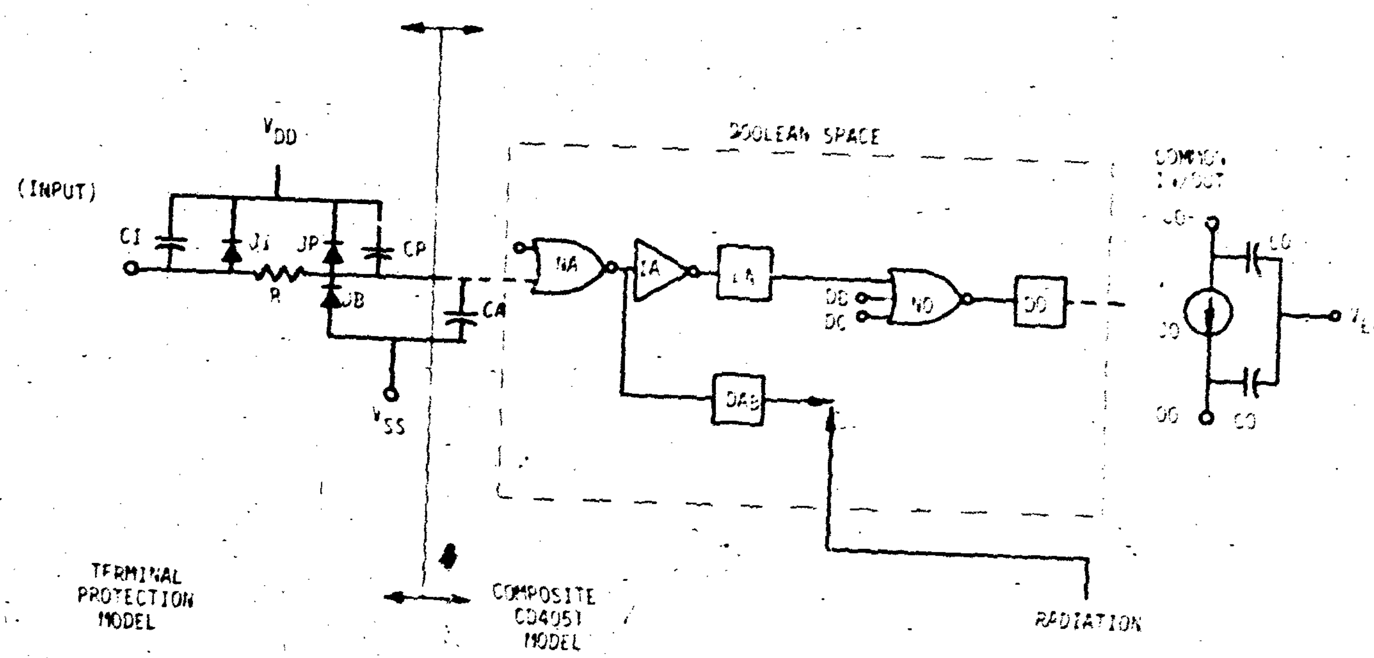


Figure VI-40. Composite Model

Key Letter	Element
A	AND
O	OR
M	NAND
N	NOR
I	INVERTER
E	EXCLUSIVE OR
X	BOOLEAN EXPRESSION
Z	BOOLEAN EXPRESSION WITH FEEDBACK
B	FLIP-FLOP
D	DELAY
U	EDGE DETECTOR
T	LOGIC TRANSISTOR

Figure VI-41. Key Letters and Corresponding Logical Elements for SCEPTRE/LOGIC

can be included without assembling a collection of gates. The flip-flop element is a J-K type with set and reset. This type can be used to generate any other flip-flop type with appropriate connections. The delay element can be a delay within a given time step to assure proper sequencing or it can be a given time delay. A delay element can have different delay times for positive and negative transitions. An edge detector is included which can detect either positive or negative edges. The logic transistor allows simulation of some of the logic functions of saturated transistors.

The logic elements of NET-2, part of the system elements incorporated into that code, are shown in figure VI-42. While the list is not as extensive as that for SCEPTRE/LOGIC, it is still possible to model logic networks in a straightforward manner. Time delay elements and hysteresis effects are allowed for. The AND, OR, and EOR functions allow multiple inputs. The RST FLIP-FLOP can accomplish all flip-flop functions if external gating is used. It has a built-in edge detector element.

Key	Element
DELAY	DELAY
HYST	HYSTERESIS
AND	AND
OR	OR
EOR	EXCLUSIVE OR
RSTFF	RST FLIP-FLOP

Figure VI-42. Logic elements in NET-2

An example of composite modeling is presented later in this chapter. Example 5 in chapter VII shows how composite modeling can be used to simulate large circuits.

c. Radiation Effects

1) Neutron and Total Dose Effects

The effects of neutrons and total ionizing dose are to change the parameter describing the input and output characteristics and the propagation delay time. These effects can be incorporated by making the appropriate parameter changes based on experimental measurements. It is possible to simulate complete logic failure of a node internal to the device, but this is usually of little interest except in device failure analysis.

It is usually most important to simulate the loss of output current sink capability and the changes in propagation delay time.

2) Dose Rate Effects

The effects of ionizing dose rate can be simulated by adding the appropriate photocurrent generators to the input and output terminals and by making transient logic state changes internal to the device. The proper values of photocurrent and the proper state changes can be determined experimentally.

Terminal photocurrents must be simulated accurately. A device may show no false state changes when tested alone, but may upset in a circuit where terminal photocurrents can interact with other circuit elements to produce unwanted signals.

3) EMP Effects

The effects of EMP upset are simulated by the normal electrical model of the device. The effects of EMP-induced burnout can be modeled using a modified version of the techniques presented in chapter II.

A power monitoring element is included at each terminal to be studied. This element does not affect normal electrical operation. It does simulate the terminal voltage and current characteristics when it is driven into breakdown. As shown in figure VI-43, this operation is characterized by a breakdown voltage and a surge resistance. The parameters can be determined experimentally or can be determined from the data presented in reference VI-9.

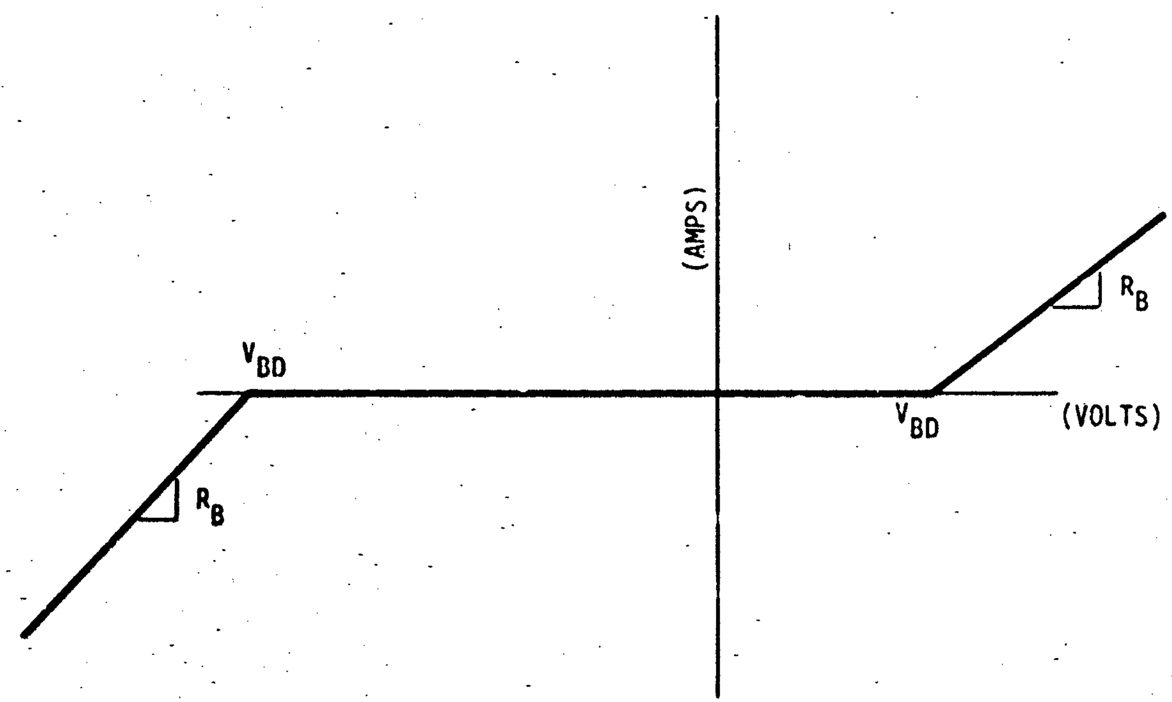


Figure VI-43. Diode Table for the Simplified EMP Model

The power required to fail the terminal is defined by

$$P_f = At^{-B}$$

where A and B are experimentally determined coefficients and t is the duration of the overstress pulse. Values for A and B and the breakdown voltage and surge resistance may also be found in reference VI-9. The actual power in the power monitoring element is compared to the failure power. A message is printed if the actual power exceeds the failure power.

3. Example Digital Simplified Models

a. RSN54L00

A simplified model of this low power TTL NAND gate will be developed in SCEPTRE using a subroutine to define the functional operation. The techniques used here are specific to SCEPTRE but can be adjusted to any circuit analysis code which allows the use of subroutines.

The manufacturer data sheet for the RSN54L00 is shown in figure VI-44. Data were taken from this sheet and from reference VI-11 in parameterizing the simplified model. The topology of the simplified model is shown in figure VI-45. Since the maximum input current is only 0.18 mA, the input current will not be modeled. Current sources JA and JB will have a zero value and will serve to measure the input voltages. If the input must be modeled, values for JA and JB can be specified in tables.

The second stage defines the logic state of the output based on the voltages sensed across JA and JB. The logic state is set through E1 which is defined by the following logical statements.

```
IF    VJA and VJB < 0.8V
THEN  E1  =  3.1V

IF    VJA or VJB > 0.8V
THEN  E1  =  0.3V
```

CIRCUIT TYPES RSN54L00, RSN54L10, RSN54L20, RSN54L130, RSN54L131
POSITIVE-NAND GATES

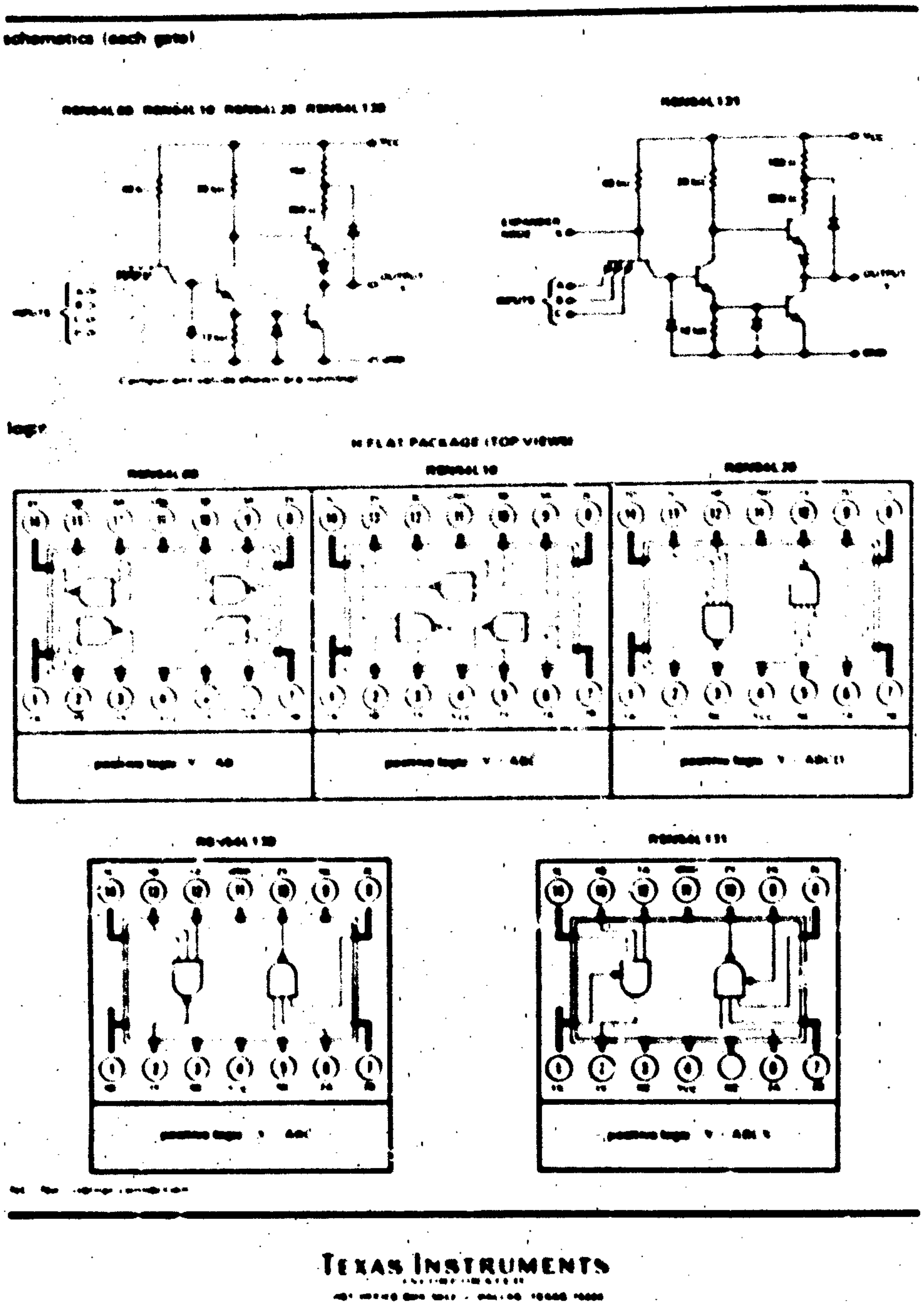


Figure VI-44. RSN54L00 Manufacturer Specification Sheet (ref. VI-13)

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from each gate, N			10	
Operating free-air temperature, T_A	55		125	C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage	1		1.9		V
V_{IL}	Low-level input voltage	2			0.8	
V_{OH}	High-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = 100 µA	2.4		V
V_{OL}	Low-level output voltage	1	V_{CC} = MIN, V_{IH} = 1.9 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	3	V_{CC} = MAX, V_I = 5.5 V		100	µA
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V		10	µA
I_{IL}	Low-level input current	4	V_{CC} = MAX, V_I = 0.3 V		0.18	mA
I_{OS}	Short-circuit output current	5	V_{CC} = MAX	3	15	mA
I_{CCH}	Supply current, high-level output (average per gate)	6	V_{CC} = MAX, V_I = 0		0.2	mA
I_{CCL}	Supply current, low-level output (average per gate)	6	V_{CC} = MAX, V_I = 4.5 V		0.51	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

switching characteristics, V_{CC} = 5 V, T_A = 25 C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	28	C_L = 50 pF, R_L = 4 kΩ		60	ns
t_{PHL}	Propagation delay time, high-to-low-level output				60	ns

Figure VI-44. RSN54L00 Manufacturer Specification Sheet (Concluded)

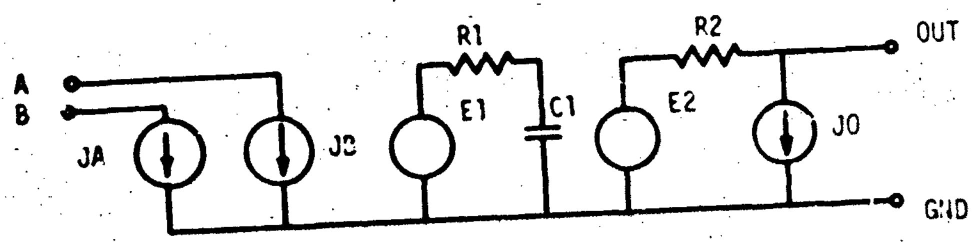


Figure VI-45. Simplified Model of RSN54L00 NAND Gate

The delay stage is composed of E1, R1, and C1. The time constant R1C1 determines the propagation delay of a state change through the IC. In this model, the time constant is conditionally altered by a subroutine to satisfy both the low-to-high propagation delay and the high-to-low propagation delay.

The output characteristics are modeled by the last stage composed of E2, R2, and J0. E2 is a dependent voltage source equal to the voltage across capacitor C1. Doing this eliminates any loading of the propagation delay stage. R2 is chosen to approximate the low state output impedance characteristics of the gate.

The RSN54L00 model was tested using the circuit of figure VI-46. The purpose of the circuitry connected to the output of the gate is to simulate the loading and fan-out effects of other TTL circuitry driven by the gate.

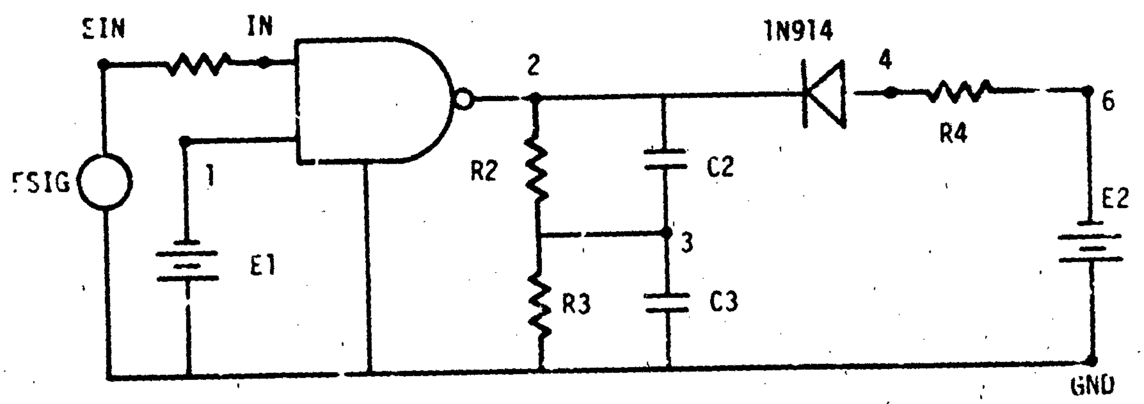


Figure VI-46. RSN54L00 Test Circuit

The SCEPTRE test circuit, as input to SCEPTRE, is presented in figure VI-47. Proper logic operation is established by the subroutine FN2. Subroutine FCAP1 selects the proper value of capacitor C1 to model the propagation delay time for either a high-to-low or low-to-high transition. The input signal voltage has a waveform which is demonstrated in figure VI-48. The output of the NAND gate in response to the input voltage is given in figure VI-49. This test yields the truth table:

Input A	Input B	Output
0	1	1
1	1	0

which is consistent with the NAND truth table:

Input A	Input B	Output
0	1	1
1	1	0
0	0	1
1	0	1

Propagation delay time, low-to-high level output, is defined as that time from when the input signal drops to 1.5 volts to the time when the gate output rises to 1.5 volts. This time can be determined to be 20 ns from the simulation runs. This time is less then the maximum propagation delay time found in specification sheets (60 ns) and compares favorably to observed propagation delay times.

Propagation delay time, high-to-low level output, is defined as the time interval from when the input voltage rises to 1.5 volts to the time when the output voltage falls to 1.5 volts. Simulation produces a propagation delay time of 50 ns, which is under the specification sheet maximum of 60 ns.

b. CD4051

The power of composite modeling will be illustrated by modeling a CD4051 CMOS analog multiplexer using SCEPTRE/LOGIC. The CD4051 is predominantly a digital circuit which has analog outputs. A

```
S C E P T R E   NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2       5/76
 12/16/77     10.43.11.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD  "DOCUMENT"  AS THE FIRST CARD
OF THE INPUT TEXT


COMPUTER TIME ENTERING SETUP PHASE-
          CPA        .335 SEC.
          PP        0.000 SEC.
          IO        0.000 SEC.


SUBPROGRAM
CFN2              QUAD 2 INPUT NAND GATE LEVEL SELECT
C      FOR USE WITH 2 INPUT NAND GATE
       FUNCTION FN2(A,B,C,D,E,F)
C      A=VJA B=VJB C=0.8
C      D=3.1 E=1.9 F=0.3
       IF(A.LE.C.OR.B.LE.C)GO TO 4
       IF(A.GE.E.AND.B.GE.E)GO TO 5
       FN2=D-AMIN1(A,B)
       RETURN
     4 FN2=D
       RETURN
     5 FN2=F
       RETURN
       END
C              DIGITAL IC CAPACITOR SELECT
       FUNCTION FCAP1(A,B,C,D)
C      TO ESTABLISH CAPACITOR VALUE OF DIGITAL IC
       FCAP1=C
       IF(A.GE.B)FCAP1=D
       RETURN
       END
MODEL DESCRIPTION
MODEL L00(A-B-OUT-GND)
2 INPUT NAND GATE
A = INPUT A
B = INPUT B
ELEMENTS
JA,A-GND=0.
JB,B-GND=0.
JO,OUT-GND=0.
E1,GND-1=Q4(VJA,VJB,0.8,3.1,1.9,0.3)
R1,1-2=100.
```

Figure VI-47. RSN54L00 SCEPTRE Test Circuit

```
C1,2-GND=Q2(E1,E2,550.E-12,300.E-12)
E2, GND-3=X1(VC1)
R2,3-OUT=30.
FUNCTIONS
Q2(A,B,C,D)=(FCAP1(A,B,C,D))
Q4(A,B,C,D,E,F)=(FN2(A,B,C,D,E,F))
OUTPUTS
VJA(AIN),VJB(BIN),VJD(OUTPUT),PLOT
CIRCUIT DESCRIPTION
ELEMENTS
NA,IN-1-2-GND=MODEL .00
R2,2-3=4300.
C2,2-3=2.6E-12
R3,3-GND=750.
C3,3-GND=15.E-12
ESIG,GND-EIN=TABLE 1(TIME)
R1,EIN-IN=50.
E1,GND-1=2.4
CJD,4-2=1.E-12
JD,4-2=DIODE EQUATION(2.68E-14,33.28)
R4,4-5=800.
R5,6-5=1.
E2,GND-6=2.4
FUNCTIONS
TABLE 1
0,3,3.3E-7,3,3.7E-7,0.5,7.4E-7,0.5,7.5E-7,3,8.E-7,3
RUN CONTROLS
STOP TIME = 999.E-9
 MAXIMUM PRINT POINTS= 100
MINIMUM STEP SIZE = 1.E-18
OUTPUTS
ESIG,PLOT
END


THE TERM  VR1     WILL CAUSE A COMPUTATIONAL DELAY.



SYSTEM NOW ENTERING SIMULATION



COMPUTER TIME AT TERMINATION OF SETUP PHASE-
          CPA       2.324 SEC.
          PP        0.000 SEC.
          IO        0.000 SEC.
```

Figure VI-47. RSN54L00 SCEPTRE Test Circuit (Concluded)

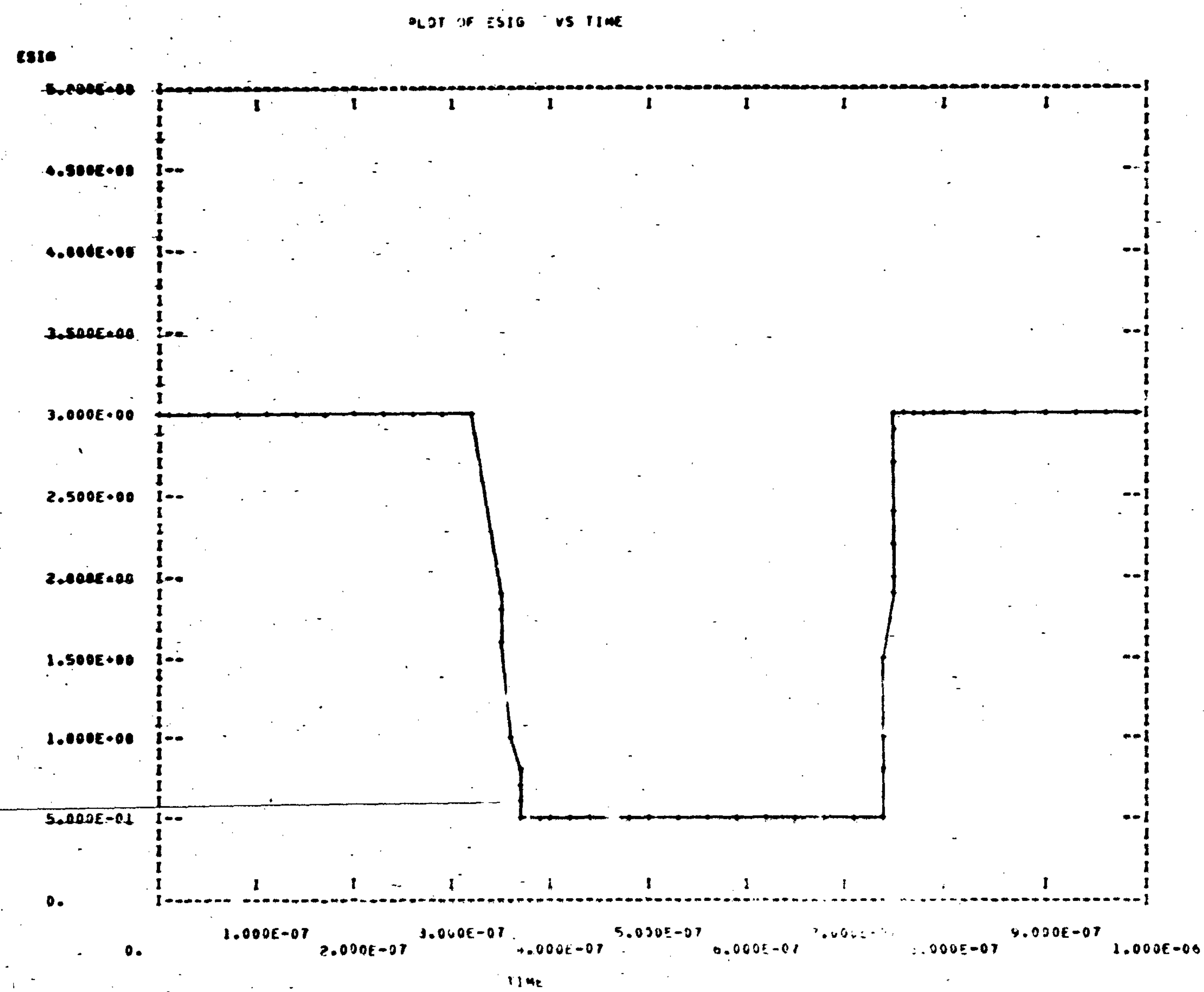


Figure VI-48. Input Voltage Waveform

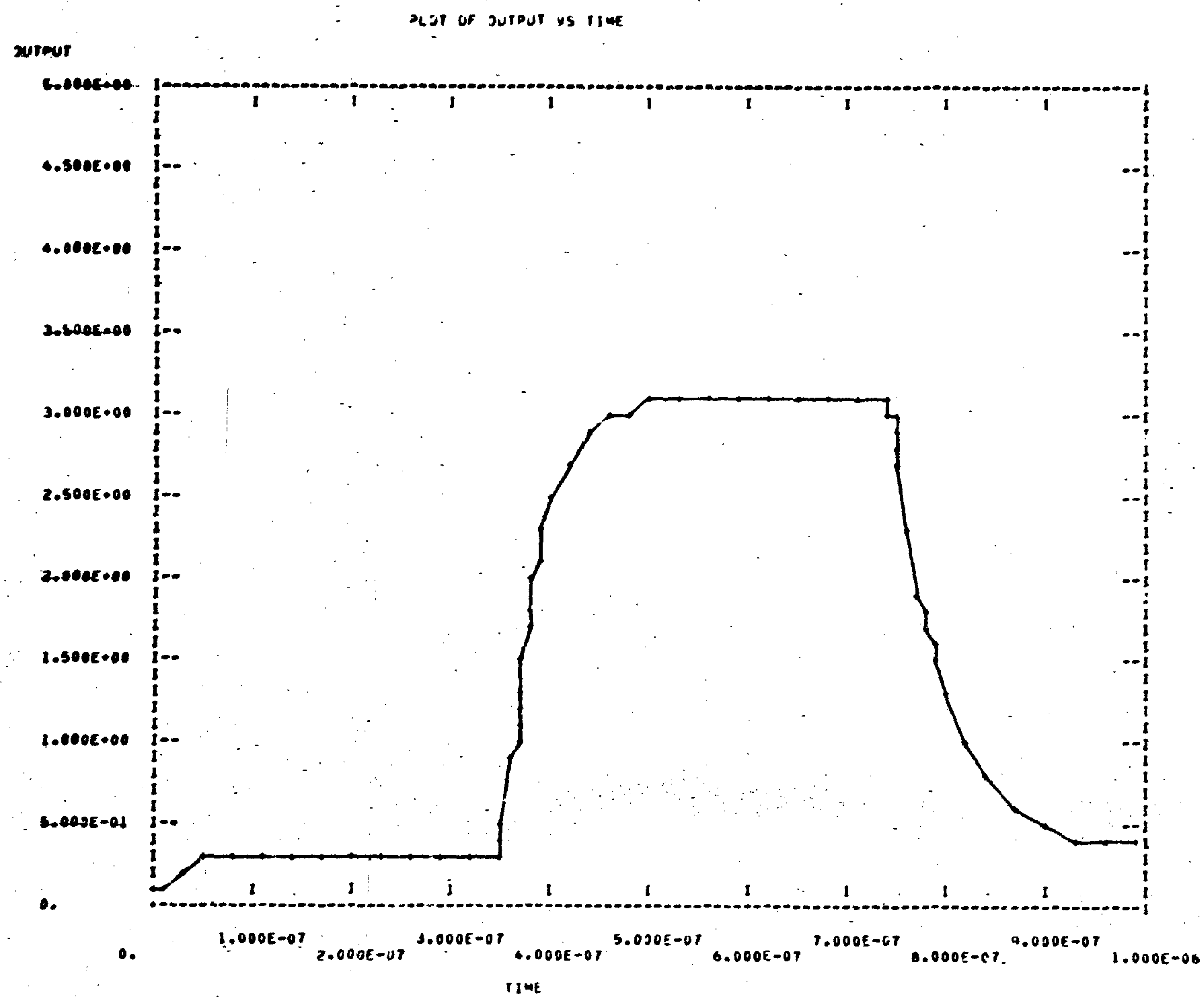


Figure VI-49. NAND Gate Output Waveform

data sheet is given in figure VI-50. Additional information was obtained through other data sheets and through visual inspection of an opened device. A complete description of the modeling of this device is given in reference VI-5.

Figures VI-51 and VI-52 give the circuit diagram and SCEPTRE listing of the CD4051 composite model. The particular listing given is from an EMP demonstration run, but it is essentially the same as the listings of the model and circuit description for electrical and photocurrent demonstrations The only differences lie in the specification of the input voltage generators (EA, EB, EC, and EI) and in the circuit description and the specification of a dose rate for the PGD defined parameter in the model.

In general, the model is a straightforward application of the composite modeling concepts to the circuit topology of the CD4051. The decoding network is included in the LOGIC model FCD051 which is called into the SCEPTRE model via the equation QIJ. The elements in the FCD051 represent a one-for-one substitution of logical elements for the functional blocks found in the CD4051 decoding network. The values for the delay elements were based on estimates of propagation delay of similar CMOS gates and on the results of detailed modeling of CMOS circuits.

The output of FCD051 is used to control the current sources JT0 through JT7. These current sources are essentially variable resistors which have been modeled as current sources due to SCEPTRE's aversion to nonconstant resistance. JT0 is equivalent to the transmission gate impedance connecting the common in/out terminal (node CO) with the channel 0 terminal (node 00). A constant value of transmission gate impedance has been chosen for the "channel on" state. Actually, the impedance varies as a function of current and of total dose. To model the variation in impedance, JT0 could be modeled with an I/V table. However, the nonconstant impedance was not a significant factor in either theoretical or experimental efforts for which this model was developed. Consequently, the simpler, constant impedance formulation was used.

CD4051B, CD4052B, CD4053B Types

COS/MOS Analog Multiplexers/Demultiplexers*

With Logic Level Conversion

High Voltage Types (3 to 20 Volt Rating)

CD4051B – Single 8-Channel Multiplexer/Demultiplexer

CD4052B – Differential 4-Channel Multiplexer/Demultiplexer

CD4053B – Triple 2-Channel Multiplexer/Demultiplexer

The RCA CD4051, CD4052 and CD4053 analog multiplexers demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V peak to peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if $V_{DD}-V_{SS}$ = 3 V, a $V_{DD}-V_{EE}$ of up to 13 V can be controlled; for $V_{DD}-V_{EE}$ level differences above 13 V, a $V_{DD}-V_{SS}$ of at least 4.5 V is required). For example, if V_{DD} = +5 V, V_{SS} = 0 and V_{EE} = −13.5 V, analog signals from −13.5 V to +4.5 V can be controlled by digital inputs of 0 to 4.5 V. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are OFF.

The CD4051 is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned ON, and connect one of the 8 inputs to the output.

The CD4052 is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053 is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

The CD4051, CD4052 and CD4053 are supplied in 16-lead ceramic dual-in-line packages (D, F, Y suffixes), 16-lead plastic dual-in-line packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

* When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.

MAXIMUM RATINGS, *Absolute-Maximum Values*

STORAGE TEMPERATURE RANGE (T_{STG})	−65 to +150°C
OPERATING TEMPERATURE RANGE (T_A)	
Package Types D, F, K, H	−55 to +125°C
Package Types E, Y	−40 to +85°C
DC SUPPLY VOLTAGE RANGE, V_{DD}	
(Voltages referenced to V_{SS} or V_{EE}, whichever is more negative)	−0.5 to +20 V
POWER DISSIPATION PER PACKAGE	
For T_A = −40 to +60°C (Package Types E, Y)	500 mW
For T_A = +60 to +85°C (Package Types E, Y)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (Package Types D, F, K)	500 mW
For T_A = +100 to +125°C (Package Types D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER CHANNEL	
For T_A = Full Package Temperature Range (All Package Types)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

RECOMMENDED OPERATING CONDITIONS AT T_A = 25°C (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

CHARACTERISTIC	V_{DD}	Min.	Max.	Units
Supply Voltage Range (T_A = Full Package Temp. Range)	–	3	18	V
Multiplexer Switch Input Current Capability*	–	–	25	mA
Output Load Resistance	–	100	–	Ω

* In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 3 on the CD4051, terminals 3 and 13 on the CD4052, terminals 4, 14, and 15 on the CD4053.

Applications

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating

Features

- Wide range of digital and analog signal levels: digital 3 to 20 V, analog to 20 V_{p-p}
- Low ON resistance: 125 Ω (typ.) over 15 V_{p-p} signal-input range for $V_{DD}-V_{EE}$ = 15 V
- High OFF resistance: channel leakage of ±10 pA (typ.) @ $V_{DD}-V_{EE}$ = 10 V
- Logic-level conversion for digital addressing signals of 3 to 20 V ($V_{DD}-V_{SS}$ = 3 to 20 V) to switch analog signals to 20 V p-p ($V_{DD}-V_{EE}$ = 20 V), see introductory text
- Matched switch characteristics: R_{ON} = 5 Ω (typ.) for $V_{DD}-V_{EE}$ = 15 V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2 μW (typ.) @ $V_{DD}-V_{SS}$ = $V_{DD}-V_{EE}$ = 10 V
- Binary address decoding on chip
- Quiescent current specified to 20 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)
- 5-, 10-, and 15-V parametric ratings

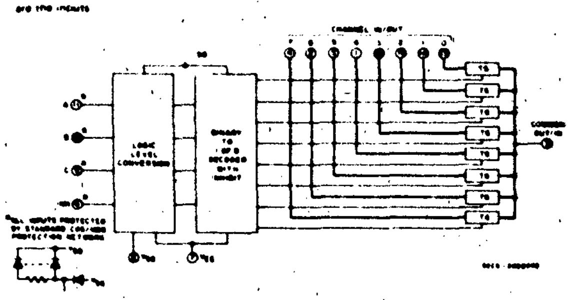


Fig. 1 – Functional diagram of CD4051.

Figure VI-50. CD4051 Manufacturer Specification Sheet (ref. VI-14)

CD4051B, CD4052B, CD4053B, Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS at Indicated Temperatures (°C) Values at −55, +25, +125, apply to D,F,K,H pkg Values at −40, +25, +85, apply to E,Y pkgs −55	−40	+85	+125	+25 Min.	Typ.	Max.	Units
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})												
Quiescent Device Current, I_L Max				5	5	5	50	100	–	0.02	5	µA
				10	10	10	100	200	–	0.02	10	
				15	20	20	200	400	–	0.02	20	
				20	100	100	1000	2000	–	0.04	100	
ON Resistance $0 \le V_{IS} \le V_{DD}$ R_{ON} Max		0	0	5	2000	2100	3700	3800	–	470	2500	Ω
		0	0	10	310	330	520	580	–	180	400	
		0	0	15	220	230	380	400	–	125	280	
Δ ON Resistance (Between Any Two Channels) ΔR_{ON}		0	0	5	–	–	–	–	–	10	–	Ω
		0	0	10	–	–	–	–	–	10	–	
		0	0	15	–	–	–	–	–	5	–	
OFF Channel Leakage Current Any Channel OFF Max		0	0	10	±200*				–	±0.1	±200*	nA
		0	0	15	±500*				–	±0.1	±200*	
		0	0	20	±1000*				–	±0.1	±200*	
All Channels OFF (Common OUT/IN) Max		0	0	10	±200*				–	±0.1	±200*	
		0	0	15	±500*				–	±0.1	±200*	
		0	0	20	±1000*					±0.1	±200*	
Capacitance Input C_{IS}		−5	−5	5	–	–	–	–	–	5	–	pF
Output C_{OS} CD4051					–	–	–	–	–	30	–	
CD4052					–	–	–	–	–	18	–	
CD4053					–	–	–	–	–	9	–	
Feedthrough C_{IOS}					–	–	–	–	–	0.2	–	
Propagation Delay Time (Signal Input to Output)	10V	$R_L = 10\,k\Omega$		5	–	–	–	–	–	30	–	ns
		$C_L = 50\,pF$		10	–	–	–	–	–	15	–	
		$t_r, t_f = 20\,ns$		15	–	–	–	–	–	11	–	

* Determined by minimum feasible leakage measurement for automatic testing.

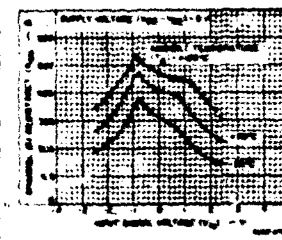


Fig.3 – Typical channel ON resistance vs input signal voltage (all types).

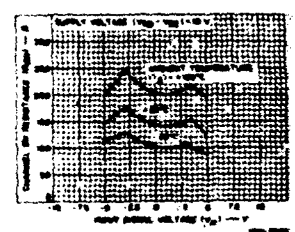


Fig.4 – Typical channel ON resistance vs. input signal voltage (all types).

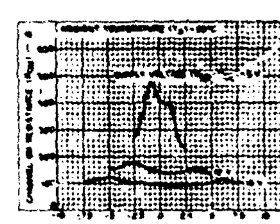


Fig.5 – Typical channel ON resistance vs. input signal voltage (all types).

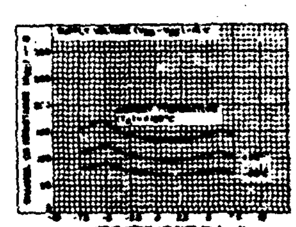


Fig. 6 – Typical channel ON resistance vs. input signal voltage (all types).

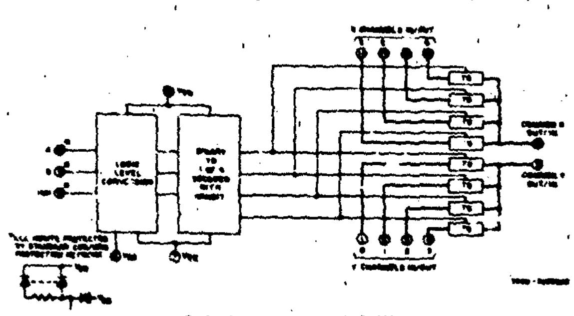


Fig.2 – Functional diagram of CD4052.

Figure VI-50. CD4051 Manufacturer Specification Sheet (Continued)

CD4051B, CD4052B, CD4053B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS at Indicated Temperatures (°C) Values at −55, +25, +125, apply to D,F,K,H pkg; Values at −40, +25, +85, apply to E,Y pkgs: −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	Units
CONTROL (ADDRESS or INHIBIT) V_C												
Noise Immunity V_{NM}: Inputs Low V_{NIL}	V_{DD} thru 1 kΩ	$V_{EE}=V_{SS}$, $R_L=1$ kΩ to V_{SS}, $I_{IS}<2$ µA on all OFF Channels		5	1.5				1.5	2.25	–	V
				10	3				3	4.5	–	V
				15	4.5				4.5	6.75	–	V
Inputs High, V_{NIH}				5	1.5				1.5	2.25	–	V
				10	3				3	4.5	–	V
				15	4.5				4.5	6.75	–	V
Input Leakage Current I_{IL}, I_{IH} Max.		("A" Series)		15	±1				–	$\pm10^{-5}$	±1	µA
		("B" Series)		20	±1				–	$\pm10^{-5}$	±1	µA
Propagation Delay Time: Address-to-Signal OUT (Channels ON or OFF) See Figs. 14, 15, 18	$t_r, t_f=20$ ns, $C_L=50$ pF											
		0	0	5	–	–	–	–	–	300	720	ns
		0	0	10	–	–	–	–	–	180	320	ns
		0	0	15	–	–	–	–	–	120	240	ns
		−5	0	5	–	–	–	–	–	225	450	ns
Inhibit-to-Signal OUT (Channel turning ON)	$R_L=10$ kΩ, $C_L=50$ pF, $t_r, t_f=20$ ns											
		0	0	5	–	–	–	–	–	380	720	ns
		0	0	10	–	–	–	–	–	160	320	ns
		0	0	15	–	–	–	–	–	120	240	ns
		−10	0	5	–	–	–	–		200	400	ns
Inhibit-to-Signal OUT (Channel turning OFF)	$R_L=300$ Ω, $C_L=50$ pF, $t_r, t_f=20$ ns											
		0	0	5	–	–	–	–	–	200	450	ns
		0	0	10	–	–	–	–	–	90	210	ns
		0	0	15	–	–	–	–	–	70	160	ns
		−5	0	5	–	–	–	–	–	130	300	ns
Average Input Capacitance, C_I (Any Address or Inhibit Input)					–	–	–	–	–	5	–	pF

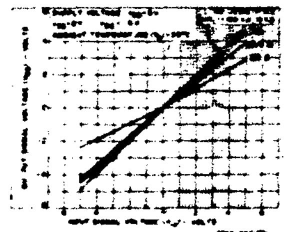


Fig.8 – Typical ON characteristics for 1 of 8 channels (CD4051)

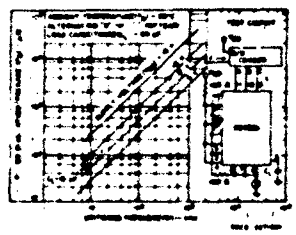


Fig.9 – Typical dynamic power dissipation vs. switching frequency (CD4051)

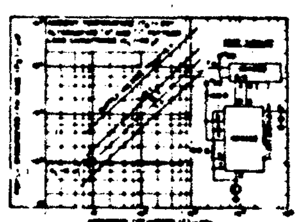


Fig.10 – Typical dynamic power dissipation vs. switching frequency (CD4052)

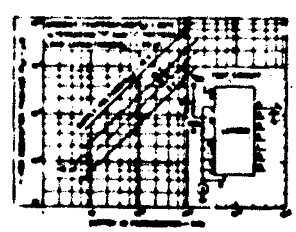


Fig.11 – Typical dynamic power dissipation vs. switching frequency (CD4053)

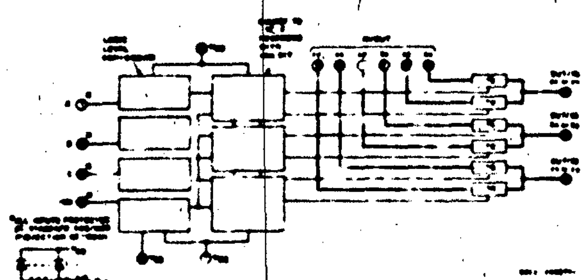


Fig.7 – Functional diagram of CD4052

Figure VI-50 CD4051 Manufacturer Specification Sheet (Continued)

CD4051B, CD4052B, CD4053B Types

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS V_{IS} (V)	V_{DD} (V)	R_L (kΩ)	TYPICAL LIMITS AT INDICATED CONDITIONS		VALUE	UNITS
Frequency Response Channel "ON" (Sine Wave Input)	5*	10	1	V_{OS} at Common OUT/IN	CD4053	30	MHz
	VEE = VSS				CD4052	25	
	20 log V_{OS}/V_{IS} = -3 dB				CD4051	20	
				V_{OS} at Any Channel		60	
Sine Wave Response (Distortion)	2*	5	10			0.3	%
	3*	10				0.2	
	5*	15				0.12	
	VEE = VSS, f_{IS} = 1 kHz						
Feedthrough (All Channels OFF)	5*	10	1	V_{OS} at Common OUT/IN	CD4053	8	MHz
	VEE = VSS				CD4052	10	
	20 log V_{OS}/V_{IS} = -40 dB				CD4051	12	
				V_{OS} at Any Channel		8	
Signal Crosstalk (Frequency at -40 dB)	5*	10	1	Between Any 2 Channels		3	MHz
	VEE = VSS			Between Sections CD4052 Only	Measured on Common	6	
	20 log V_{OS}/V_{IS} = -40 dB				Measured on Any Channel	10	
				Between Any 2 Sections CD4053 Only	In Pin 2, Out Pin 14	2.5	
					In Pin 15, Out Pin 14	6	
Address-or-Inhibit-to-Signal Crosstalk		10	10*			65	mV (Peak)
	VEE = VSS, t_r, t_f = 20 ns, V_C = VDD - VSS (Square Wave)						

* Peak-to-peak voltage symmetrical about $\frac{V_{DD} - V_{EE}}{2}$

Both ends of channel

INPUT STATES INHIBIT	C	B	A	"ON" CHANNEL(S)
CD4051				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE
CD4052				
INHIBIT		B	A	
0		0	0	0x, 0y
0		0	1	1x, 1y
0		1	0	2x, 2y
0		1	1	3x, 3y
1		X	X	NONE
CD4053				
INHIBIT	A or B or C			
0	0			ax or bx or cx
0	1			ay or by or cy
1	X			NONE

X = Don't care

Fig. 18 – Truth table.

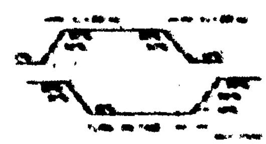


Fig. 19 – Waveforms, channel being turned ON (R_L = 10 kΩ).

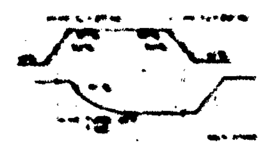
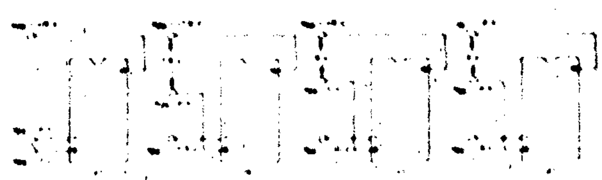


Fig. 20 – Waveforms, channel being turned OFF (R_L = 300 Ω).



The ADDRESS (digital control inputs) and INHIBIT logic levels are "0" = V_{SS} and "1" = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

Fig. 17 – Typical bias voltages.

Figure VI-50. CD4051 Manufacturer Specification Sheet (Continued)

CD4051B, CD4052B, CD4053B Types

TEST CIRCUITS

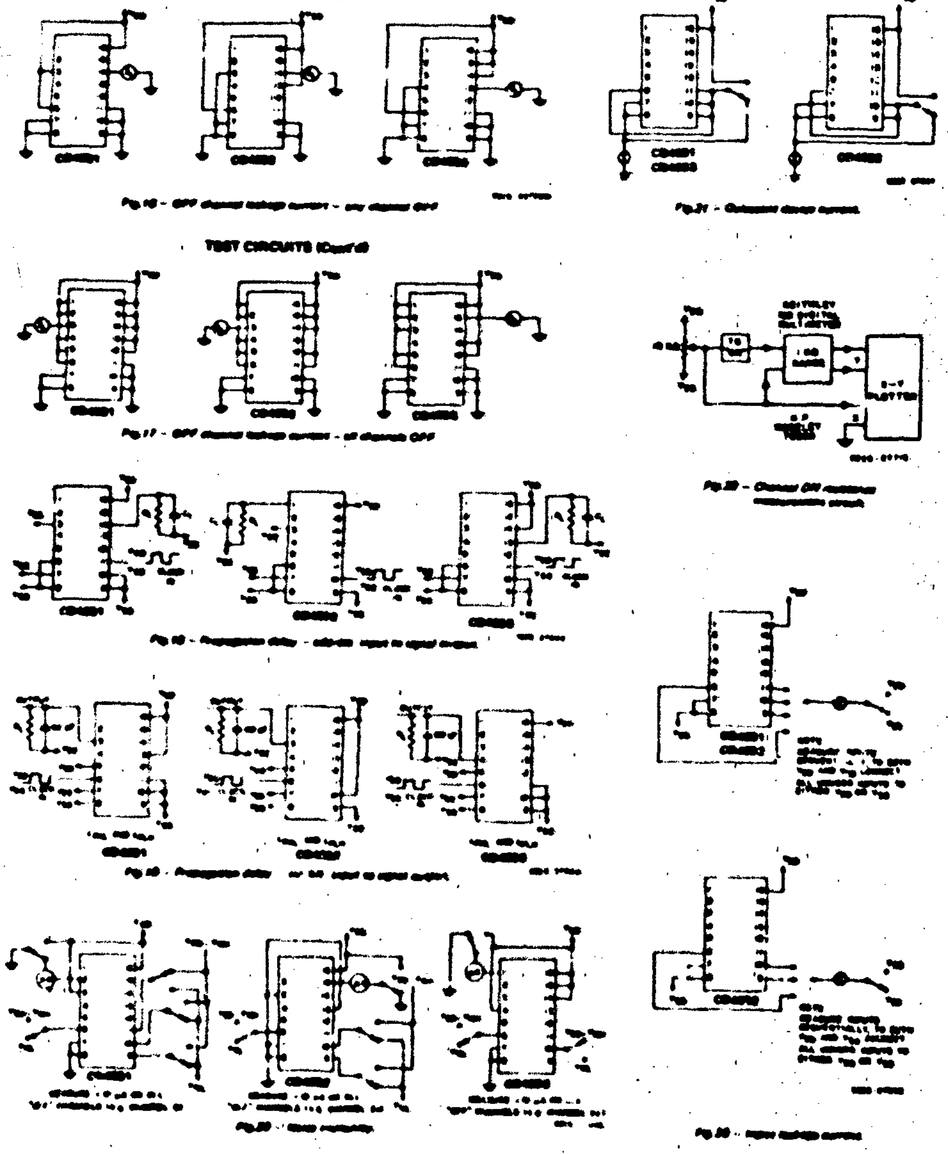


Figure VI-5C. CD4051 Manufacturer Specification Sheet (Continued)

CD4051B, CD4052B, CD4053B Types

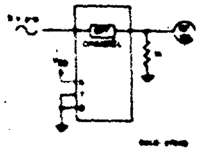


Fig.24 - Feedthrough test (all types)

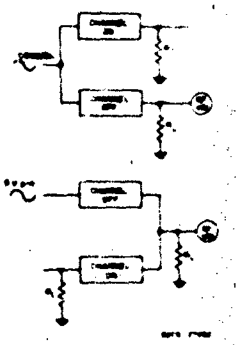


Fig.25 - Crosstalk between any two channels (all types)

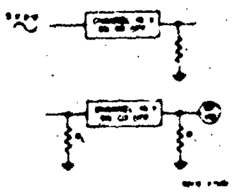


Fig.26 - Crosstalk between duals or triplets (CD4052, CD4053)

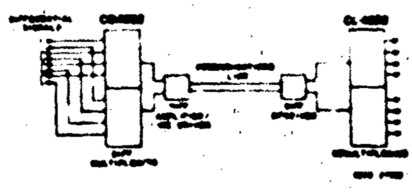


Fig.27 - Typical time-division application of the CD4052

SPECIAL CONSIDERATIONS

In applications where separate power sources are used to drive VDD and the signal inputs, the VDD current capability should exceed VDD/RL (RL = effective external load). This provision avoids permanent current flow or clamp action on the VDD supply when power is applied or removed from the CD4051, CD4052, or CD4053.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned ON or OFF by an address input, there is a momentary conductive path from the channel to VEE, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning ON a channel will similarly dump some charge to VEE.

The amount of charge dumped is mostly a function of the signal level above VEE. Typically, at VDD-VEE = 10 V, a 100 pF capacitor connected to the input or output of the channel will lose 3-4 % of its voltage at the moment the channel turns ON or OFF. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 µs. When the inhibit signal turns a channel OFF, there is no charge dumping to VEE. Rather, there is a slight rise in the channel voltage level ([illegible] mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

Figure VI-50. CD4051 Manufacturer Specification Sheet (Concluded)

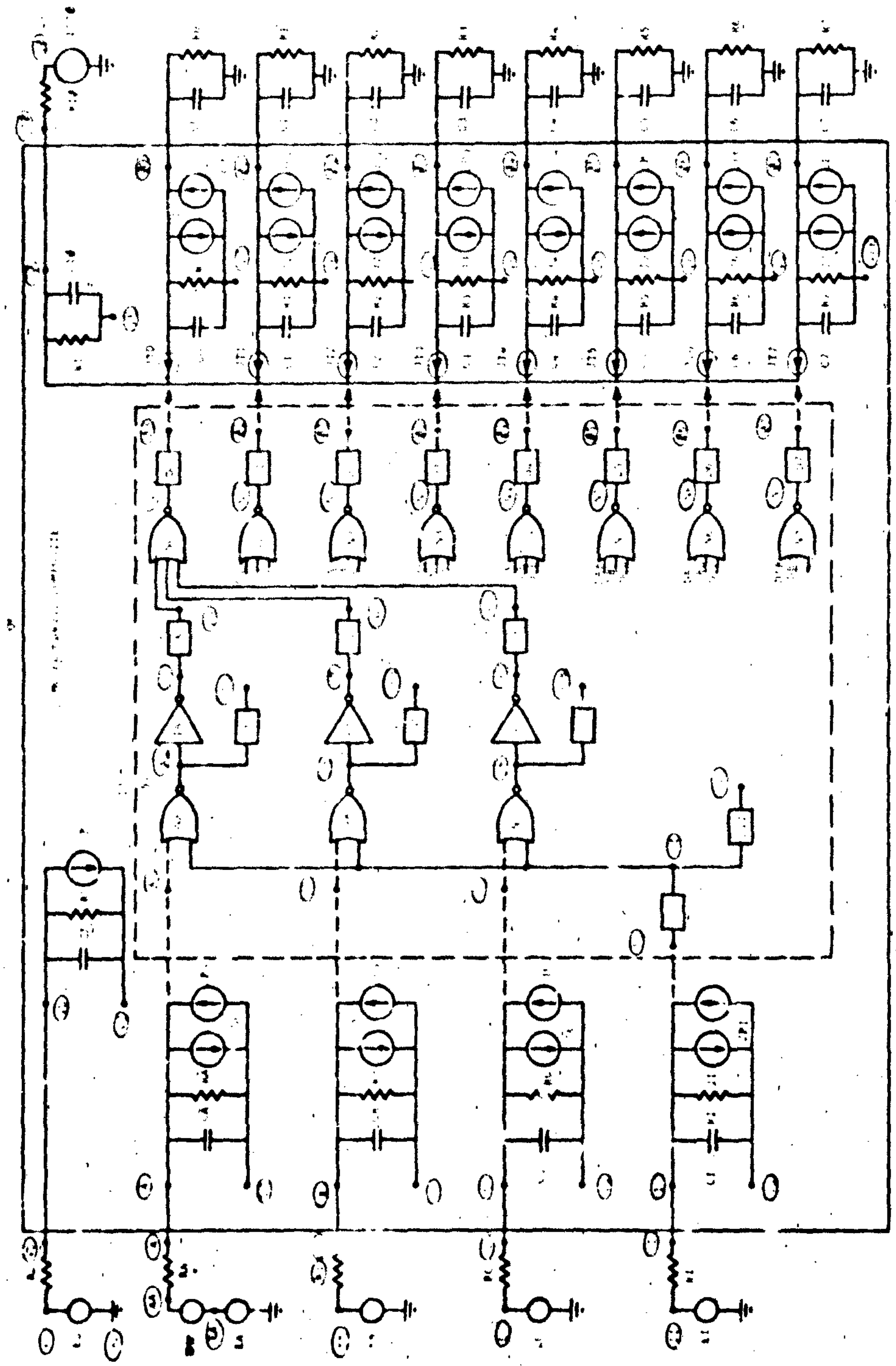


Figure VI-51. Schematic of CD4051 Composite Model

```
SUBPROGRAM
      FUNCTION FBURN(AD,TIME,PAVE,PFAIL,I,V,TE,A,B)
C     THIS SUBROUTINE MONITORS POWER IN A JUNCTION AND FLAGS FAILURE.
C     FAILURE IS DEFINED BY P=AT**(-B)  USING AVERAGE POWER.
C     PAVE = AVERAGE POWER,   PFAIL = FAILURE POWER,  FBURN = PAVE/PFAIL
C     I,V,A,B  SHOULD ALL REFER TO JUNCTION VALUES OR OVERALL VALUES-
C     I,V,A,B  MAY REFER TO EITHER FORWARD OR REVERSE POLARITIES.
C      V= VOLTAGE,  I= CURRENT
C     A,B ARE CONSTANTS IN THE FAILURE POWER VERSES TIME RELATIONSHIP.  CONSIEMP
      REAL I                                                            CONSIEMP
C     AD IS INTEGER IDENTIFYING JUNCTION AND POLARITY TO BE EVALUATED.
      DIMENSION OLDP(20),OLDT(20),OLDE(20),OLDF(20)
      MAXMOD = 20
C     TO INCREASE NUMBER OF BURNOUT MODELS AVAILABLE,
C     INCREASE ALL DIMENSIONS AND MAXMOD EQUALLY.
C     THIS MODEL ASSUMES P=AT**(-B) FOR 0..LT.T-TE.LT.TMAX              CONSIEMP
      TMAX = 500.E-6
      P = I*V
C     FR IS THE RATIO OF AVERAGE POWER/FAILUER POWER DEFINED AS FAILURE
      FR = 1.
      ID = INT(AD)
      IF((ID.GT.MAXMOD).OR.(ID.LT.1))   GO TO 10
      IF(TIME.LE.TE)  GO TO 20
      IF(TIME.LT.OLDT(ID))  GO TO 30
      IF(TIME.GT.TMAX)  GO TO 20
C     TRANSIENT HAS STARTED AND
C     POINT AT TIME = OLDT WAS ACCEPTED BY ERROR CRITERIA.
      OLDE(ID) = OLDE(ID) + (P +OLDP(ID))*(TIME-OLDT(ID))/2.
      PAVE = OLDE(ID)/(TIME-TE)
      PFAIL = A*(AMAX1(TIME-TE,0.)**(-B))                               CONSIEMP
      FBURN = PAVE/PFAIL
      IF(OLDF(ID).GT.FR)  GO TO 5
      IF(FBURN.GT.FR)  PRINT 100,ID,TIME,PAVE,PFAIL
      OLDF(ID) = FBURN
    5 CONTINUE
      OLDP(ID) = I*V
      OLDT(ID) = TIME
      RETURN
C     BURNOUT MODEL IDENTIFIER OUT OF RANGE
 10   PAVE = 0.
      PFAIL = 0.
      FBURN = 0.
      PRINT 200,ID
      RETURN
C     TRANSIENT HAS NOT STARTED,
C     OR TIME EXCEEDS VALID INTERVAL FOR P=K/SQRT(T).
 20   OLDP(ID) = 0.
      OLDT(ID) = TE
      OLDE(ID) = 0.
      PFAIL = 0.
      PAVE = 0.
      OLDF(ID) = 0.
      FBURN = 0.
      RETURN
 30   PRINT 300
      STOP
  100 FORMAT(A(/),10X,*ID =*,I5,5X,*FAILURE TIME =*,E17.7,5X,
    1 *AVERAGE POWER =*,E13.3,5X,*THRESHOLD FAILURE POWER =*,E13.3)
  200 FORMAT(10X,*BURNOUT MODEL IDENTIFIER OUT OF RANGE.  ID =*,I5)
  300 FORMAT(10X,*INVALID RESUTLS FROM DAMAGE MODEL*,/,10X,
    1  *RUN TERMINATED.*,/,10X,*RESULTS OF DAMAGE MODEL MAYBE USED *,
    2  *ONLY IN THE OUTPUTS SECTION.*)
```

Figure VI-52. CD4051 Composite Model Listing

```
      END
**SUBPROGRAM
      FUNCTION   FGEN(T,TP,VMAX,VMIN,TRS,TRM,TFS,TFM)
      TN = T/TP
    5 IF (TN.LT.1.0) GO TO 10
      TN = TN - 1.
      GO TO 5
   10 IF ((TN.LE.TRM).AND.(TN.GT.TRS)) GO TO 20
      IF ((TN.LT.TFM).AND.(TN.GE.TFS)) GO TO 30
      FGEN = VMIN
      IF ((TN.LT.TFS).AND.(TN.GT.TRM)) FGEN = VMAX
      RETURN
   20 FGEN = VMIN + (VMAX-VMIN)*(TN-TRS)/(TRM-TRS)
      RETURN
   30 FGEN = VMAX - (VMAX-VMIN)*(TN-TFS)/(TFM-TFS)
      RETURN
      END
MODEL DESCRIPTION

   MODEL CD4051 COMPOSITE(A-B-C-I-VD-VS-VE-CO-00-01-02-03-04-05-06-07)
       ELEMENTS
             CP,VD -VE = 150.E-12
             RP,VD -VE = 6.67E9
             JP,VD -VE = TABLE VP(VJP)
             CA,A  -VS =  .466E-12                                 COM51
             RA,A  -VS = 1.E12                                     COM51
             JA,A  -VS = TABLE VI(VJA)                             COM51
             JPA,VS -A = Q JP(PGD,2.81E-5,PX1,PX2)                 COM51IPP
             CB,B  -VS =  .466E-12                                 COM51
             RB,B  -VS = 1.E12                                     COM51
             JB,B  -VS = TABLE VI(VJB)                             COM51
             JPB,VS -B = Q JP(PGD,2.81E-5,PX1,PX2)                 COM51IPP
             CC,C  -VS =  .466E-12                                 COM51
             RC,C  -VS = 1.E12                                     COM51
             JC,C  -VS = TABLE VI(VJC)                             COM51
             JPC,VS -C = Q JP(PGD,2.81E-5,PX1,PX2)                 COM51IPP
             CI,I  -VS =  .466E-12                                 COM51
             RI,I  -VS = 1.E12                                     COM51
             JI,I  -VS = TABLE VI(VJI)                             COM51
             JPI,VS -I = Q JP(PGD,2.81E-5,PX1,PX2)                 COM51IPP
             CIO,CO -VE = 35.1E-12                                 COM51
             RIO,CO -VE = 1.E12                                    COM51
             C0 ,00 -VE = 5.32E-12                                 COM51
             R0 ,00 -VE = 1.E12                                    COM51
             JT0,00 -CO =  Q 1J(VCIO,VC0,1.,VCA,VCB,VCC,VCI,4.5)   COM51
             J0 ,00 -VE =  TABLE VO(VJ0)                           COM51
             JP0,VE -00 = Q TR(PPD,VC0,0.,15.E3,120.,0.)           COM51IPP
             C1 ,01 -VE = 5.32E-12                                 COM51
             R1 ,01 -VE = 1.E12                                    COM51
             JT1,01 -CO =  Q 1J(VCIO,VC1,1.,JT0,0.,0.,0.,0.)       COM51
             J1 ,01 -VE =  TABLE VO(VJ1)                           COM51
             JP1,VE -01 = Q TR(PPD,VC1,0.,15.E3,120.,0.)           COM51IPP
             C2 ,02 -VE = 5.32E-12                                 COM51
             R2 ,02 -VE = 1.E12                                    COM51
             JT2,02 -CO =  Q 1J(VCIO,VC2,1.,JT1,0.,0.,0.,0.)       COM51
             J2 ,02 -VE =  TABLE VO(VJ2)                           COM51
             JP2,VE -02 = Q TR(PPD,VC2,0.,15.E3,120.,0.)           COM51IPP
             C3 ,03 -VE = 5.32E-12                                 COM51
             R3 ,03 -VE = 1.E12                                    COM51
             JT3,03 -CO =  Q 1J(VCIO,VC3,1.,JT2,0.,0.,0.,0.)       COM51
             J3 ,03 -VE =  TABLE VO(VJ3)                           COM51
             JP3,VE -03 = Q TR(PPD,VC3,0.,15.E3,120.,0.)           COM51IPP
             C4 ,04 -VE = 5.32E-12                                 COM51
             R4 ,04 -VE = 1.E12                                    COM51
             JT4,04 -CO =  Q 1J(VCIO,VC4,1.,JT3,0.,0.,0.,0.)       COM51
             J4 ,04 -VE =  TABLE VO(VJ4)                           COM51
```

Figure VI-52. CD4051 Composite Model Listing (Continued)

```
        JP4,VE -04 = Q TR(PPO,VC4,0.,15.E3,120.,0.)                 CONSIIPP
        C5 ,05 -VE = 5.32E-12                                         CONSI
        R5 ,05 -VE = 1.E12                                            CONSI
        JT5,05 -CO =  Q 1J(VCIO,VC5,1.,JT4,0.,0.,0.,0.)               CONSI
        J5 ,05 -VE =  TABLE VO(VJ5)                                   CONSI
        JP5,VE -05 = Q TR(PPO,VC5,0.,15.E3,120.,0.)                   CONSIIPP
        C6 ,06 -VE = 5.32E-12                                         CONSI
        R6 ,06 -VE = 1.E12                                            CONSI
        JT6,06 -CO =  Q 1J(VCIO,VC6,1.,JT5,0.,0.,0.,0.)               CONSI
        J6 ,06 -VE =  TABLE VO(VJ6)                                   CONSI
        JP6,VE -06 = Q TR(PPO,VC6,0.,15.E3,120.,0.)                   CONSIIPP
        C7 ,07 -VE = 5.32E-12                                         CONSI
        R7 ,07 -VE = 1.E12                                            CONSI
        JT7,07 -CO =  Q 1J(VCIO,VC7,1.,JT6,0.,0.,0.,0.)               CONSI
        J7 ,07 -VE =  TABLE VO(VJ7)                                   CONSI
        JP7,VE  07 = Q TR(PPO,VC7,0.,15.E3,120.,0.)                   CONSIIPP

    DEFINED PARAMETERS
        PGD=0.                                                        CONSIIPP
        PIP = .5E-6
        PTP = .525E-6
        PT1 = Q 1T(TIME,PIP,2.E-7)                                    CONSIIPP
        PT2 = Q 1T(TIME,PTP,2.E-7)                                    CONSIIPP
        PX1 = Q 1X(7.8E-5,2.49E-3,PT1)                                CONSIIPP
        PX2 = Q 1X(7.8E-5,2.49E-3,PT2)                                CONSIIPP
        PPO= Q JP(PGD,10.,6E-5,PX1,PX2)                               CONSIIPP
        PA = 0.                                                       CONSIEMP
        PF = 0.                                                       CONSIEMP
        PIF= X 1(AMAX1(JA,0.))                                            CONS
        PIR= X 2(AMIN1( J5,0.) )
        PUF= F4URN(1.,TIME,PA,PF,V A,PIF,0.,5.2 ,.243)                CONSIEM
        PUR= F4URN(2.,TIME,PA,PF,V,A,PIR,0.,.334,.243)                CONSIEM
    FUNCTIONS
        TABLE VF = -11.,-1.23, -1.,0., 11.,0., 21.,.617
        TABLE VI =  -162.,-.098, 0.,0., 10.,1., 20.,.59               CONSI
        TABLE VO = -10.,-.343, 0.,0., 10.,0., 20.,1.                  CONSI
        Q 1J(V2,VC,AD,A,B,C,I,VT)=((VC-VO)/(200SI(AD,A,B,C,I,VT)) CONSI
        Q 1T(T,TP,TAU)=(AMIN1(SQRT(AMAX1((T-TP)/TAU,0.)),1.))       CONSIIPP
        Q 1X(A,D,X) = (A*D*(1.-(1.+.27A+9)*X+.23D*A*X*X+.0009*3*CONSIIPP
       X*X*X-.07A1D8*X*X*X*X)*E(-X))*AMIN1(1.,AMAX1(0.,1.-20*X)))CONSIIPP
        Q JP(GAMAP,A,D,X1,X2) = (GAMAP*A*D*6.E-6*(X1-X2))            CONSIIPP
       Q TR(APP,VO,V,R,B,C)=(AMAX1((-.6-VO-V)/R*APP1*B,0.)*C*APP)CONSIIP

LOGIC DESCRIPTION
    LOGIC FCLOS1 (A-B-C-I-VT)
        LOGIC ELEMENTS
            D1 ,D1 -IL    (87.7E-9,78.0E-9)                          CONSIR=0
            D11,D11-D1    (314.E-9,253.E-9)                          CONSIR=0
            NA ,AB -D1 -A
            IA ,A  -AN
            DA ,DA -A  = (314.E-9,253.E-9)                           CONSIR=0
            DAB,DAB-AB = (314.E-9,253.E-9)                           CONSIR=0
            N1 ,BL -D1 -BL
            IB ,B  -BB
            DB ,DB -B  = (314.E-9,253.E-9)                           CONSIR=0
            DBB,DBB-BB = (314.E-9,253.E-9)                           CONSIR=0
            NC ,CB -D1 -CL
            IC ,C  -CB
            DC ,DC -C  = (314.E-9,253.E-9)                           CONSIR=0
            DCB,DCB-CB = (314.E-9,253.E-9)
            N0 ,N0 -DA -DB -DC
            D0 ,D0 -N0 = (99.6E-9,53.0E-9)                           CONSIR=0
            N1 ,N1 -DAB-DB -DC
            D1 ,D1 -N1 = (99.6E-9,53.0E-9)                           CONSIR=0
            N2 ,N2 -DA -DBB-DC
            D2 ,D2 -N2 = (99.6E-9,53.0E-9)                           CONSIR=0
            N3 ,N3 -DAB-DBB-DC
            D3 ,D3 -N3 = (99.6E-9,53.0E-9)                           CONSIR=0
            N4 ,N4 -DA -DB -DCB
            D4 ,D4 -N4 = (99.6E-9,53.0E-9)                           CONSIR=0
            N5 ,N5 -DAB-DB -DCB
            D5 ,D5 -N5 = (99.6E-9,53.0E-9)                           CONSIR=0
            N6 ,N6 -DA -DBB-DCB
            D6 ,D6 -N6 = (99.6E-9,53.0E-9)                           CONSIR=0
            N7 ,N7 -DAB-DBB-DCB-D11
            D7 ,D7 -N7 = (99.6E-9,53.0E-9)                           CONSIR=0
```

Figure VI-52. CD4051 Composite Model Listing (Continued)

```
          LOGIC INPUTS
               AL= A.GT.VT
               BL= B.GT.VT
               CL= C.GT.VT
               IL= I.GT.VT
          LOGIC OUTPUTS
               00 = 500.E6.145.
               01 = 500.E6.145.                                        COMS1R=0
               02 = 500.E6.145.                                        COMS1R=0
               03 = 500.E6.145.                                        COMS1R=0
               04 = 500.E6.145.                                        COMS1R=0
               05 = 500.E5.145.                                        COMS1R=0
               06 = 500.E6.145.                                        COMS1R=0
               07 = 50(.E6.145.                                        COMS1R=0
CIRCUIT DESCRIPTION                                                    COMS1R=0
CD4051  8 CHANNEL MULTIPLEXE/DEMULTPLEXER      COMPOSITE MODEL
ELECTRICAL PULSE OVERSTRESS                                            COMS1SEA
    ELEMENTS                                                           COMS1EMP
        ED.GRD-ED = 10.
        RD.ED -VD = 50.                                                COMS1
        EA.GRD-EA = 10.                                                COMS1
        EMP.EA -AA = PEMP                                              COMS1
        RA.AA - A = 50.                                                COMS1
        EB.GRD- BB= 0.                                                 COMS1
        RB.BB - B = 50.                                                COMS1
        EC.GRD- CC= 0.                                                 COMS1
        RC.CC - C = 50.                                                COMS1
        EI.GRD- II= 0.                                                 COMS1
        RI.II - I = 50.                                                COMS1
        ECIO.GRD-IO = 2.5                                              COMS1
        RIO.IO-CIO= 50.                                                COMS1
        XM.A-B-C-I-VD-GRD-GRD-CIO-00-01-02-03-04-05-06-07=             COMS1
        MODEL CD4051 COMPOSITE                                         COMS1
        C0.00 -GRD= 100.E-12
        R0.00 -GRD= 2.E3                                               COMS1
        C1.01 -GRD= 100.E-12                                           COMS1
        R1.01 -GRD= 2.E3                                               COMS1
        C2.02 -GRD= 100.E-12                                           COMS1
        R2.02 -GRD= 2.E3                                               COMS1
        C3.03 -GRD= 100.E-12                                           COMS1
        R3.03 -GRD= 2.E3                                               COMS1
        C4.04 -GRD= 100.E-12                                           COMS1
        R4.04 -GRD= 2.E3                                               COMS1
        C5.05 -GRD= 100.E-12                                           COMS1
        R5.05 -GRD= 2.E3                                               COMS1
        C6.06 -GRD= 100.E-12                                           COMS1
        R6.06 -GRD= 2.E3                                               COMS1
        C7.07 -GRD= 100.E-12                                           COMS1
        R7.07 -GRD= 2.E3                                               COMS1
  DEFINED PARAMETERS                                                   COMS1
        PEMP = 200.                                                    COMS1
  FUNCTIONS
        TABLE 1E = -1.,10., .1E-6,10., .2E-6,0.,  1.,0.
        TABLE 2E = -10,0.,  .1E-6,0.,  .2E-6,10., 1.,10.               COMS1
        TABLE IE = -1.,0.,  1.E-6,0.,  1.1E-6,10., 1.8E-6,10.,         COMS1
                                                                       COMS1
                       1.9E-6,0., 1.,0.
  INITIAL CONDITIONS                                                   COMS1
        VCPXM = 10.
        VCAXM =  10.
        VCIOXM=  2.5
        VCI   = 2.28
        VCIXM= 2.28
  OUTPUTS
        VCAXM.PLOT
        IRA.PLOT
  RUN CONTROLS
        TERMINATE IF(PUFXM.GT.1.)
        TERMINATE IF(PURXM.GT.1.)
        INTEGRATION ROUTINE = IMPLICIT                                   GTD
        STOP TIME = 10.E-6
END                                                                      EMP
```

Figure VI-52. CD4051 Composite Model Listing (Concluded)

Two important techniques are demonstrated in the I/V portion of the composite model. They deal with the implementation of the EMP burnout model and the photoresponse model. Predictions could be made of the EMP failure thresholds for input, output, and power supply terminals based on relatively complex models of the PN junctions and MOS devices connected to each of the terminals. Such models are too complex to be consistent with the composite modeling concept which stresses a limited number of elements and simpler functional forms. Also, the goal of the composite model is to simulate terminal performance rather then to predict failure characteristics. To simplify the modeling of EMP effects, an empirical model can be constructed directly from experimental test data using techniques discussed earlier in this chapter.

The correct current and voltage response of the terminals in breakdown can be simulated using a diode table as shown in figure VI-43. When the element described by the diode table is pulsed with an EMP signal, it will exhibit the proper terminal I/V characteristics and, hence, the proper terminal power. The terminal power can then be used in a modified FBURN subroutine to indicate the terminal failure threshold. The modification to the FBURN subroutine involves replacing the functional form

$$P = Kt^{-1/2}$$

with the form

$$P = At^{-B} .$$

The required charge is shown in the listing of FBURN in figure VI-52. The elements JA, JB, JC, and JI represent the EMP diode elements for the CD4051 inputs. The elements J0 through J7 represent the diode elements for the output.

Both experimental and detailed analyses show that the photoresponse of CMOS multiplexer outputs can be significantly influenced by the secondary photocurrent produced by the parasitic NPN transistor associated with the NMOS device in the transmission gate. The detailed models successfully predict this influence but require an Ebers-Moll model of the parasitic transistor. Such a procedure is not consistent with the composite model goals. However, reexamination of the problem indicates a method for including the secondary photocurrent effects without a complete parasitic transistor model.

Consider the diagram of the parasitic transistor in figure VI-53. The secondary photocurrent will not be produced until the voltage drop in the bulk resistance, R, exceeds the reverse bias across the emitter base junction plus the 0.6V turn-on threshold. Therefore, the minimum amount of photocurrent which must flow before the secondary photocurrent is generated is:

$$I_{PP} = \frac{V + V_o + 0.6}{R}$$

where I_{PP}, V, V_o, R are defined in figure VI-53. The amount of secondary photocurrent can be calculated from the expression

$$I_{SP} = I_{PP} - \left(\frac{V + V_o + 0.6}{R} \right) \beta$$

where:

I_{SP} = secondary photocurrent
β = common emitter current gain

If there is not enough primary photocurrent to produce a secondary photocurrent, the I_{SP} equation must be limited to zero and provision made for the primary photocurrent or a fraction thereof to flow out of the terminal. Equation QTR in the SCEPTRE model listing implements the technique

described above. The procedure provides a means for automatically reflecting the influence of secondary photocurrent over a wide range of dose rates without unnecessary elements.

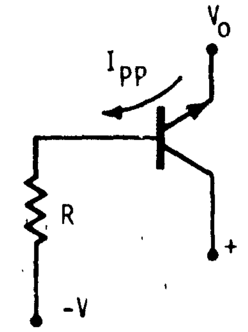


Figure VI-53. Parasitic Transistor Schematic for Simplified Secondary Photocurrent Model Development

The results of exercising the composite model of the CD4051 are shown in figures VI-54 through VI-56. Figure VI-54 shows the results of cycling through the multiplexer channels (channels 0, 4, and 7 are shown) and demonstrates the electrical operation of the model. The output of channel 7 is terminated by an inhibit signal. Note the glitches occurring on channel 7 as other channels are selected. These are the result of propagation delay variations in the circuitry. They are also observable in electrical measurements on the CD4051. Figures VI-55 and VI-56 show the output photoresponse simulations for low and high state outputs, respectively. They demonstrate the utility of the secondary photocurrent model developed above.

Further examples of the application of composite modeling are given in example 5 of chapter VII.

D. REFERENCES

VI-1. Pocock, D. N., et al. "Simplified Microcircuit Modeling," AFWL-TR-73-273, March 1974.

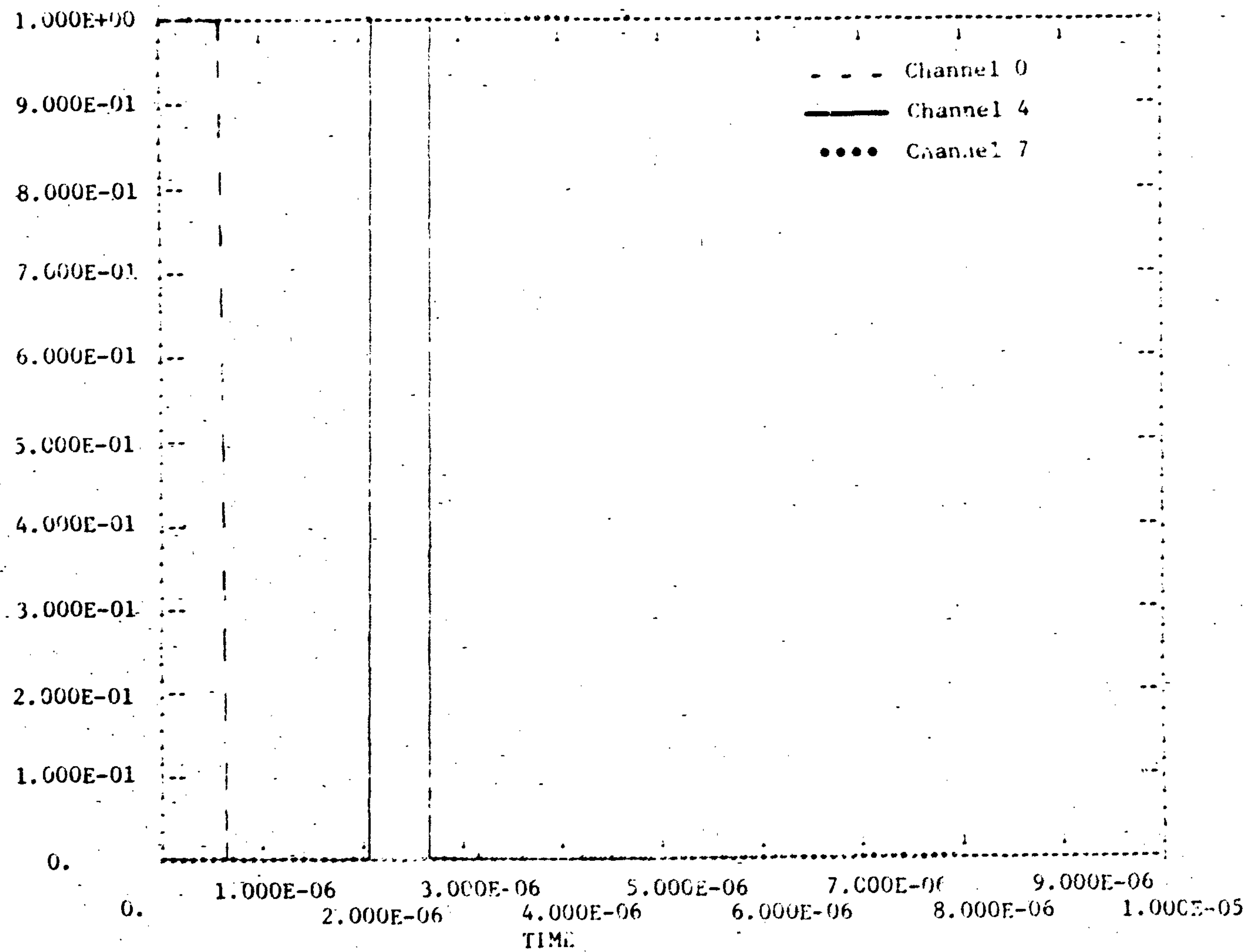


Figure VI-54. Composite CD4051 Model Output Selection - Channels 0, 4, and 7

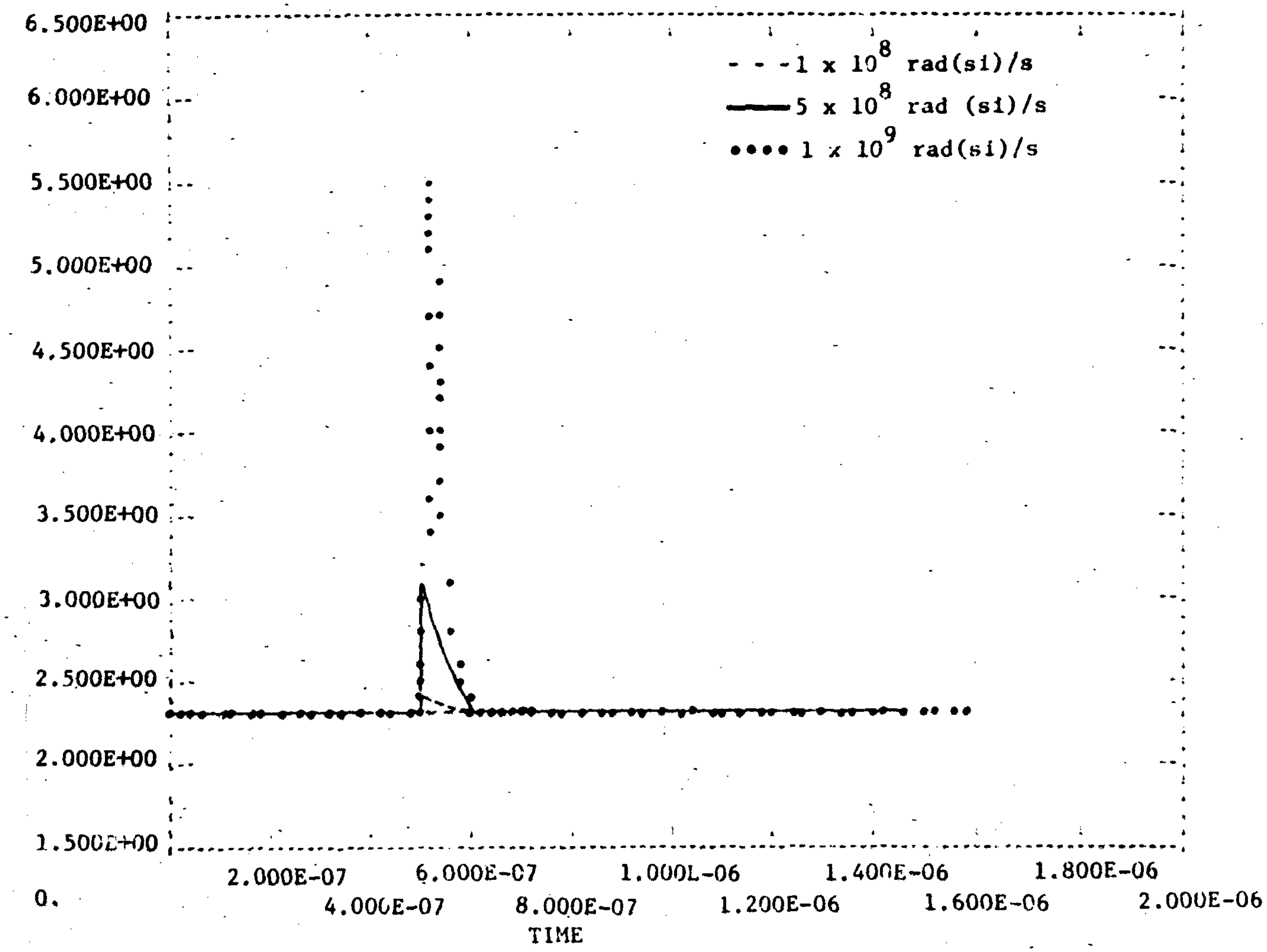


Figure VI-55. - Composite Model Simulation of CD4051 Photoresponse-High State Output

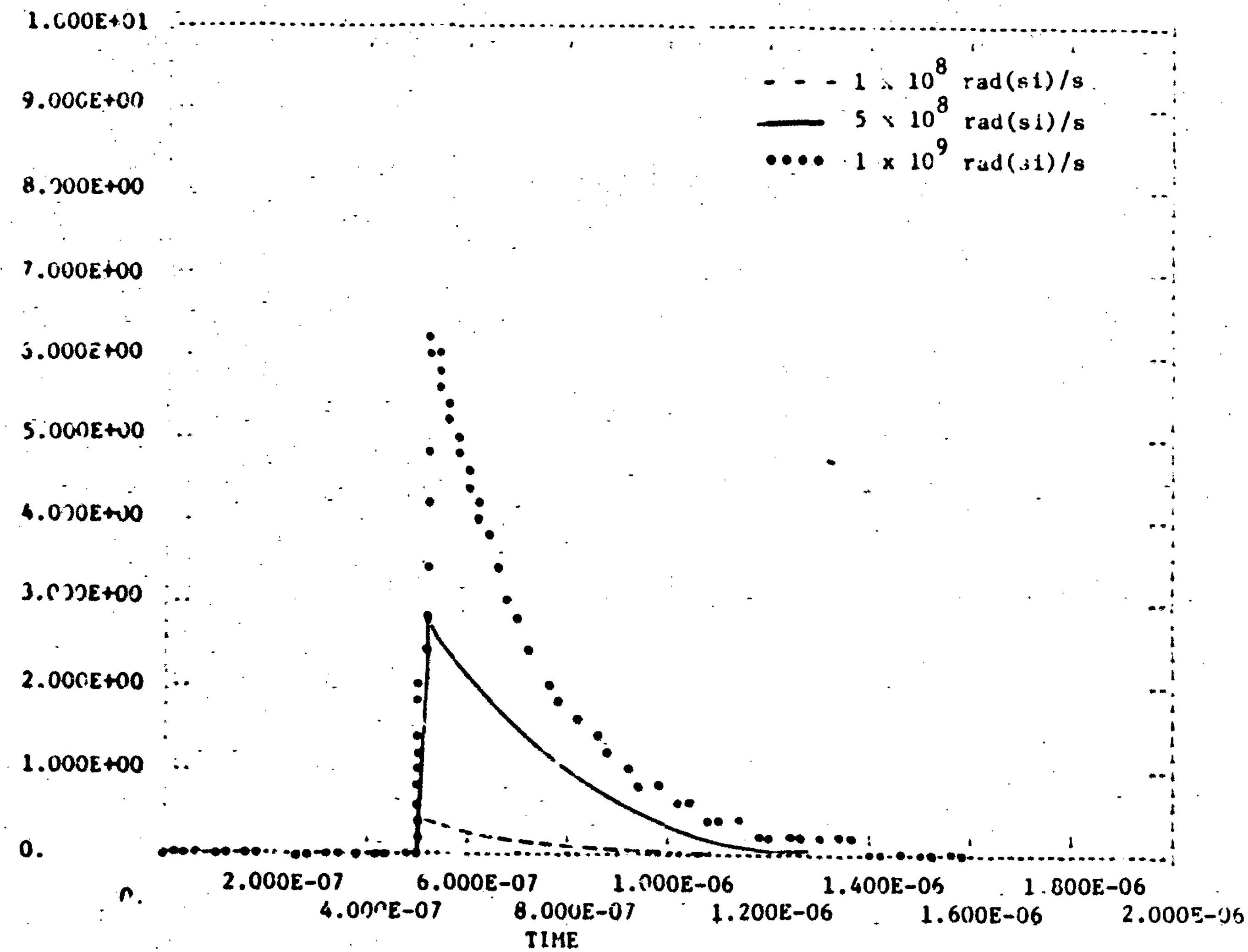


Figure VI-56. Composite Model Simulation of CD4051 Photoresponse - Low State Output

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VI-10. Jenkins, C. R and D. L. Durgin. "EMP Susceptibility of Integrated Circuits," IEEE Trans. Nuclear Science, December 1975.

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VI-13. The Integrated Circuits Catalog for Design Engineers, Texas Instruments Incorporated.

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CHAPTER VII

EXAMPLES

CHAPTER VII

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CHAPTER VII

EXAMPLES

A. ILLUSTRATION OF THE EFFECTS OF NEUTRON DEGRADATION, DOSE RATE INDUCED UPSET, AND EMP INDUCED BURNOUT ON DISCRETE AND INTEGRATED LOGIC CIRCUITS

This example is a study of the interface latch circuit shown in figure VII-1. This circuit is representative of a number of circuits commonly seen in S/V (survivability/vulnerability) analysis. The interface latch circuit interfaces 10-volt logic signals into signals compatible with low power TTL logic.

The model interface latch circuit is a combination of a basic transistor model and a simplified digital logic model. Both of these models were demonstrated as examples in this handbook.

The first example run was intended to verify the electrical behavior of the latch. The signal sequence used to test the behavior of the latch is shown in figure VII-2. The desired behavior of the "OUT" node was observed. Figure VII-3 is the listing and output for this run.

What is the radiation response of this circuit? Computer simulations will give much insight into this problem. Before simulations are to be made, the analyst must decide what possibilities are important and what effects need to be considered.

For the latch circuit, an electromagnetic pulse may travel from any external pin to the circuit and produce failure. The analyst must decide which pins are to be analyzed as potential hazards.

Ionizing radiation will affect the two TTL gates and produce a primary photocurrent in the 2N2222A. The analyst must first decide if upset is a possibility and which components need be considered as upset possibilities.

Neutron radiation will degrade the performance of the semiconductor components. Again, the analyst must decide what effects need to be

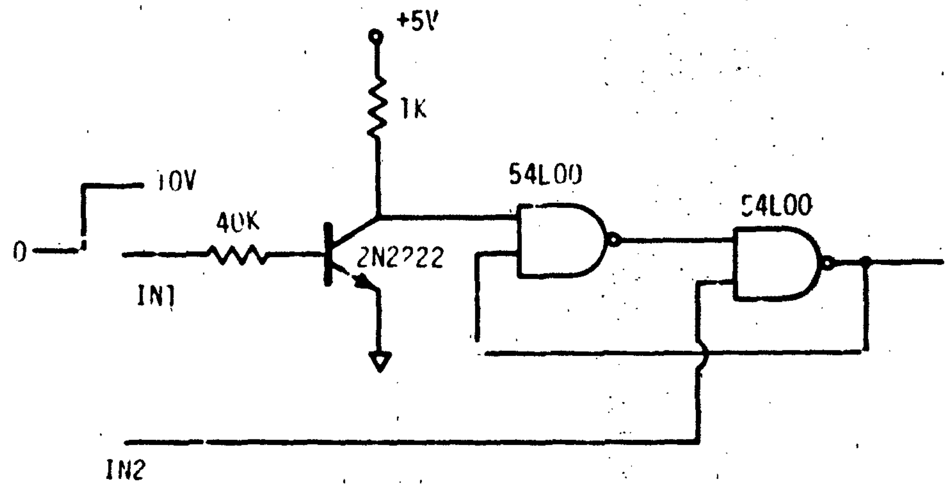

Figure VII-1. Interface Latch Circuit

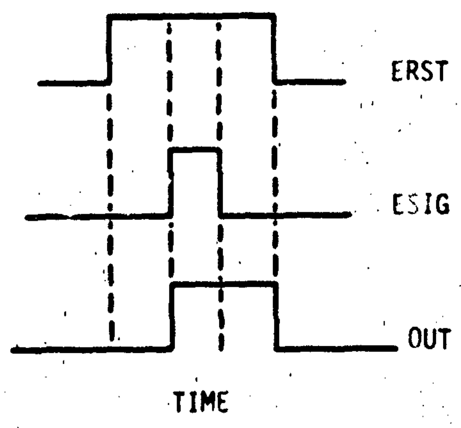

Figure VII-2. Timing Sequence of Model Voltage Signals

```
S C E P T R E    NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2       5/76
 03/17/78     18.12.04.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD  "DOCUMENT"  AS THE FIRST CARD
OF THE INPUT TEXT


COMPUTER TIME ENTERING SETUP PHASE-
          CPA        .355 SEC.
          PP        0.000 SEC.
          IO        0.000 SEC.


SUBPROGRAM
      FUNCTION FBURN(AD,TIME,PAVE,PFAIL,I,V,TE,A,B)
C     THIS SUBROUTINE MONITORS POWER IN A JUNCTION AND FLAGS FAILURE.
C     FAILURE IS DEFINED BY P=AT**(-B) USING AVERAGE POWER.
C     PAVE = AVERAGE POWER, PFAIL = FAILURE POWER, FBURN = PAVE/PFAIL
C     I,V,A,B SHOULD ALL REFER TO JUNCTION VALUES OR OVERALL VALUES.
C     I,V,A,B MAY REFER TO EITHER FORWARD OR REVERSE POLARITIES.
C      V= VOLTAGE, I= CURRENT
C     A,B ARE CONSTANTS IN THE FAILURE POWER VERSES TIME RELATIONSHIP.
      REAL I
C     AD IS INTEGER IDENTIFYING JUNCTION AND POLARITY TO BE EVALUATED.
      DIMENSION OLDP(20),OLDT(20),OLDE(20),OLDF(20)
      MAXMOD = 20
C     TO INCREASE NUMBER OF BURNOUT MODELS AVAILABLE,
C     INCREASE ALL DIMENSIONS AND MAXMOD EQUALLY.
C     THIS MODEL ASSUMES P=AT**(-B) FOR 0..LT.T-TE.LT.TMAX
      TMAX = 500.E-6
      P = I*V
C     FR IS THE RATIO OF AVERAGE POWER/FAILUER POWER DEFINED AS FAILURE
      FR = 1.
      ID = INT(AD)
      IF((ID.GT.MAXMOD).OR.(ID.LT.1)) GO TO 10
      IF(TIME.LE.TE) GO TO 20
      IF(TIME.LT.OLDT(ID)) GO TO 30
      IF(TIME.GT.TMAX) GO TO 20
C     TRANSIENT HAS STARTED AND
C     POINT AT TIME = OLDT WAS ACCEPTED BY ERROR CRITERIA.
      OLDE(ID) = OLDE(ID) + (P+OLDP(ID))*(TIME-OLDT(ID))/2.
      PAVE = OLDE(ID)/(TIME-TE)
      PFAIL = A*(AMAX1(TIME-TE,0.)**(-B))
      FBURN = PAVE/PFAIL
      IF(OLDF(ID).GT.FR) GO TO 5
      IF(FBURN.GT.FR) PRINT 100,ID,TIME,PAVE,PFAIL
      OLDF(ID) = FBURN
    5 CONTINUE
      OLDP(ID) = I*V
      OLDT(ID) = TIME
      RETURN
C     BURNOUT MODEL IDENTIFIER OUT OF RANGE
```

Figure VII-3. Computer Verification of Interface Latch Electrical Behavior

```
   10 PAVE = 0.
      PFAIL = 0.
      FBURN = 0.
      PRINT 200,ID
      RETURN
C     TRANSIENT HAS NOT STARTED.
C     OR TIME EXCEEDS VALID INTERVAL FOR P*R/SQRT(T).
   20 OLDP(ID) = 0.
      OLDT(ID) = TE
      OLDE(ID) = 0.
      PFAIL = 0.
      PAVE = 0.
      OLDF(ID) = 0.
      FBURN = 0.
      RETURN
   30 PRINT 300
  100 FORMAT(6(/),10X,*ID=*,I5,5X,*FAILURE TIME =*,E17.7,5X,
     1 *AVERAGE POWER =*,E12.3,5X,*THRESHOLD FAILURE POWER =*,E13.3)
  200 FORMAT(10X,*BURNOUT MODEL IDENTIFIER OUT OF RANGE.  ID=*,I5)
  300 FORMAT(10X,*INVALID RESULTS FROM DAMAGE MODEL*,/,10X,
     1 *RUN TERMINATED.*,/,10X,*RESULTS OF DAMAGE MODEL MAYBE USED *,
     2 *ONLY IN THE OUTPUTS SECTION.*)
      STOP
      END
CFN2          QUAD 2-INPUT NAND GATE LEVEL SELECT
C     FOR USE WITH 2 INPUT NAND GATE
      FUNCTION FN2(A,B,C,D,E,F)
C     A=VJA B=VJB C=3.8
C     D=3.1 E=1.9 F=0.3
      IF(A.LE.C.OR.B.LE.C)GO TO 4
      IF(A.GE.E.AND.B.GE.E)GO TO 5
      FN2=D-AMIN1(A,B)
      RETURN
    4 FN2=D
      RETURN
    5 FN2=F
      RETURN
      END
C             DIGITAL IC CAPACITOR SELECT
      FUNCTION FCAP1(A,B,C,D)
C     TO ESTABLISH CAPACITOR VALUE OF DIGITAL IC
      FCAP1=C
      IF(A.GE.B)FCAP1=D
      RETURN
      END
MODEL DESCRIPTION
MODEL L00(A-B-OUT-GND)
2 INPUT NAND GATE
A=INPUT A
B=INPUT B
ELEMENTS
JA,A-GND=0.
JB,B-GND=0.
JO,OUT-GND=0.
CO,OUT-GND=1.E-12
E1,GND-1=Q4(VJA,VJB,3.8,3.1,1.9,0.3)
R1,1-2=100.
C1,2-GND=Q2(E1,F2,55.E-12,300.E-12)
E2,GND-3=A1(VC1)
R2,3-OUT=30.
FUNCTIONS
Q2(A,B,C,D)=(FCAP1(A,B,C,D))
Q4(A,B,C,D,E,F)=(FN2(A,B,C,D,E,F))
MODEL 2N2222 (1-2-3)
```

Figure VII-3. Computer Verification of Interface Latch Electrical Behavior (Continued)

```
ELEMENTS
JCC,1-2=X3(3.30E-14*(EXP(38.61*VJE)-1.))
JEC,3-2=X4(3.30E-14*(EXP(38.61*VJC)-1.))
JC,2-1=Q1(JEC,0.398)
JE,2-3=Q1(JCC,0.99567)
CC,1-2=1.E-12
CE,3-2=1.E-12
FUNCTIONS
Q1(A,B)=(A/B)
CIRCUIT DESCRIPTION
ELEMENTS
R1,1-2=40000.
T1,3-2-0=MODEL 2N2222
R2,4-3=1000.
ECC,0-4=5.
NA1,3-6-5-0=MODEL LOD
NA2,5-7-6-0=MODEL LOD
JOUT,6-0=0
ESIG,0-1=TABLE 1(TIME)
ERST,0-7=TABLE 2(TIME)
JB,7-0=0
DEFINED PARAMETERS
PFR=FRURN(1.,TIME,PA,PF,PIR,PVR,PTE,PK,PB)
PA=0
PF=0
PIR=X1(-JB)
PVR=X2(-VJB)
PTE=0.0
PK=0.00216
PB=0.689
FUNCTIONS
TABLE 1
0,0,4.E-3,0,4.1E-3,10,6.E-3,10,6.1E-3,0,1.E-2,0
TABLE 2
0,0,2.E-3,0,2.1E-3,5,8.E-3,5,8.1E-3,0,1.E-2,0
OUTPUTS
ESIG,ERST,VR2,VJOUT,PLOT
RUN CONTROLS
STOP TIME=1.E-2
MAXIMUM INTEGRATION PASSES=5.E4
END

SYSTEM NOW ENTERING SIMULATION


COMPUTER TIME AT TERMINATION OF SETUP PHASE-
         CPA        3.383 SEC.
         PP         0.000 SEC.
         IO         0.000 SEC.
```

Figure VII-3. Computer Verification of Interface Latch Electrical Behavior (Continued)

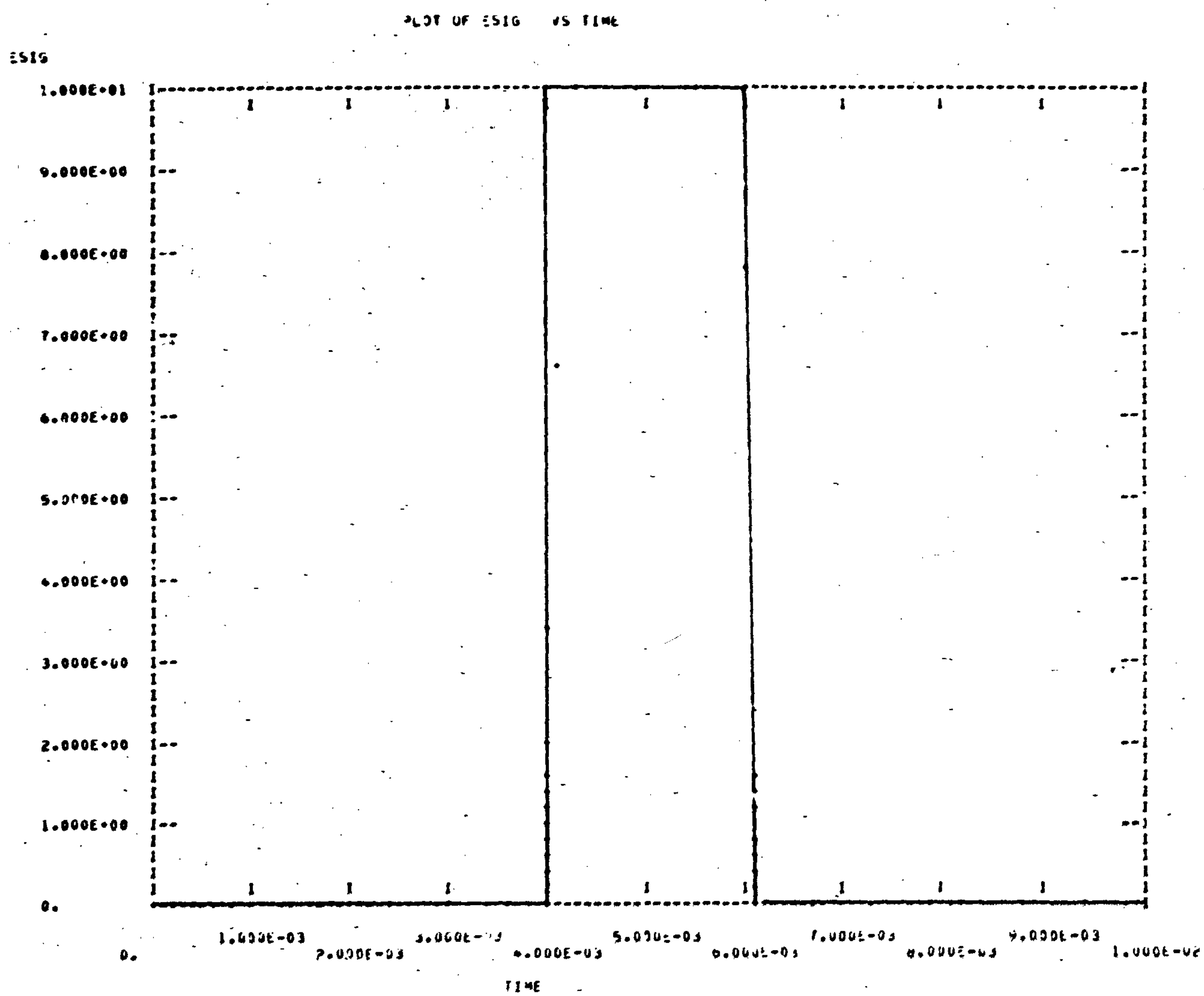

Figure VII-3. Computer Verification of Interface Latch Electrical Behavior (Continued)

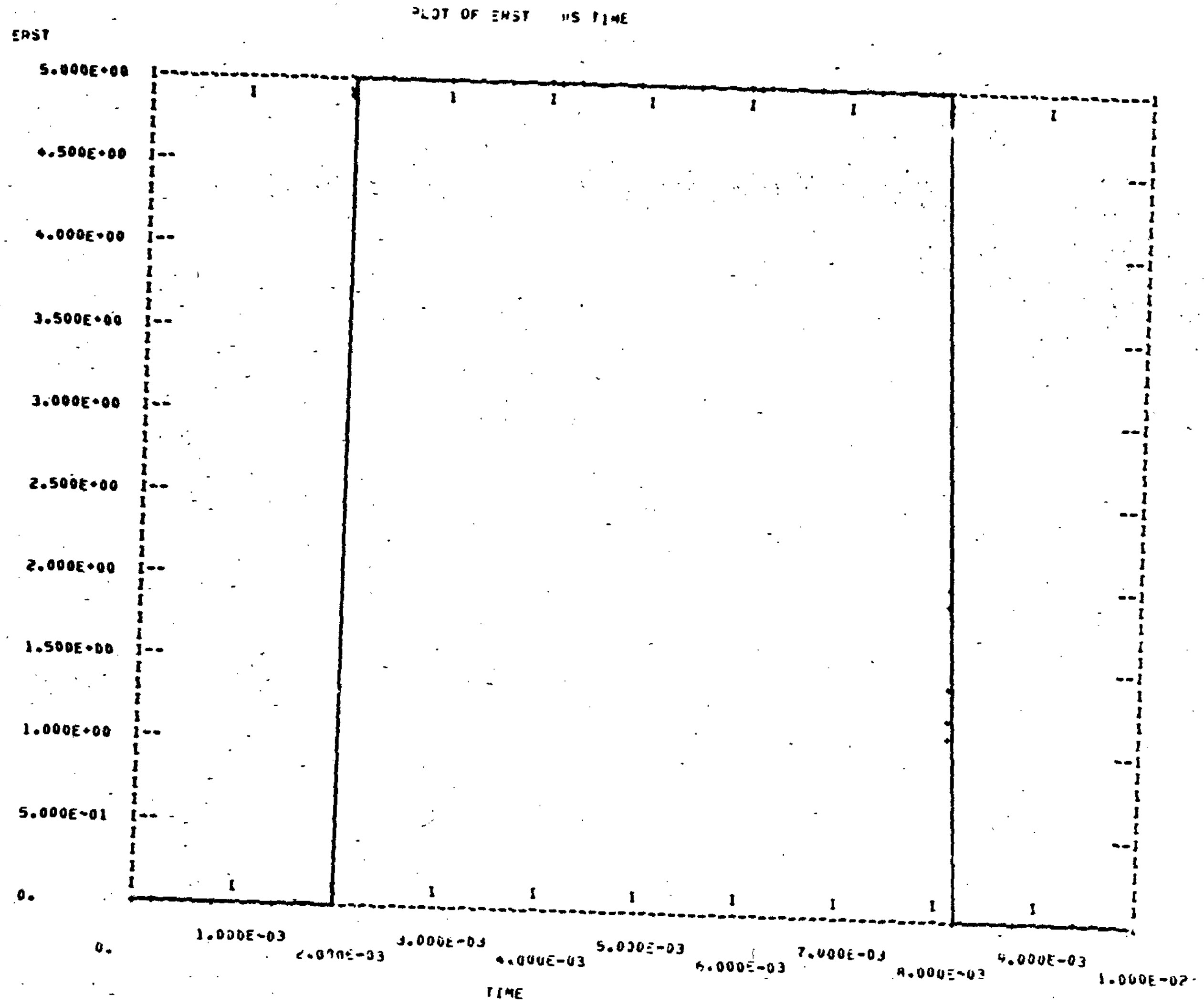

Figure VII-3. Computer Verification of Interface Latch Electrical Behavior (Continued)

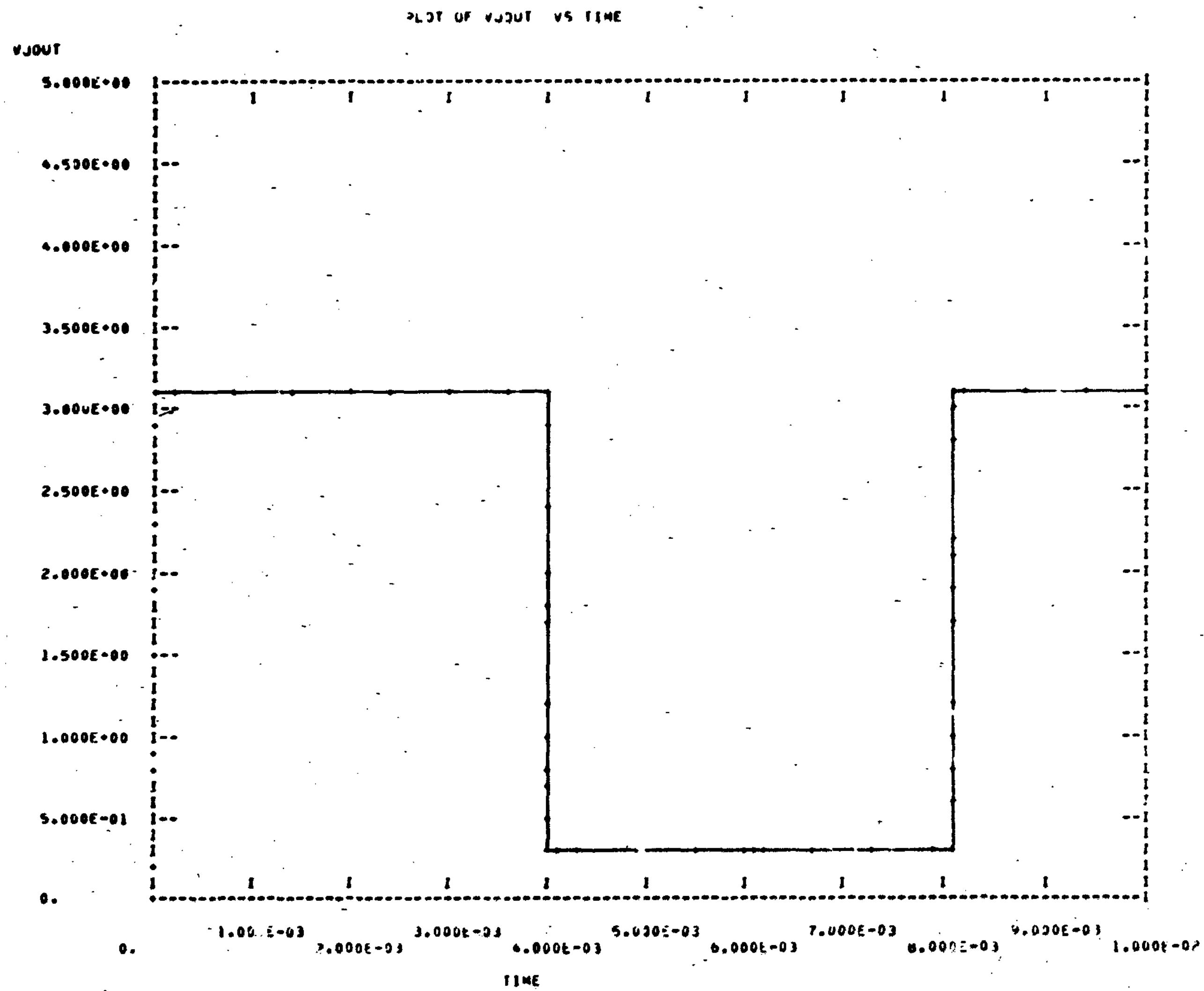

Figure VII-3. Computer Verification of Interface Latch Electrical Behavior (Concluded)

simulated, whether a simulation is even required, and which components are affected in the simulation.

What will happen to the latch when exposed to a neutron fluence of 1×10^{14} n/cm^2? This question may be answered by a computer simulation. The major damaging effect to the 2N2222A transistor will be a degradation in the current gain. An estimation of the amount of degradation can be made from the preirradiation gain and f_T of the model transistor as:

$$\frac{1}{\beta_\phi} = \frac{1}{\beta_o} + \frac{k\phi}{2\pi\ f_T}$$

$$\frac{1}{\beta_\phi} = \frac{1}{230} + \frac{(10^{-6})(1 \times 10^{14})}{2\pi\ (155\ \text{MHz})}$$

$$\beta_\phi = 9.34$$

The next question is how to model damage to the TTL gates? TTL is considered safe from failure at and below 10^{14} n/cm^2. Therefore, behavior modifications to the TTL models are not necessary.

The simulation can now be made. The computer listing is identical except for the modified alpha of the 2N2222A. The results of this simulation predict that the voltage at node OUT will become locked in the high state. The voltage across the collector resistor of the 2N2222A (VR2) was observed to change by slightly over 2 volts which is not sufficient to produce a change in a logic state as 4.2 volts would be required. The listing and output for this simulation is given in figure VII-4.

What if the primary upset mechanism was from gamma radiation at a dose rate level of 1×10^8 rad (Si)/sec? A solution of Notthoff's equations using only data sheet parameters will produce a predicted value of peak photocurrent for the transistor. Again, TTL remains unaffected at this level of radiation intensity.

A solution of Notthoff's equations yields:

```
S C E P T R E   NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2       5/76
 03/17/78     18.18.13.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD  "DOCUMENT"  AS THE FIRST CARD
OF THE INPUT TEXT



COMPUTER TIME ENTERING SETUP PHASE-
          CPA        .371 SEC.
          PP        0.000 SEC.
          IO        0.000 SEC.


SUBPROGRAM
      FUNCTION FBURN(AD,TIME,PAVE,PFAIL,I,V,TE,A,B)
C     THIS SUBROUTINE MONITORS POWER IN A JUNCTION AND FLAGS FAILURE.
C     FAILURE IS DEFINED BY P=AT**(-B) USING AVERAGE POWER.
C     PAVE = AVERAGE POWER. PFSIL = FAILURE POWER. FBURN = PAVE/PFAIL
C     I,V,A,B SHOULD ALL REFER TO JUNCTION VALUES OR OVERALL VALUES.
C     I,V,A,B MAY REFER TO EITHER FORWARD OR REVERSE POLARITIES.
C      V= VOLTAGE, I= CURRENT
C     A,B ARE CONSTANTS IN THE FAILURE POWER VERSES TIME RELATIONSHIP.
      REAL I
C     AD IS INTEGER IDENTIFYING JUNCTION AND POLARITY TO BE EVALUATED.
      DIMENSION OLDP(20),OLDT(20),OLDE(20),OLDF(20)
      MAXMOD = 20
C     TO INCREASE NUMBER OF BURNOUT MODELS AVAILABLE,
C     INCREASE ALL DIMENSIONS AND MAXMOD EQUALLY.
C     THIS MODEL ASSUMES P=AT**(IB) FOR 0..LT.T-TE.LT.TMAX
      TMAX = 500.E-6
      P = I*V
C     FR IS THE RATIO OF AVERAGE POWER/FAILUER POWER DEFINED AS FAILURE
      FR = 1.
      ID = INT(AD)
      IF((ID.GT.MAXMOD).OR.(ID.LT.1)) GO TO 10
      IF(TIME.LE.TE) GO TO 20
      IF(TIME.LT.OLDT(ID)) GO TO 30
      IF(TIME.GT.TMAX) GO TO 20
C     TRANSIENT HAS STARTED AND
C     POINT AT TIME = OLDT WAS ACCEPTED BY ERROR CRITERIA.
      OLDE(ID) = OLDE(ID) + (P+OLDP(ID))*(TIME-OLDT(ID))/2.
      PAVE = OLDE(ID)/(TIME-TE)
      PFAIL = A*(AMAX1(TIME-TE,0.)**(-B))
      FBURN = PAVE/PFAIL
      IF(OLDF(ID).GT.FR) GO TO 5
      IF(FBURN.GT.FR) PRINT 100,ID,TIME,PAVE,PFAIL
      OLDF(ID) = FBURN
    5 CONTINUE
      OLDP(ID) = I*V
      OLDT(ID) = TIME
      RETURN
```

Figure VII-4. Interface Latch Behavior Following Neutron Exposure

```
C      BURNOUT MODEL IDENTIFIER OUT OF RANGE
   10 PAVE = 0.
      PFAIL = 0.
      PBURN = 0.
      PRINT 200,ID
      RETURN
C      TRANSIENT HAS NOT STARTED,
C      OR TIME [illegible] VALID INTERVAL FOR [illegible]
   20 [illegible](ID) = 0.
      [illegible](ID) = [illegible]
      [illegible](ID) = 0.
      PFAIL = 0.
      PAVE = 0.
      [illegible](ID) = 0.
      PBURN = 0.
      RETURN
   30 PRINT 300
  100 FORMAT([illegible]FAILURE TIME =[illegible]E17.7,5X,
     1 *AVERAGE POWER =[illegible]THRESHOLD FAILURE POWER =*,E13.5)
  200 FORMAT(10X,*BURNOUT MODEL IDENTIFIER OUT OF RANGE.  ID=*,I5)
  300 FORMAT(10X,*INVALID RESULTS FROM DAMAGE MODEL,*,/,10X,
     1 *RUN TERMINATED.*,/,10X,*RESULTS OF DAMAGE MODEL MAY BE USED *,
     2 *ONLY IN THE OUTPUTS SECTION.*)
      STOP
      END
CEND          QUAD 2-INPUT NAND GATE LEVEL SELECT
C      FOR USE WITH 2 INPUT NAND GATE
      FUNCTION FN2(A,B,C,D,E,F)
C      [illegible]
C      [illegible]
      IF(A.LT.C.OR.B.LT.C)GO TO 6
      IF(A.GE.E.AND.B.GE.E)GO TO 5
      FN2=D-AMIN1(A,B)
      RETURN
      FN2=D
      RETURN
    5 FN2=F
      RETURN
      END
C              DIGITAL IC CAPACITOR SELECT
      FUNCTION FCAP(A,B,C,D)
C      TO ESTABLISH CAPACITOR VALUE OF DIGITAL IC
      FCAP=C
      IF(A.GE.B)FCAP=D
      RETURN
      END
MODEL DESCRIPTION
MODEL [illegible](A=B=OUT=GND)
2 INPUT NAND GATE
A=INPUT A
B=INPUT B
ELEMENTS
JA,A-GND=0.
JB,B-GND=0.
JO,OUT-GND=0.
[illegible]
[illegible]
[illegible]
[illegible]
[illegible]
[illegible]
```

Figure VII-4. Interface Latch Behavior Following Neutron Exposure (Continued)

```
FUNCTIONS
Q2(A,B,C,D)=(FCAP1(A,B,C,D))
Q4(A,B,C,D,E,F)=(FN2(A,B,C,D,E,F))
MODEL 2N2222 (1-2-3)
ELEMENTS
JCC,1-2=X3(3.30E-14*(EXP(38.61*VJE)-1.))
JEC,3-2=X4(3.30E-14*(EXP(38.61*VJC)-1.))
JC,2-1=Q1(JEC,0.499)
JC,2-3=Q1(JCC,0.903248)
CC,1-2=1.E-12
CE,3-2=1.E-12
FUNCTIONS
Q1(A,B)=(A/B)
CIRCUIT DESCRIPTION
ELEMENTS
R1,1-2=40000.
T1,3-2-0=MODEL 2N2222
R2,4-3=1000.
ECC,0-4=5.
VA1,3-6-5-0=MODEL (0)
VA2,5-7-6-0=MODEL (0)
JOUT,6-0=0
ESIG,0-1=TABLE 1(TIME)
EHST,0-7=TABLE 2(TIME)
JB,7-0=0
DEFINED PARAMETERS
PFR=FBURN(1.,TIME,PA,PF,PIR,PVR,PTE,PK,PB)
PA=0
PF=0
PIR=X1(-JB)
PVR=X2(-VJB)
PTE=0.0
PK=0.00216
PB=0.689
FUNCTIONS
TABLE 1
0,0,4.E-3,0,4.1E-3,1,6.E-3,10,6.1E-3,0,1.E-2,0
TABLE 2
0,0,2.E-3,0,2.1E-3,5,8.E-3,5,8.1E-3,0,1.E-2,0
OUTPUTS
ESIG,EHST,VR2,VJOUT,PLOT
RUN CONTROLS
STOP TIME=1.E-2
MAXIMUM INTEGRATION PASSES=5.E4
END

SYSTEM NOW ENTERING SIMULATION



COMPUTER TIME AT TERMINATION OF SETUP PHASE-
          CPA       3.085 SEC.
          PP        0.000 SEC.
          IO        0.000 SEC.
```

Figure VII-4. Interface Latch Behavior Following Neutron Exposure (Continued)

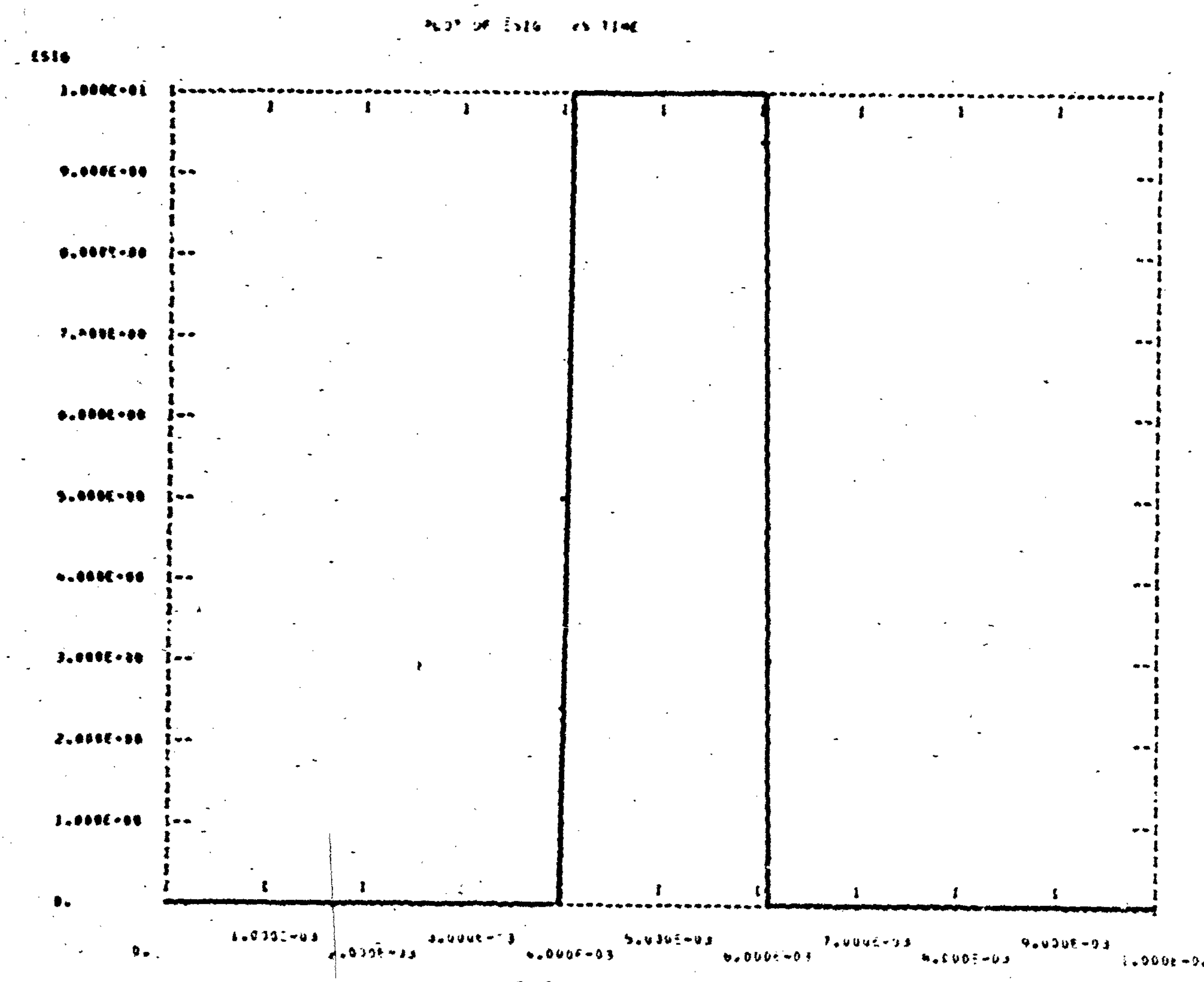

Figure VII-4. Interface Latch Behavior Following Neutron Exposure (Continued)

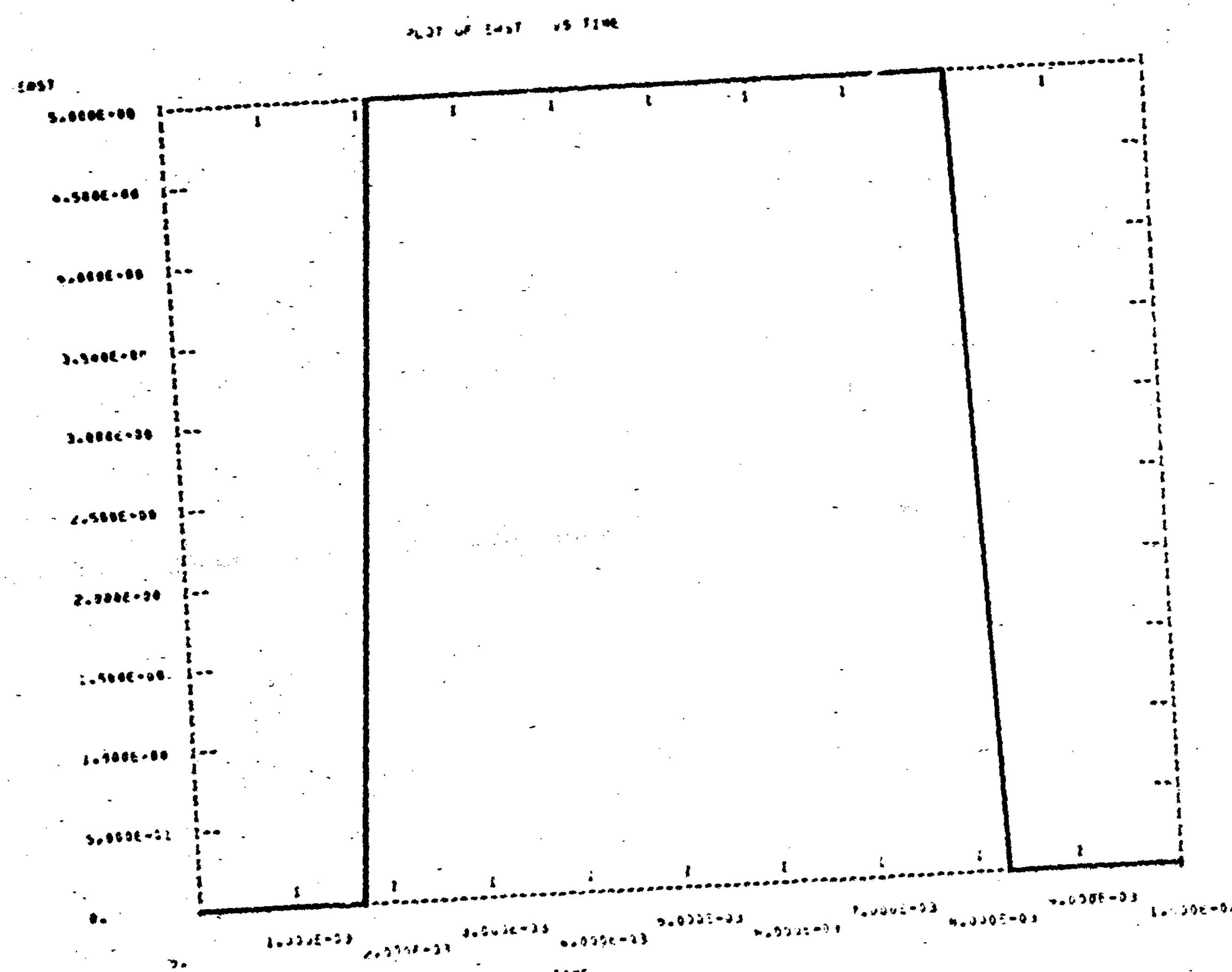

Figure VII-4. Interface Latch Behavior Following Neutron Exposure (Continued)

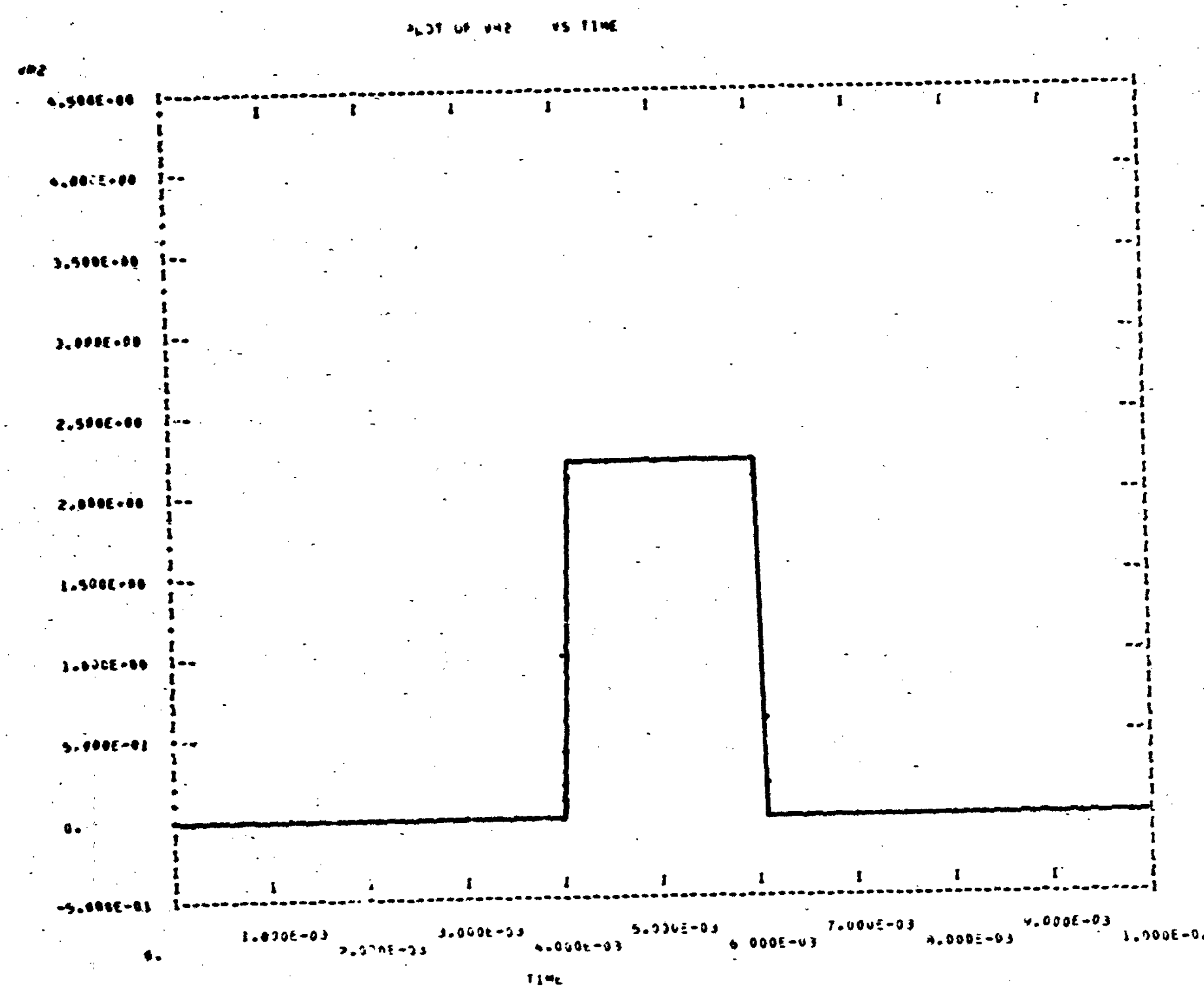

Figure VII-4. Interface Latch Behavior Following Neutron Exposure (Continued)

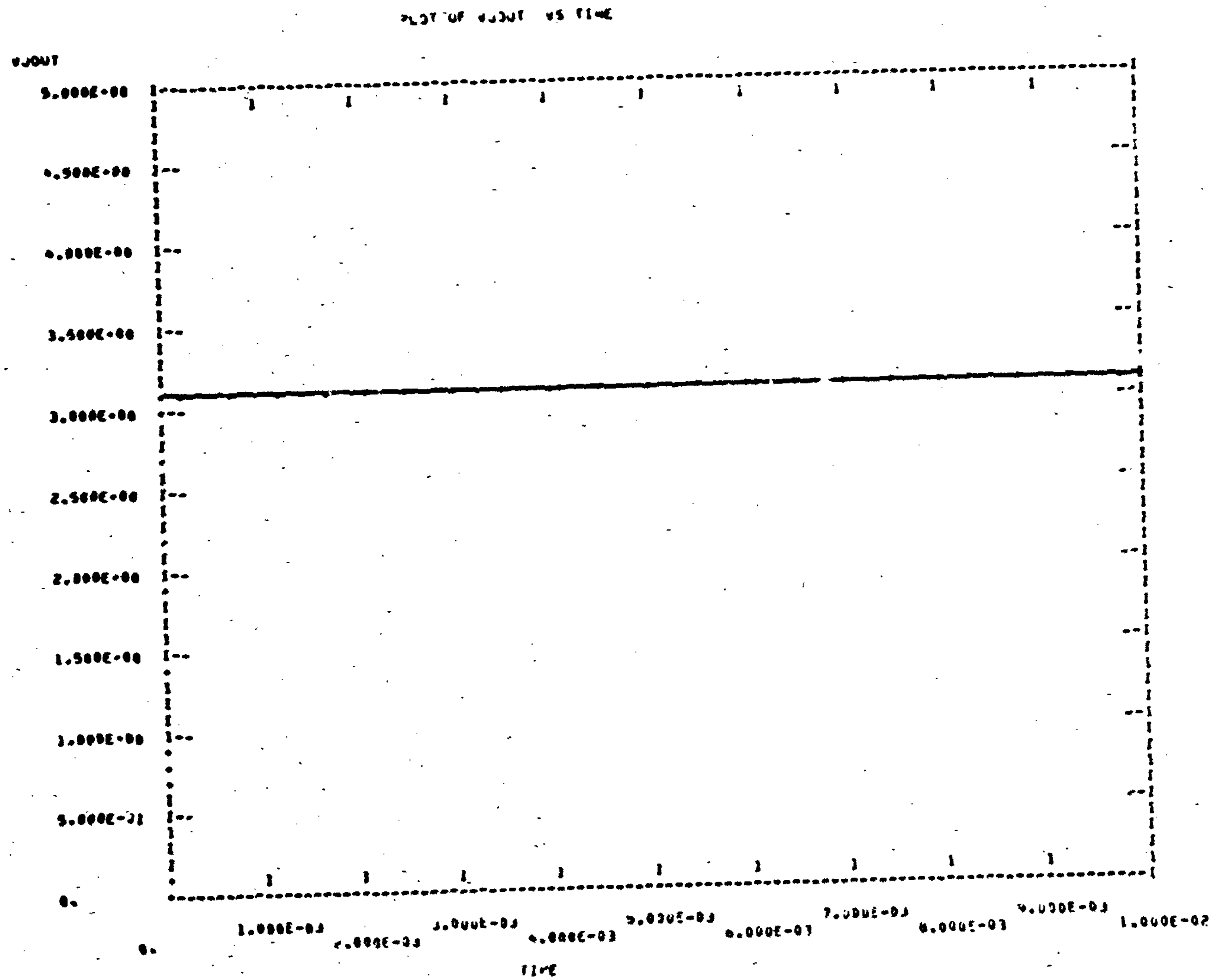

Figure VII-4. Interface Latch Behavior Following Neutron Exposure (Concluded)

$$I_{pp}\ (\text{mA}) = 10^{8}\ (0.3\ \text{GHz})^{-2/5}\ (75\ \text{V})(8\ \text{pF}\ 10\ \text{V}^{1/3} + 1.08)$$
$$(21.6 + 5^{1/3})(3.24 \times 10^{-13})$$

$$I_{pp} = 1.68\ \text{mA}$$

Note: The data sheet value of f_t = 300 MHz was used instead of the measured value of f_t = 155 MHz. The ionizing waveform was chosen to be triangular, rising to the peak value in 20 ns and falling in 70 ns.

The latch reset line voltage (ERST) was set high to allow the observation of a false triggering of the latch due to photocurrents. The photocurrent generator (JPP) was then placed between the collector and base of the transistor and a simulation run made. Observation of the voltage across the collector resistor (VR2) indicates that the photocurrent saturated the 2N2222A producing an erroneous logic state. The final result was a false latching of the output (VJOUT). Figure VII-5 is the computer run for this example.

A nuclear burst also produces a powerful electromagnetic pulse which may be coupled to a circuit and then produce a burnout failure. The latch reset line (ERST) is to be analyzed for hardness to electrical overstress.

The overstress waveform for this example is the double exponential described in chapter II.B.8 in the photocurrent section. The parameters describing this waveform are:

V_{peak}	(I_{pp})	= 100 volts
t_{D1}		= 0
t_{D2}		= 1×10^{-7} seconds
τ_R		= 5×10^{-7} seconds
τ_F		= 1×10^{-6} seconds

The waveform which is described by these constants is generated in the computer output of figure VII-6 as EP.

```
S C E P T R E   NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2        5/76
 03/17/78     18.54.55.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD  "DOCUMENT"  AS THE FIRST CARD
OF THE INPUT TEXT


COMPUTER TIME ENTERING SETUP PHASE-
          CPA       .393 SEC.
          PP       0.000 SEC.
          IO       0.000 SEC.


SUBPROGRAM
      FUNCTION FBURN(AD,TIME,PAVE,PFAIL,I,V,TE,A,B)
C     THIS SUBROUTINE MONITORS POWER IN A JUNCTION AND FLAGS FAILURE.
C     FAILURE IS DEFINED BY P=AT**(-B) USING AVERAGE POWER.
C     PAVE = AVERAGE POWER, PFAIL = FAILURE POWER, FBURN = PAVE/PFAIL
C     I,V,A,B SHOULD ALL REFER TO JUNCTION VALUES OR OVERALL VALUES.
C     I,V,A,B MAY REFER TO EITHER FORWARD OR REVERSE POLARITIES.
C      V= VOLTAGE, I= CURRENT
C     A,B ARE CONSTANTS IN THE FAILURE POWER VERSES TIME RELATIONSHIP.
      REAL I
C     AD IS INTEGER IDENTIFYING JUNCTION AND POLARITY TO BE EVALUATED.
      DIMENSION OLDP(20),OLDT(20),OLDE(20),OLDF(20)
      MAXMOD = 20
C     TO INCREASE NUMBER OF BURNOUT MODELS AVAILABLE,
C     INCREASE ALL DIMENSIONS AND MAXMOD EQUALLY.
C     THIS MODEL ASSUMES P=AT**(-B) FOR 0..LT.T-TE.LT.TMAX
      TMAX = 500.E-6
      P = I*V
C     FR IS THE RATIO OF AVERAGE POWER/FAILURE POWER DEFINED AS FAILURE
      FR = 1.
      ID = INT(AD)
      IF((ID.GT.MAXMOD).OR.(ID.LT.1)) GO TO 10
      IF(TIME.LE.TE) GO TO 20
      IF(TIME.LT.OLDT(ID)) GO TO 30
      IF(TIME.GT.TMAX) GO TO 20
C     TRANSIENT HAS STARTED AND
C     POINT AT TIME = OLDT WAS ACCEPTED BY ERROR CRITERIA.
      OLDE(ID) = OLDE(ID) + (P+OLDP(ID))*(TIME-OLDT(ID))/2.
      PAVE = OLDE(ID)/(TIME-TE)
      PFAIL = A*(AMAX1(TIME-TE,2.)**(-B))
      FBURN = PAVE/PFAIL
      IF(OLDF(ID).GT.FR) GO TO 5
      IF(FBURN.GT.FR) PRINT 100,ID,TIME,PAVE,PFAIL
      OLDF(ID) = FBURN
    5 CONTINUE
      OLDP(ID) = I*V
      OLDT(ID) = TIME
      RETURN
```

Figure VII-5. Computer Run for Ionizing Environment Simulation

```
C      BURNOUT MODEL IDENTIFIER OUT OF RANGE
   10 PAVE = 0.
      PFAIL = 0.
      FBURN = 0.
      PRINT 200,ID
      RETURN
C      TRANSIENT HAS NOT STARTED.
C      OR TIME EXCEEDS VALID INTERVAL FOR P=K/SQRT(T).
   20 OLDP(ID) = 0.
      OLDT(ID) = TE
      OLDF(ID) = 0.
      PFAIL = 0.
      PAVE = 0.
      OLDF(ID) = 0.
      FBURN = 0.
      RETURN
   30 PRINT 300
  100 FORMAT(6(/),10X,*ID=*,I5,5X,*FAILURE TIME =*,E17.7,5X,
     1 *AVERAGE POWER =*,E13.3,5X,*THRESHOLD FAILURE POWER =*,E13.3)
  200 FORMAT(10X,*BURNOUT MODEL IDENTIFIER OUT OF RANGE.  ID=*,I5)
  300 FORMAT(10X,*INVALID RESULTS FROM DAMAGE MODEL*,/,10X,
     1 *RUN TERMINATED.*,/,10X,*RESULTS OF DAMAGE MODEL MAYBE USED *,
     2 *ONLY IN THE OUTPUTS SECTION.*)
      STOP
      END
CFN2          QUAD 2-INPUT NAND GATE LEVEL SELECT
C      FOR USE WITH 2 INPUT NAND GATE
      FUNCTION FN2(A,B,C,D,E,F)
C      A=VJA B=VJB C=0.8
C      D=4.1 E=1.4 F=0.3
      IF(A.LE.C.OR.B.LE.C)GO TO 4
      IF(A.GE.E.AND.B.GE.E)GO TO 5
      FN2=D-AMIN1(A,B)
      RETURN
    4 FN2=D
      RETURN
    5 FN2=F
      RETURN
      END
C             DIGITAL IC CAPACITOR SELECT
      FUNCTION FCAP1(A,B,C,D)
C      TO ESTABLISH CAPACITOR VALUE OF DIGITAL IC
      FCAP1=C
      IF(A.GE.B)FCAP1=D
      RETURN
      END
MODEL DESCRIPTION
MODEL L00(A-B-OUT-GND)
2 INPUT NAND GATE
A=INPUT A
B=INPUT B
ELEMENTS
JA,A-GND=0.
JB,B-GND=0.
J0,OUT-GND=0.
C0,OUT-GND=1.E-12
E1,GND-1=Q4(VJA,VJB,0.8,3.1,1.4,0.3)
R1,1-2=100.
C1,2-GND=Q2(E1,E2,550.E-12,300.E-12)
E2,GND-3=X1(VC1)
R2,3-OUT=30.
```

Figure VII-5. Computer Run for Ionizing Environment Simulation (Continued)

```
FUNCTIONS
Q2(A,B,C,D)=(FCAP1(A,B,C,D))
Q4(A,B,C,D,E,F)=(FN2(A,B,C,D,E,F))
MODEL 2N2222 (1-2-3)
ELEMENTS
JCC,1-2=X3(3.30E-14*(EXP(38.61*VJE)-1.))
JEC,3-2=X4(3.30E-14*(EXP(38.61*VJC)-1.))
JC,2-1=Q1(JEC,0.998)
JE,2-3=Q1(JCC,0.99567)
CC,1-2=1.E-12
CE,3-2=1.E-12
FUNCTIONS
Q1(A,B)=(A/B)
CIRCUIT DESCRIPTION
ELEMENTS
JB,7-0=0
ESIG,0-1=0
R1,1-2=40000.
T1,3 2-0=MODEL 2N2222
R2,4-3=1000.
ECC,0-4=5.
VA1,3-6-5-0=MODEL LOD
VA2,5-7-6-0=MODEL LOD
ERST,0-7=TABLE 2(TIME)
JPP,1-2=TABLE 1(TIME)
JOUT,6-0=0
DEFINED PARAMETERS
PFR=FBURN(1.,TIME,PA,PF,PIR,PVR,PTE,PK,PB)
PA=0
PF=0
PIR=X1(-JB)
PVR=X2(-VJB)
PTE=0.0
PK=0.00216
PB=0.689
FUNCTIONS
TABLE 1
0,0,5.E-6,0,5.02E-5,1.68E-3,5.09E-5,0,1.E-7,0
TABLE 2
0,0,1.E-6,5,1,5
OUTPUTS
ESIG,ERST,VR2,VJOUT,PLOT
RUN CONTROLS
STOP TIME=1.E-5
MAXIMUM INTEGRATION PASSES=5.E4
END

SYSTEM NOW ENTERING SIMULATION



COMPUTER TIME AT TERMINATION OF SETUP PHASE-
          CPA       4.127 SEC.
          PP        0.000 SEC.
          IO        0.000 SEC.
```

Figure VII-5. Computer Run for Ionizing Environment Simulation (Continued)

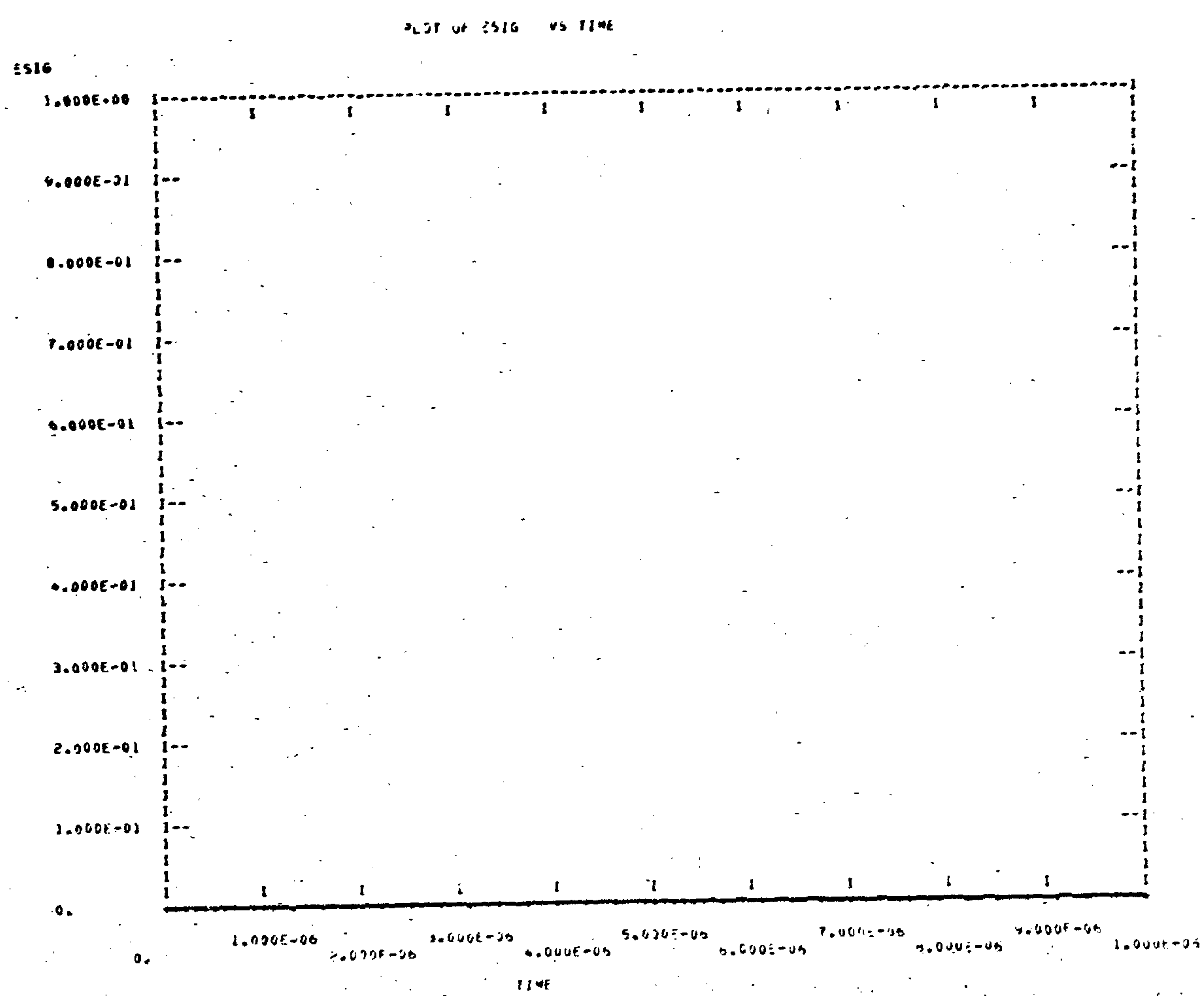

Figure VII-5. Computer Run for Ionizing Environment Simulation (Continued)

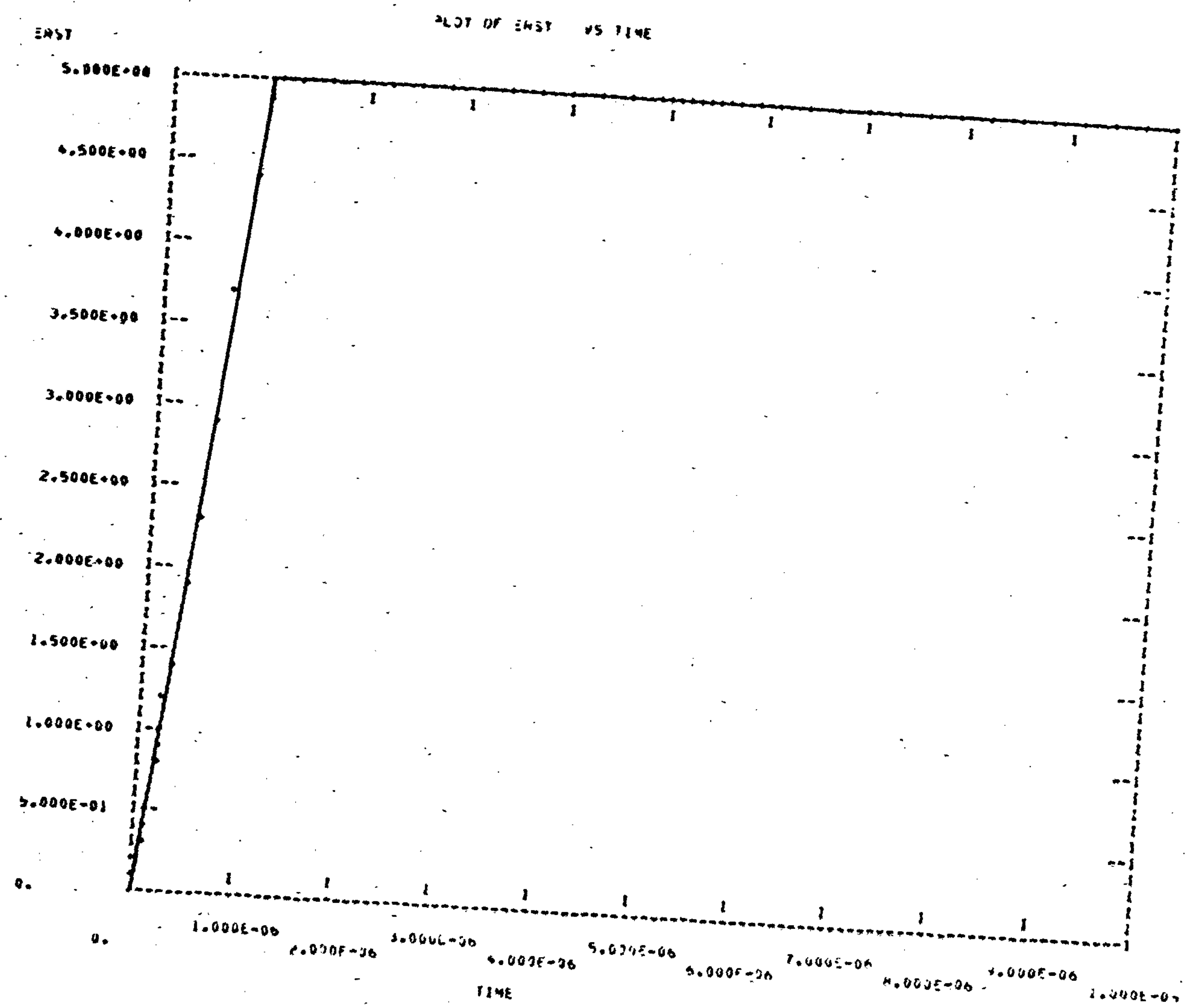

Figure VII-5. Computer Run for Ionizing Environment Simulation (Continued)

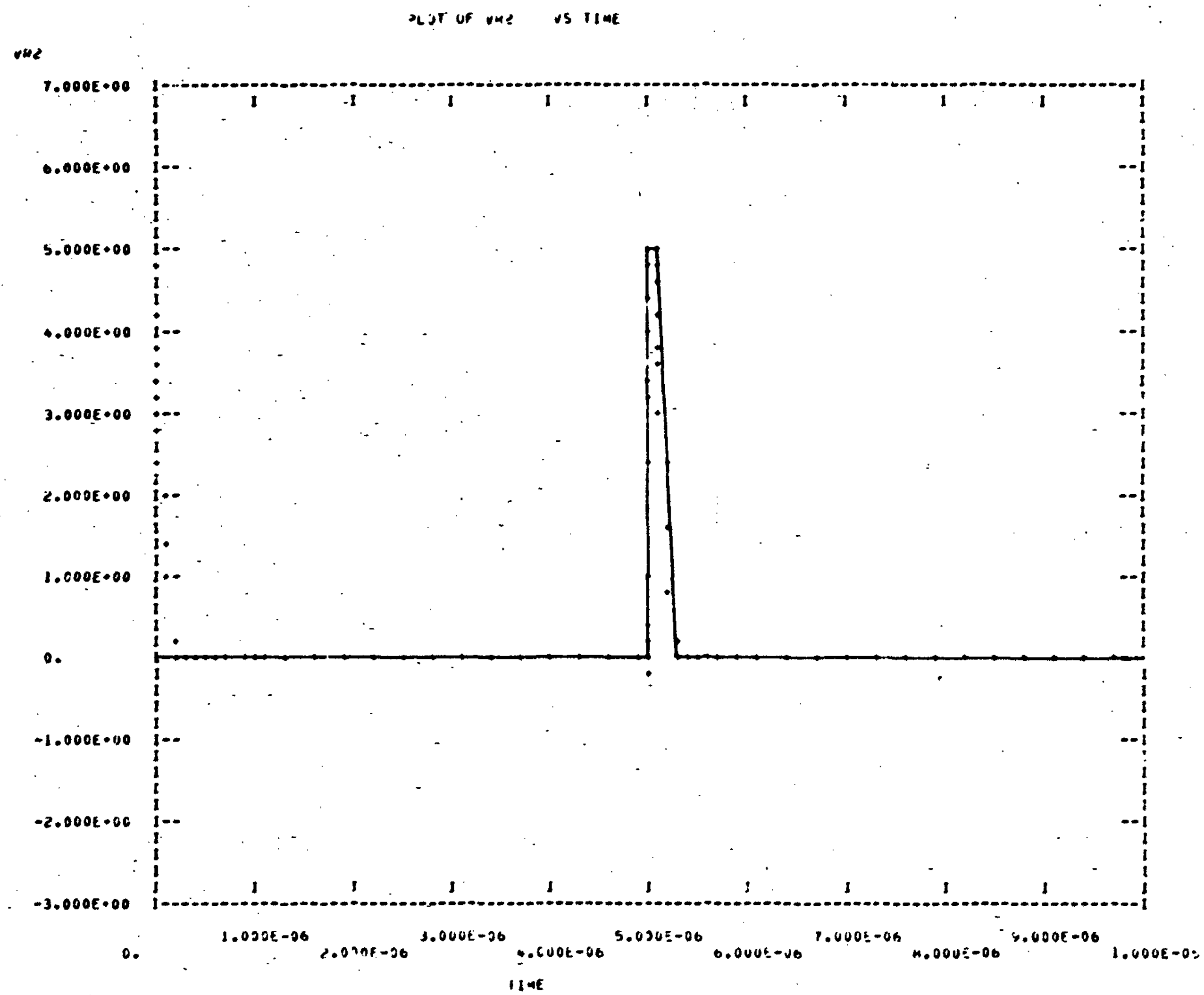

Figure VII-5. Computer Run for Ionizing Environment Simulation (Continued)

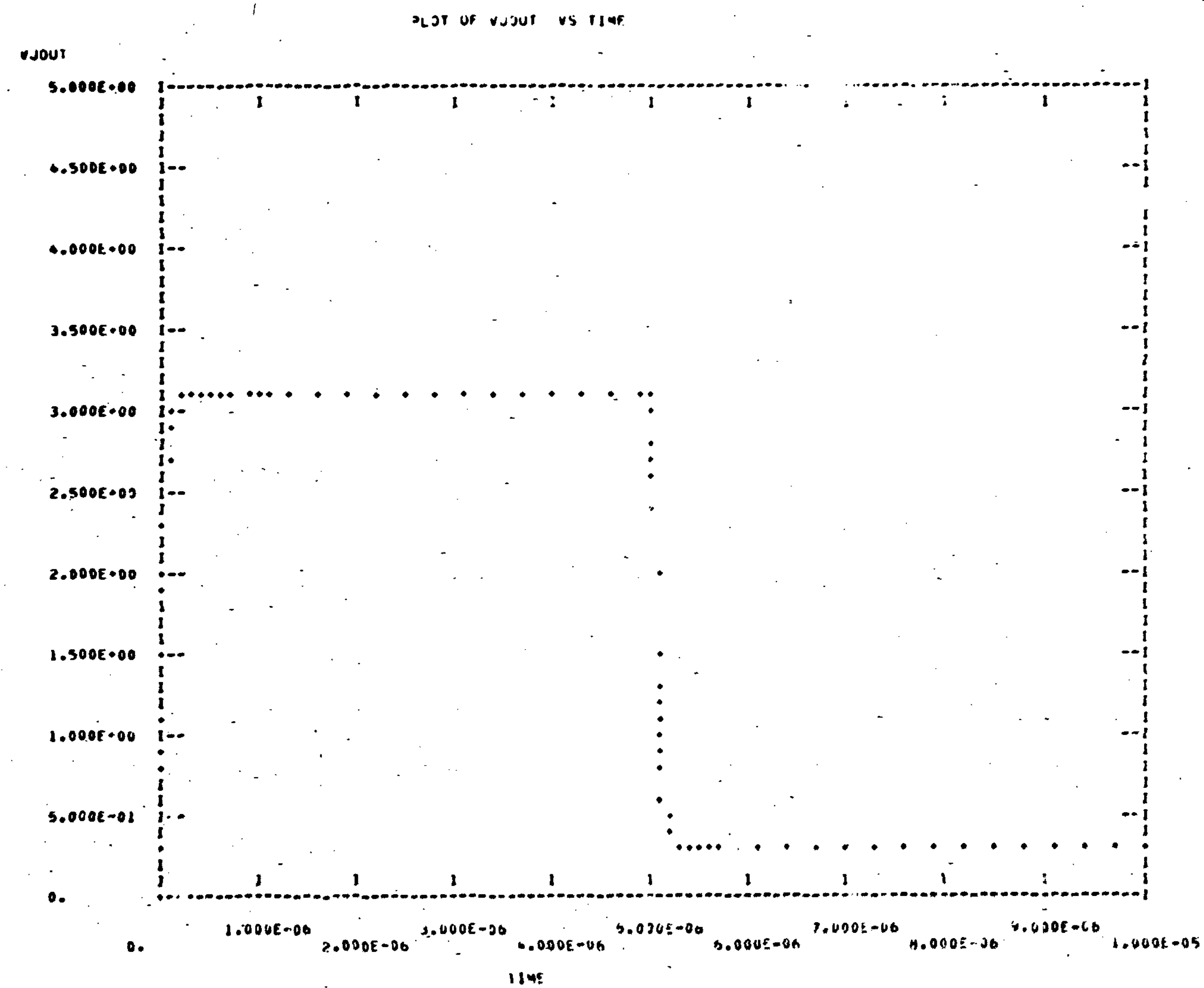

Figure VII-5. Computer Run for Ionizing Environment Simulation (Concluded)

```
S C E P T R E    NETWORK SIMULATION PROGRAM
AIR FORCE WEAPONS LABORATORY - KAFB NM
VERSION CDC 4.5.2         5/76
 03/17/78     18.29.32.


FOR A LISTING OF USER FEATURES UNIQUE TO THIS VERSION OF SCEPTRE
SUPPLY A CARD CONTAINING THE WORD  MODCURENT  AS THE FIRST CARD
OF THE INPUT TEXT


COMPUTER TIME ENTERING SETUP PHASE-
        CPA          .353 SEC.
        PP          0.000 SEC.
        IO          0.000 SEC.


SUBPROGRAM
      FUNCTION FBURN(AD,TIME,PAVE,PFAIL,I,V,TE,A,B)
C     THIS SUBROUTINE MONITORS POWER IN A JUNCTION AND FLAGS FAILURE.
C     FAILURE IS DEFINED BY PEAT**(-B) USING AVERAGE POWER.
C     PAVE = AVERAGE POWER. PFAIL = FAILURE POWER. FBURN = PAVE/PFAIL
C     I,V,A,B SHOULD ALL REFER TO JUNCTION VALUES OR OVERALL VALUES.
C     I,V,A,B MAY REFER TO EITHER FORWARD OR REVERSE POLARITIES.
C      V= VOLTAGE, I= CURRENT
C     A,B ARE CONSTANTS IN THE FAILURE POWER VERSES TIME RELATIONSHIP.
      REAL I
C     AD IS INTEGER IDENTIFYING JUNCTION AND POLARITY TO BE EVALUATED.
      DIMENSION OLDP(20),OLDT(20),OLD (20),OLDF(20)
      MAXMOD = 20
C     TO INCREASE NUMBER OF BURNOUT MODELS AVAILABLE,
C     INCREASE ALL DIMENSIONS AND MAXMOD EQUALLY.
C     THIS MODEL ASSUMES P=AT**(IB) FOR 0..LT.T-TE.LT.TMAX
      TMAX = 500.E-6
      P = I*V
C     FR IS THE RATIO OF AVERAGE POWER/FAILUER POWER DEFINED AS FAILURE
      FR = 1.
      ID = INT(AD)
      IF((ID.GT.MAXMOD).OR.(ID.LT.1)) GO TO 10
      IF(TIME.LE.TE) GO TO 20
      IF(TIME.LT.OLDT(ID)) GO TO 40
      IF(TIME.GT.TMAX) GO TO 20
C     TRANSIENT HAS STARTED AND
C     POINT AT TIME = OLDT WAS ACCEPTED BY ERROR CRITERIA.
      OLDE(ID) = OLDE(ID) + (P+OLDP(ID))*(TIME-OLDT(ID))/2.
      PAVE = OLDE(ID)/(TIME-TE)
      PFAIL = A*(A*A(I(TIME-TE+0.)**(-B))
      FBURN = PAVE/PFAIL
      IF(OLDF(ID).GT.FR) GO TO 5
      IF(FBURN.GT.FR) PRINT 100,ID,TIME,PAVE,PFAIL
      OLDF(ID) = FBURN
    5 CONTINUE
      OLDP(ID) = I*V
      OLDT(ID) = TIME
      RETURN
```

Figure VII-6. Computer Results of Overstress Simulation

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FROM COPY FURNISHED TO DDC

```
C     BURNOUT MODEL IDENTIFIER OUT OF RANGE
   10 PAVE = 0.
      PFAIL = 0.
      FRORN = 0.
      PRINT 200,I)
      RETURN
C     TRANSIENT HAS NOT STARTED.
C     OR TIME [illegible] VALID INTERVAL FOR [illegible]
   20 OLDP(I0) = 0.
      OLDT(I0) = T
      OLDF(I0) = 0.
      PFAIL = 0.
      PAVE = 0.
      OLDF(I0) = 0.
      FRORN = 0.
      RETURN
   30 PRINT 400
  100 FORMAT [illegible] FAILURE TIME [illegible]
     1 AVERAGE POWER [illegible] FAILURE POWER [illegible]
  200 FORMAT [illegible] BURNOUT MODEL IDENTIFIER OUT OF RANGE [illegible]
  400 FORMAT [illegible] RESULTS [illegible] DAMAGE MODE [illegible]
     1 [illegible] TERMINATED [illegible] DAMAGE MODEL MAY BE USED [illegible]
     2 [illegible] IN THE OUTPUTS SECTION [illegible]
      STOP
      END
C             QUAD 2-INPUT NAND GATE LEVEL SELECT
C     FOR USE WITH 2 INPUT NAND GAT
      FUNCTION [illegible]
C     [illegible]
C     [illegible]
      IF [illegible] GO TO 4
      IF [illegible] GO TO 5
      [illegible]=AMIN1[illegible]
      RETURN
    4 [illegible]
      RETURN
    5 [illegible]
      RETURN
      END
C             DIGITAL IC CAPACITOR SELECT
      FUNCTION FCAP[illegible]
C     TO ESTABLISH CAPACITOR VALUE OF DIGITAL IC
      FCAP=C
      IF [illegible]
      RETURN
      END
MODEL DESCRIPTION
MODEL [illegible]
2 INPUT NAND GATE
A=INPUT A
B=INPUT B
ELEMENTS
[illegible]
[illegible]
[illegible]
[illegible]
[illegible]
[illegible]
[illegible]
[illegible]
[illegible]
FUNCTIONS
[illegible]
[illegible]
MODEL [illegible]
ELEMENTS
[illegible]
[illegible]
[illegible]
[illegible]
[illegible]
[illegible]
```

Figure VII-6. Computer Results of Overstress Simulation (Continued)

```
FUNCTIONS
R1(A,B)=(A/B)
CIRCUIT DESCRIPTION
ELEMENTS
JB,7-0=TABLE 3(VJB)
ESIG,0-1=0
R1,1-2=40000.
T1,3-2-0=MODEL 2N2222
R2,4-3=1000.
ECC,0-4=5.
NA1,3-6-5-0=MODEL LED
NA2,5-7-6-0=MODEL LED
JOUT,6-0=0
EP,0-P=R3(100.*(EXP(-1.*AMAX1((TIME-1.E-7),0.)/1.E+6)-EXP(-TIME/5.E-7)))
REMP,P-7=.01
DEFINED PARAMETERS
PFR=FBURN(P,TIME,PA,PF,PIR,PVR,PTE,PK,PB)
PA=0
PF=0
PIR=R1(-JB)
PVR=R2(-VJB)
PTE=0.0
PK=0.00216
PB=0.689
FUNCTIONS
TABLE 3
0.0,7.0,6.0525
OUTPUTS
VJOUT,EP,PFR,PLOT
RUN CONTROLS
STOP TIME=1.E-5
MAXIMUM INTEGRATION PASSES=5.E6
END


THE TERM VREMP , WILL CAUSE A COMPUTATIONAL DELAY.


THE TERM VREMP WILL CAUSE A COMPUTATIONAL DELAY.


SYSTEM NOW ENTERING SIMULATION


COMPUTER TIME AT TERMINATION OF SETUP PHASE
          CPA        4.456 SEC.
          PP         0.100 SEC.
          IO         0.100 SEC.
```

Figure VII-6. Computer Results of Overstress Simulation (Continued)

```
COMPUTER TIME ENTERING SIMULATION-
        CPA        5.702 SEC.
        PP         0.300 SEC.
        IO         0.300 SEC.


    ID=    1     FAILURE TIME =     .99137[illegible]E-06     AVERAGE POWER =     .3352E+02     THRESHOLD FAILURE POWER =     .31[illegible]E+02
```

Figure VII-6. Computer Results of Overstress Simulation (Continued)

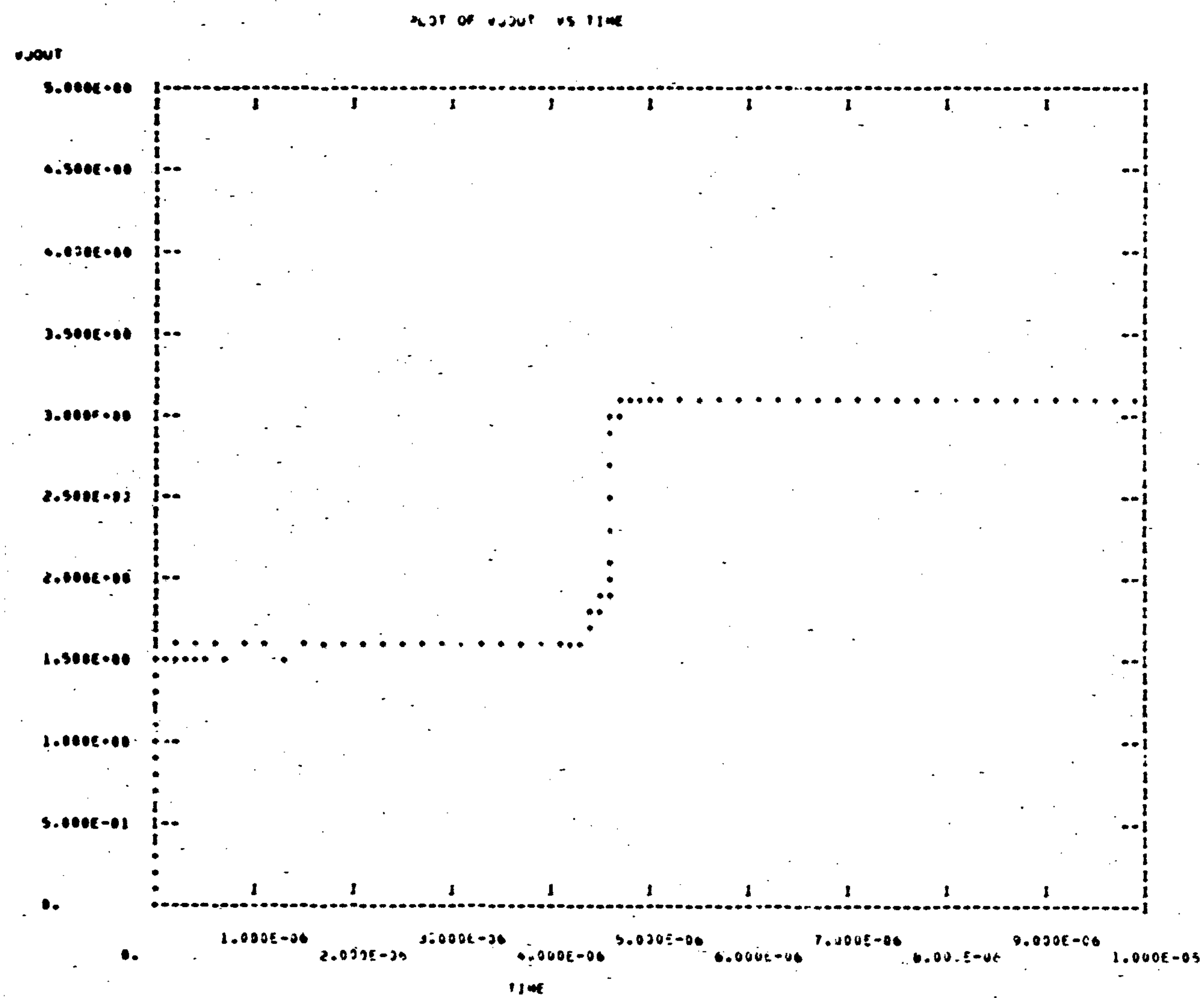


Figure VII-6. Computer Results of Overstress Simulation (Continued)

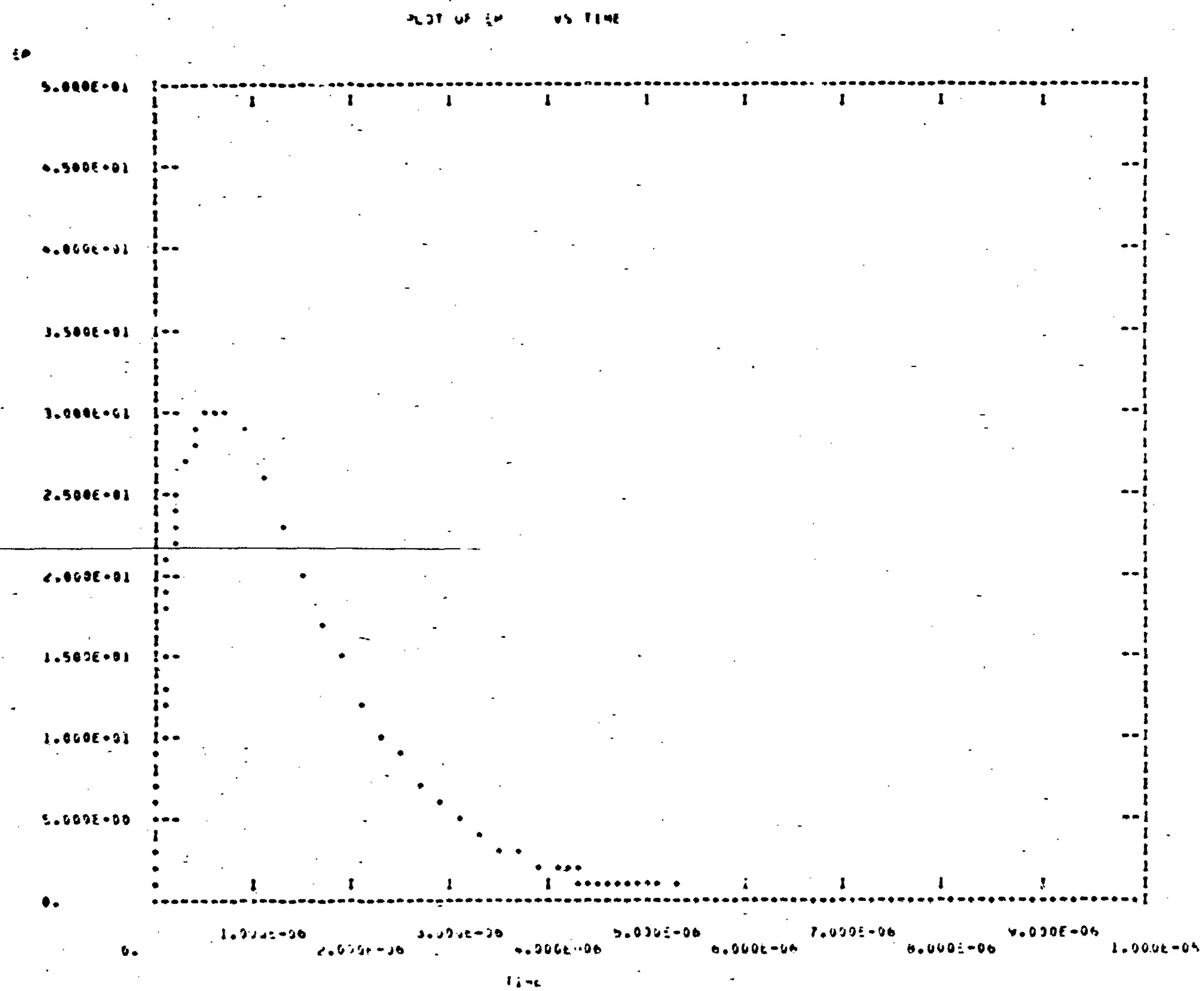


Figure VII-6. Computer Results of Overstress Simulation (Continued)

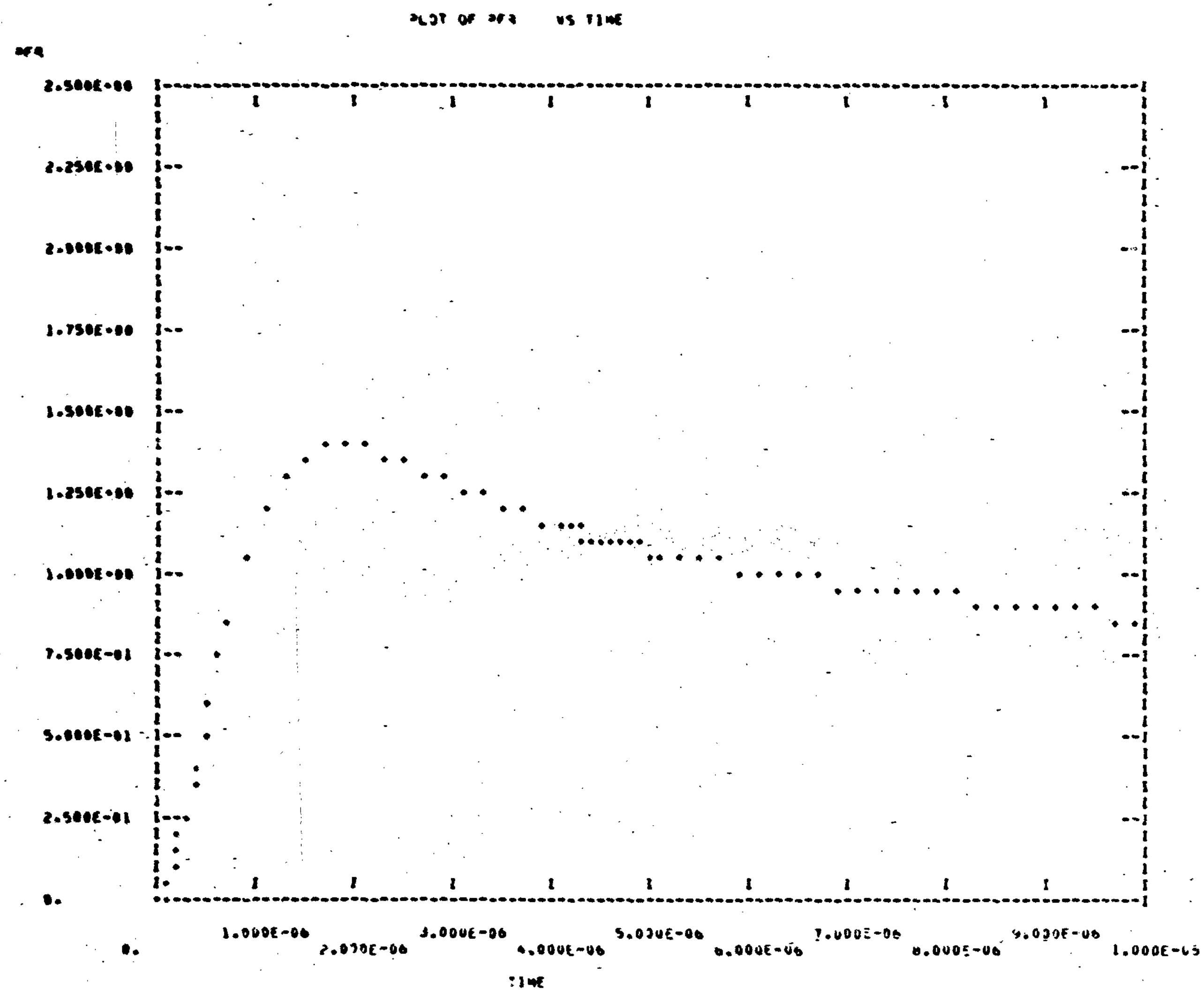


Figure VII-6. Computer Results of Overstress Simulation (Concluded)

A power monitoring device is now required at the gate input which w'll react to an electrical overstress signal. This element will be monitored by FBURN to allow a prediction of failure.

Information on the electrical overstress behavior of TTL was obtained from reference VII-1, where the overstress parameters for TTL input are listed as:

$$A \text{ of } P = At^{-B} = 0.00216$$
$$B \text{ of } P = At^{-C} = 0.689$$
$$V_{BD} = 7\ V$$
$$R_B = 16\ \Omega$$

The power monitoring element was given the characteristic of figure VII-7. The simulation predicted that under such overstress conditions, an interface latch circuit would suffer failure due to heating in about 9 x 10^{-7} seconds following the initiation of the overstress waveform.

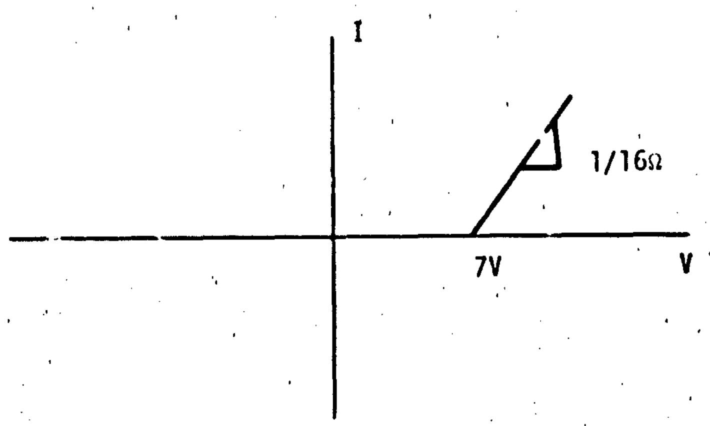


Figure VII-7. Power Monitoring Element Characteristics

B. <u>EFFECTS OF NEUTRONS, GAMMA DOSE RATE, AND EMP UPSET ON A POWER REGULATOR</u>

The discrete components of the power regulator in this example which were not previously modeled, were developed entirely from data sheets or "safe" default values demonstrating that models may be developed which do not require measurements. Also, the two transistor model for the SCR is demonstrated. Figure VII-8 is a schematic representation of the power supply to be analyzed.

The power regulator represents some special problems for hardness assessment. First, the power regulator simulations represent a special mix of long and short time constants imposing a burden on the computer code. A long simulation time problem also produces the problem of how to include very short lived phenomenon. One solution is to use the initial conditions feature of the code, if available, and then look at a very small slice of time. Another possibility is to look at the behavior of one "piece" of the circuit at a time, avoiding simulation of the whole system.

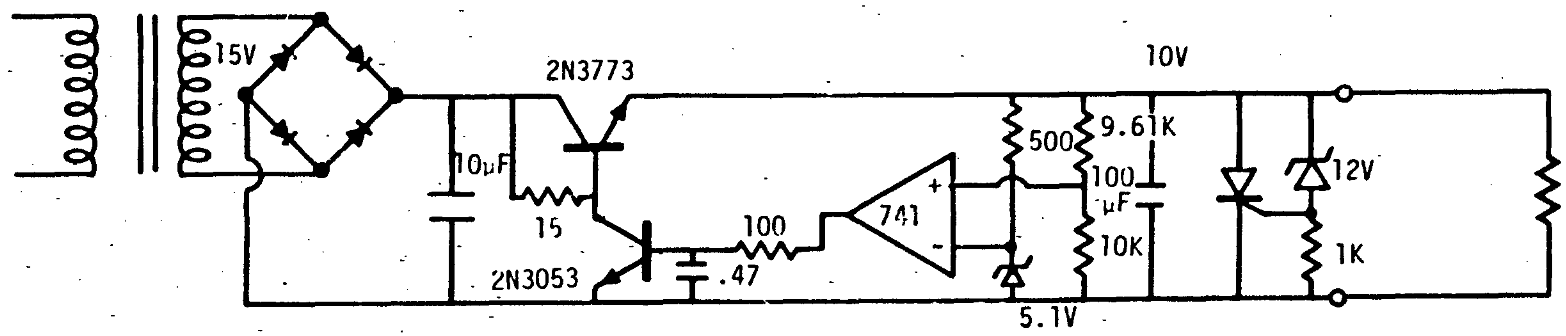
1. <u>Model Development</u>

a. <u>Bridge Diodes, Zener Diodes</u>

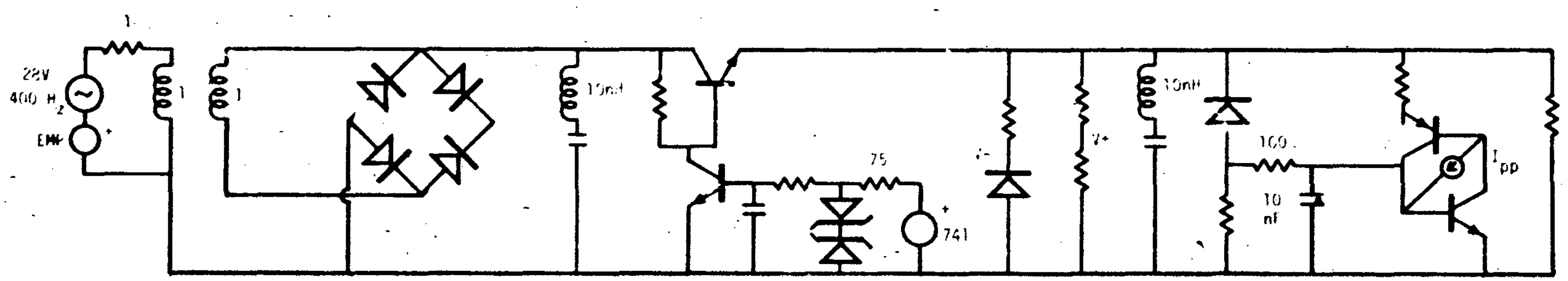
Very simple models for the diodes were used since more complex models would add nothing to the simulation results. The diodes were described by ideal diode equations. Saturation currents were simply defined by the "safe" default value of 1×10^{-14} amperes. The zener diodes were given the additional parameters of a breakdown voltage and a breakdown current chosen as 1 mA.

b. <u>Transformer</u>

The power supply transformer was given perfect flux linkage by defining K (the coupling coefficient) to be 1. The inductance of the primary and secondary coils were chosen as 1 henry for this example.



(a) Circuit Schematic



(b) Equivalent Circuit

Figure VII-8. Power Regulator

c. <u>2N3053</u>

The basic model of a 2N3053 was developed from the data sheets shown in figure VII-9.

The transistor saturation current is ideally obtained from a plot of I_C where $V_{BE} = V_{CE}$. The best available information is from figure 8 of the data sheets. Choosing $V_{BE} = 1$ V where $V_{CE} = 10$ V yields a collector current of 240 mA,

$$I_S = \frac{240 \text{ mA}}{\exp \frac{1 \text{ V}}{.0259 \text{ V}}} = 4.09 \times 10^{-18} \text{ A}$$

Figure 9 of the data sheets yields a base current of 2.3 mA at $V_{BE} = 1$ V which allows current gain to be calculated.

$$\beta = \frac{240 \text{ mA}}{2.3 \text{ mA}} = 104$$

d. <u>2N3773</u>

The basic transistor model for a 2N3773 was developed from the manufacturer's specification sheets shown in figure VII-10.

I_S, the transistor saturation current, can be obtained if I_C at $V_{BE} = V_{CE}$ is available. Figure 8 of the data sheets yields the best approximation to this condition. At $V_{BE} = 0.8$ V, collector current is 3.2 A.

$$I_S = \frac{3.2 \text{ A}}{\exp \frac{0.8 \text{ V}}{0.0259 \text{ V}}} = 1.23 \times 10^{-13} \text{ A}$$

Figure 20 of the data sheets yields the base current at $V_{BE} = 0.8$ V allowing current gain to be calculated.

$$\beta = \frac{3.2 \text{ A}}{0.07 \text{ A}} = 45.71$$

2N697, 2N699, 2N1613, 2N1711, 2N1893, 2N2102, 2N2270, 2N2405, 2N3053 40366, 40389, 40392, 41502,

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS VOLTAGE V dc V_{CB}	V_{CE}	CURRENT mA dc I_C	I_B	LIMITS 2N1893 MIN	2N1893 MAX	2N2405 MIN	2N2405 MAX	2N2270 MIN	2N2270 MAX	2N3053 40389 40392 MIN	2N3053 40389 40392 MAX	41502 MIN	41502 MAX	UNITS
*Collector Cutoff Current With emitter open	I_{CBO}	15													2	μA
		30											0.25			
		60									0.05					
		90					0.01		0.01							
At T_C = 150°C		60									50					
		90					15		10							
*Emitter Cutoff Current V_{EB} = 5 V (4 V for 2N3053)	I_{EBO}			0			0.01		0.01		0.1		0.25			μA
*DC Forward Current Transfer Ratio	h_{FE}		10	0.1				20								
			10	1						30						
			10	10*		35		35								
			10	150*		40	120	80	[illegible]	50	200	50	250	20		
At T_C = -55°C			10	10*		20		20								
*Collector to Base Breakdown Voltage With emitter open	$V_{(BR)CBO}$			0		120		120		60		60				V
*Emitter to Base Breakdown Voltage I_E = 0.1 mA	$V_{(BR)EBO}$			[illegible]		7		7		7		5		4		V
*Collector to Emitter Sustaining Voltage With base open	$V_{CEO(sus)}$			100*	0			90		45		40				V
				30*		80		90						30*		
With external base to emitter resistance (R_{BE}) = 10 Ω	$V_{CER(sus)}$			100*		100		140		60		50				V
= 500 Ω				100*				120								
*Base to Emitter Saturation Voltage	$V_{BE(sat)}$			150*	15		1.3		1.5		1.2		1.7			V
				50*	5		1.2		0.2							
*Collector to Emitter Saturation Voltage	$V_{CE(sat)}$			150*	15		1.3		1.1		0.9		1.4		1.5	V
				50*	5		1.9		0.9							
Base to Emitter Voltage	V_{BE}		10	150*											2.5	V
*Common Emitter Small Signal Forward Current Transfer Ratio f = 1 kHz	h_{fe}		5	1		30	100									
= 1 kHz			5	5				50	275	5						
= 1 kHz			10	5		45				5	275					
= 20 MHz			10	50		2.5		6		5		5*				
*Input Impedance f = 1 kHz	h_{ib}	5		1		20	[illegible]	24	34							Ω
		10		5		4	8	4	8							
*Small Signal Reverse Voltage Transfer (Feedback) Ratio f = 1 kHz	h_{rb}	5		1			1.25×10^{-4}		3×10^{-4}							
		10		5			1.25×10^{-4}		3×10^{-4}							
*Output Conductance f = 1 kHz	h_{ob}	5		1			0.5		0.5							μmho
		10		5			0.5		0.5							
*Output Capacitance I_E = 0	C_{ob}	10					15		15		15		15		15	pF
*Input Capacitance V_{EB} = 0.5 V	C_{ib}			0			85		85		80		80		80	pF
Gain Bandwidth Product	f_T					50		120		100		100*				MHz
Noise Figure Circuit Bandwidth (BW) = 1 Hz Reference signal freq. = 1 kHz Generator resistance (R_G) = 500 Ω (2N2405) 1 kΩ (2N2270)	NF	10		0.3					6		10*					dB
*Saturated Switching Time	$t_d + t_r + t_s$										30					ns
Thermal Resistance Junction to case	$R_{\theta JC}$						58.3		35		35		35*		58.3	°C/W
Junction to ambient	$R_{\theta JA}$						219		175		175		175*		219	

* 25 for 40392 * 50 for 40389

* 2N Series Types in accordance with JEDEC registration data

Figure VII-9. 2N3053 Manufacturer Specification Sheet (ref. VII-2)

2N697, 2N699, 2N1613, 2N1711, 2N1893, 2N2102, 2N2270, 2N2405, 2N3053, 40366, 40389, 40392, 41502

Low-Power Silicon N-P-N Planar Transistors

For Small-Signal Applications In Industrial and Commercial Equipment

These RCA types are silicon n-p-n planar transistors intended for a variety of small-signal and medium-power applications. They feature exceptionally high collector-to-emitter sustaining voltage, low leakage characteristics, high switching speeds, and high pulse beta (h_{FE}).

RCA-2N2102 is a direct replacement for the 2N1613. RCA-2N2405 is a direct replacement for the 2N1893. All of these devices are supplied in the JEDEC TO-39 hermetic package.

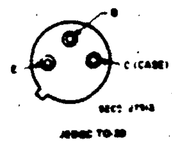
Features:

- Planar construction for low noise and low leakage
- Low output capacitance
- Low saturation voltages

Additional Features for 40366:

- High reliability assured by five pre-conditioning steps
- Group A test data included in data sheet.

TERMINAL DESIGNATIONS



Maximum Ratings, *Absolute Maximum Values*

		2N697	2N699	2N2102 40366	2N1613 2N1711	2N1893	2N2270	2N2405	2N3053 40389 40392	41502	
* COLLECTOR TO BASE VOLTAGE	V_{CBO}	80	120	120	75	120	60	120	80	–	V
COLLECTOR TO EMITTER SUSTAINING VOLTAGE											
With external base-to-emitter resistance (R_{BE}) ≤ 10 Ω	$V_{CER}(sus)$		80	80	50	100	60	140	50	–	V
With base-emitter junction reverse biased	$V_{CEV}(sus)$	–	–	–	–	120	–	120	80	–	V
* With base open	$V_{CEO}(sus)$	–	–	65	–	80	45	90	40	30	V
* EMITTER TO BASE VOLTAGE	V_{EBO}	5	5	7	7	7	7	7	5	4	V
* COLLECTOR CURRENT	I_C	0.5	1	1	1	0.5	1	1	0.7	1	A
* TRANSISTOR DISSIPATION	P_T										
At case temperatures up to 25°C		2	2	5	3	3	5	5	5●	3	W
At free air temperatures up to 25°C		0.6	0.6	1	0.8	0.8	1	1	1●	0.8	W
At temperatures above 25°C		Derate linearly to maximum temperature									
* TEMPERATURE RANGE											
Storage	T_{stg}	-65 to +175				-65 to 200					°C
Operating (Junction)	T_C	-65 to +175				-65 to 200					°C
* LEAD TEMPERATURE (During soldering)											
At distance from seating plane for 10 s max ≥ 1/16 in. (1.58 mm)	T_L	255	230	300	300	255	230	255	235	300	°C

* 2N Series types in accordance with JEDEC registration data

● 7 for 40392 ● 3.5 for 40389

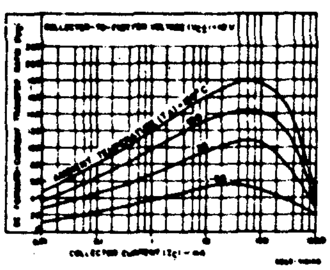


Fig. 1 - Typical dc beta characteristics for 2N699, 2N1613, 2N2102, 2N2270, 41502

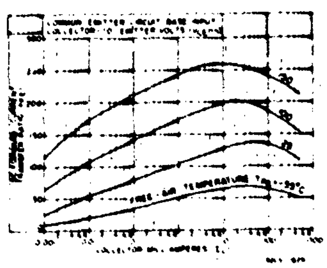


Fig. 2 - Typical dc beta characteristics for 2N1711.

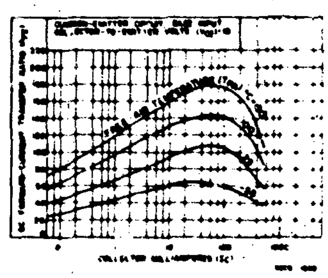


Fig. 3 - Typical dc beta characteristics for 2N1893, 2N2405.

Figure VII-9. 2N3053 Manufacturer Specification Sheet (Continued)

2N697, 2N699, 2N1613, 2N1711, 2N1893, 2N2102, 2N2270, 2N2405, 2N3053, 40366, 40389, 40392, 41502

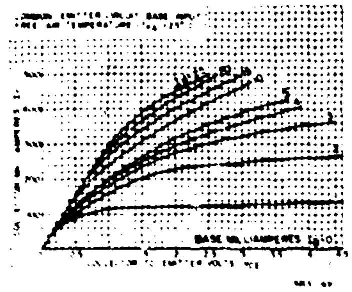


Fig. 22 · Typical high-current output characteristics for 2N1711.

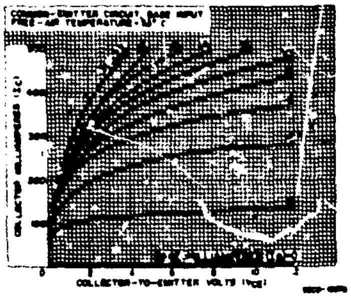


Fig. 23 · Typical high-current output characteristics for 2N1893.

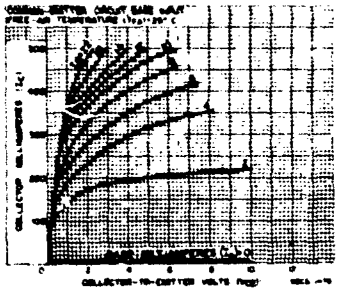


Fig. 24 · Typical high-current output characteristics for 2N2405.

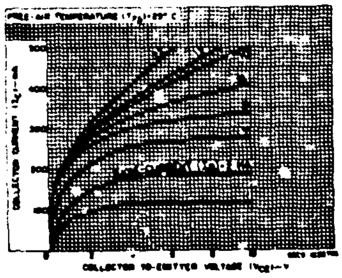


Fig. 25 · Typical high-current output characteristics for 2N3053, 40389, 40392.

Figure VII-9. 2N3053 Manufacturer Specification Sheet (Continued)

2N697, 2N699, 2N1613, 2N1711, 2N1893, 2N2102, 2N2270, 2N2405, 2N3053, 40366, 40389, 40392, 41502

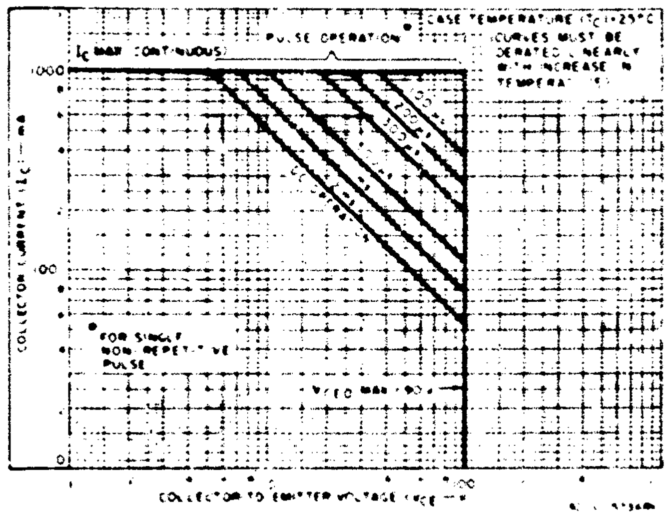


Fig. 4 Maximum operating areas for 2N2405

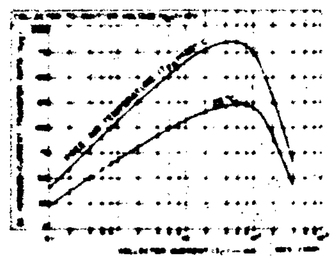


Fig. 6 Typical dc beta characteristics for 2N3053, 40389, 40392

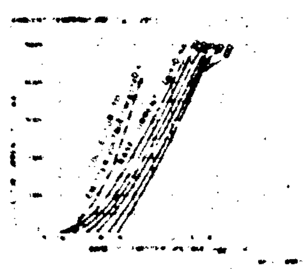


Fig. 7 Typical transfer characteristics for 2N1613, 2N1711, 2N1893, 2N2102, 2N2405

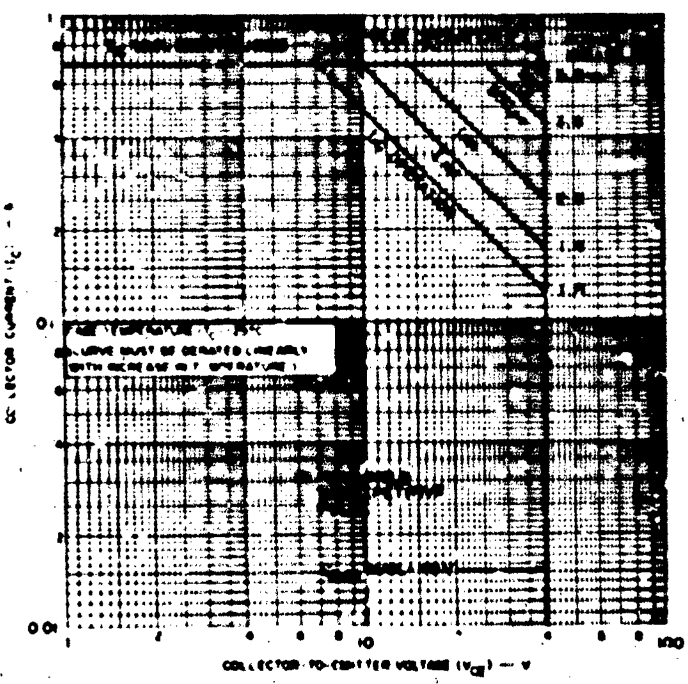


Fig. 5 Maximum operating areas for 2N3053

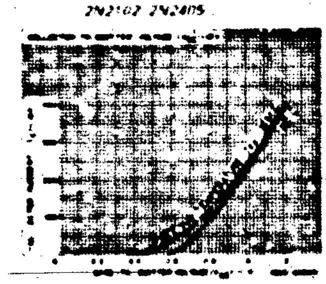


Fig. 8 Typical transfer characteristics for 2N3053, 40389, 40392

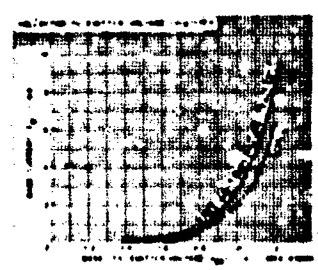


Fig. 9 Typical input characteristics for 2N3053, 40389, 40392

Figure VII-9. 2N3053 Manufacturer Specification Sheet (Continued)

2N697, 2N699, 2N1613, 2N1711, 2N1893, 2N21C2, 2N2270, 2N24C5, 2N3053, 40366, 40389, 40392, 41502

ELECTRICAL CHARACTERISTICS At Case Temperature (T_C) = 25°C unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS VOLTAGE V dc V_{CB}	V_{CE}	CURRENT mA dc I_C	I_B	LIMITS 2N697 MIN	TYP	MAX	2N699 MIN	MAX	2N1613 MIN	MAX	2N2102 40366 MIN	MAX	2N2270 MIN	MAX	UNITS
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Figure VII-9. 2N3053 Manufacturer Specification Sheet (Continued)

2N697, 2N699, 2N1613, 2N1711, 2N1893, 2N2102, 2N2270, 2N2405, 2N3053, 40386, 40389, 40392, 41502

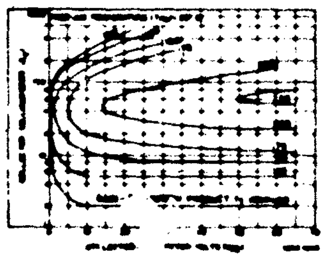


Fig. 10 · Typical gain bandwidth product (f_T) for 2N1711, 2N1893, 2N2405

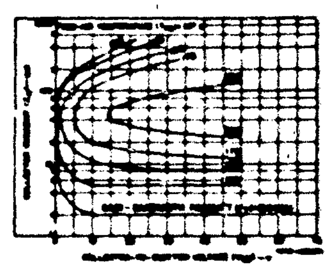


Fig. 11 · Typical gain bandwidth product (f_T) for 2N699, 2N1613, 2N2102, 2N2270, 2N3053, 40389, 40392.

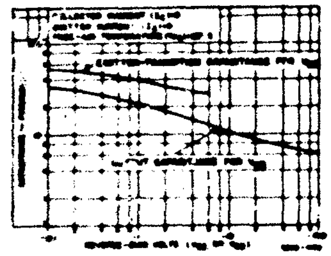


Fig. 12 · Typical capacitance characteristics for all types.

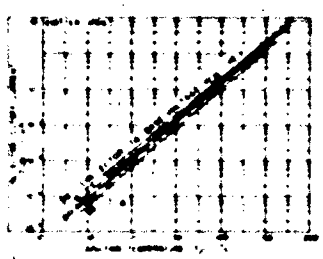


Fig. 13 · Typical collector cutoff current characteristics for 2N699, 2N1893, 2N2405

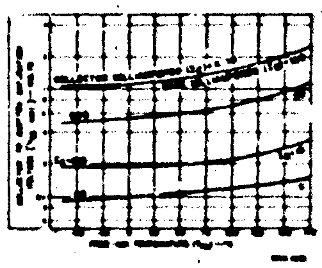


Fig. 14 · Typical collector-to-emitter saturation characteristics for 2N1893, 2N2405.

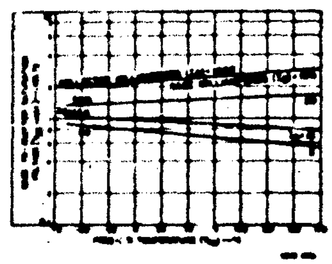


Fig. 15 · Typical base-to-emitter saturation characteristics for 2N1893, 2N2405.

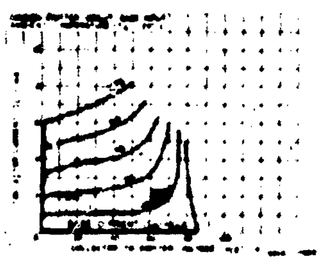


Fig. 16 · Typical low-current output characteristics for 2N697, 2N1613, 2N2102, 2N2270, 41502

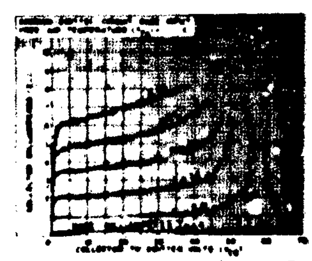


Fig. 17 · Typical low-current output characteristics for 2N1711

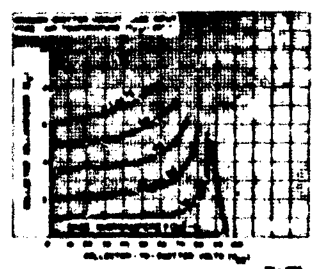


Fig. 18 · Typical low-current output characteristics for 2N1893.

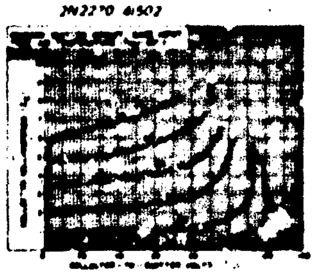


Fig. 19 · Typical low-current output characteristics for 2N2405.

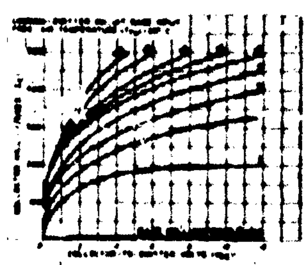


Fig. 20 · Typical high-current output characteristics for 2N699, 2N2270.

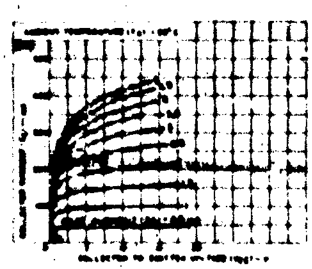


Fig. 21 · Typical high-current output characteristics for 2N1613, 2N2102, 41502.

Figure VII-9. 2N3053 Manufacturer Specification Sheet (Concluded)

POWER TRANSISTORS

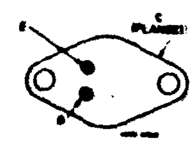
2N3773, 2N4348, 2N6259

Hometaxial-Base, High-Current Silicon N-P-N Transistors

Rugged High Voltage Devices for Applications in Industrial and Commercial Equipment

Features:

TERMINAL DESIGNATIONS



JEDEC TO-3

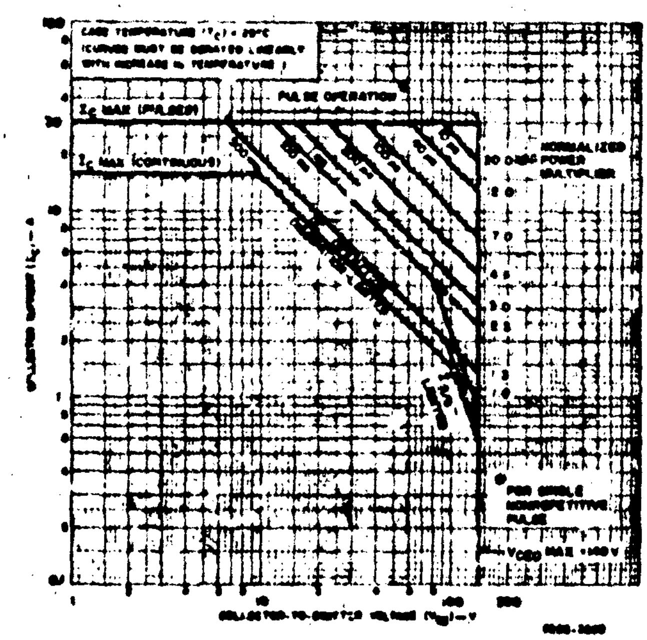


Fig. 1 - Maximum operating areas for 2N3773.

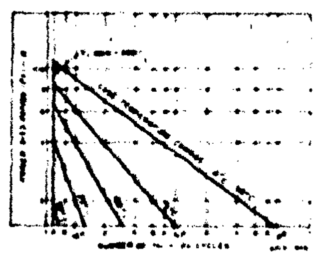


Fig. 2 - Thermal-cycle rating chart for 2N3773

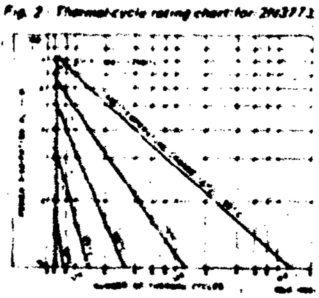


Fig. 3 - Thermal-cycle rating chart for 2N4348

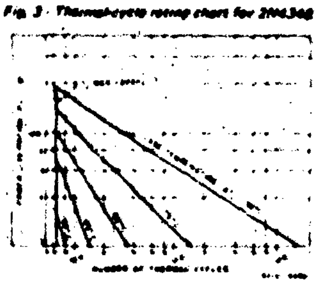


Fig. 4 - Thermal-cycle rating chart for 2N6259

Figure VII-10. 2N3773 Manufacturer Specification Sheet (ref VII-2)

2N3773, 2N4348, 2N6259

ELECTRICAL CHARACTERISTICS At Case Temperature (T_C) = 25°C Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS: VOLTAGE V dc V_{CE}	V_{BE}	CURRENT A dc I_C	I_B	LIMITS: 2N4348 Min	2N4348 Max	2N3773 Min	2N3773 Max	2N6259 Min	2N6259 Max	UNITS
[illegible]	I_{CEO}								[illegible]			mA
[illegible]	I_{CEX}	[illegible]	[illegible]				2		2		[illegible]	mA
[illegible]	I_{CEX}	[illegible]	[illegible]				[illegible]		[illegible]		[illegible]	mA
[illegible]	I_{CEO}	[illegible]					[illegible]		[illegible]		[illegible]	mA
[illegible]	[illegible]		[illegible]	[illegible]			[illegible]		[illegible]		[illegible]	mA
[illegible]	h_{FE}	[illegible]		[illegible]		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
[illegible]	[illegible]		[illegible]	[illegible]		[illegible]		[illegible]		[illegible]		[illegible]
[illegible]	[illegible]	[illegible]		[illegible]					[illegible]			[illegible]
[illegible]	[illegible]			[illegible]	[illegible]				[illegible]			[illegible]
[illegible]	[illegible]	[illegible]				[illegible]		[illegible]		[illegible]		[illegible]
[illegible]	[illegible]		[illegible]	[illegible]		[illegible]		[illegible]		[illegible]		[illegible]
[illegible]	[illegible]	[illegible]		[illegible]		[illegible]		[illegible]		[illegible]		
[illegible]	h_{fe}	[illegible]		[illegible]		[illegible]		[illegible]		[illegible]		
[illegible]	[illegible]						[illegible]		[illegible]		[illegible]	[illegible]

[illegible]

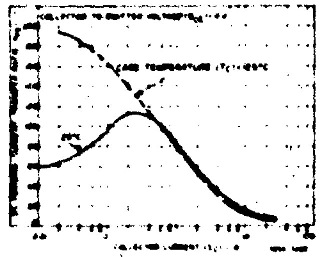


Fig. 5 Typical dc beta characteristics for 2N3773

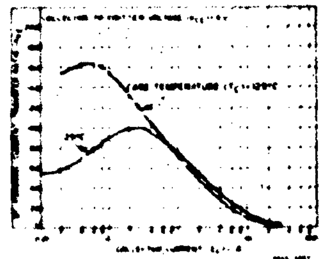


Fig. 6 Typical dc beta characteristics for 2N4348

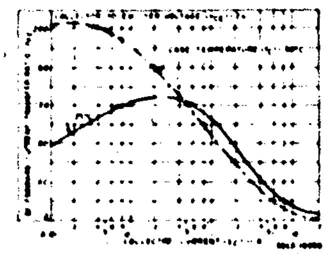


Fig. 7 Typical dc beta characteristics for 2N6259

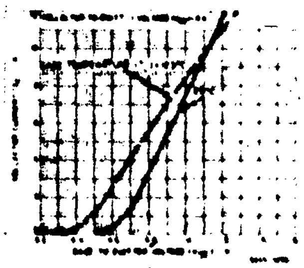


Fig. 8 Typical transfer characteristics for 2N3773

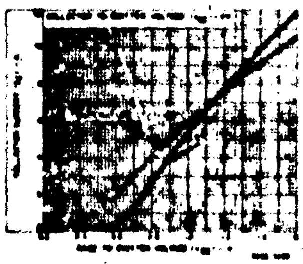


Fig. 9 Typical transfer characteristics for 2N4348

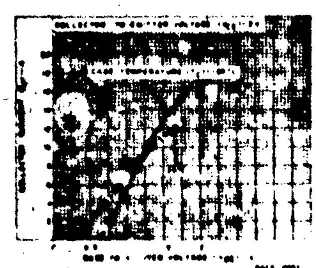


Fig. 10 Typical transfer characteristics for 2N6259

Figure VII-10. 2N3773 Manufacturer Specification Sheet (Continued)

2N3773, 2N4348, 2N6259

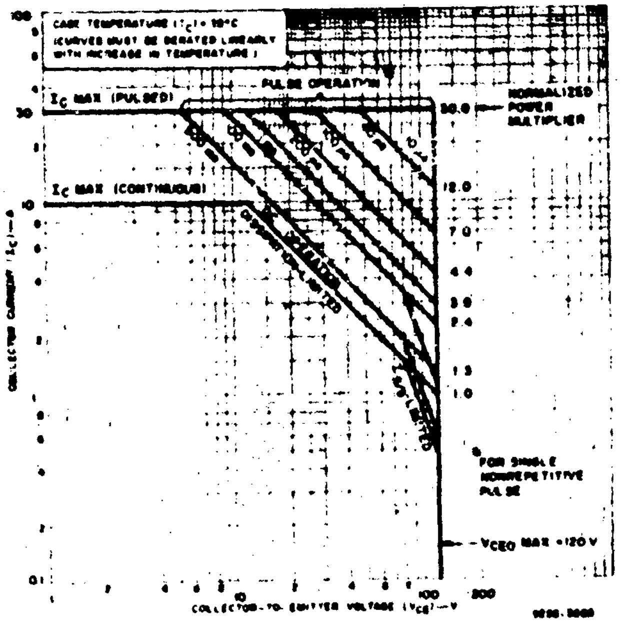


Fig. 11 Maximum operating areas for 2N4348

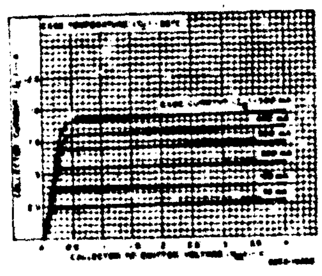


Fig. 12 Typical output characteristics for 2N3773

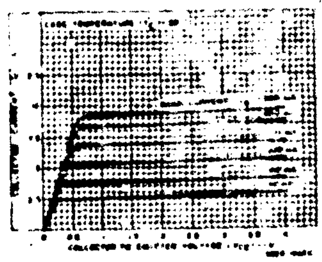


Fig. 13 - Typical output characteristics for 2N4348

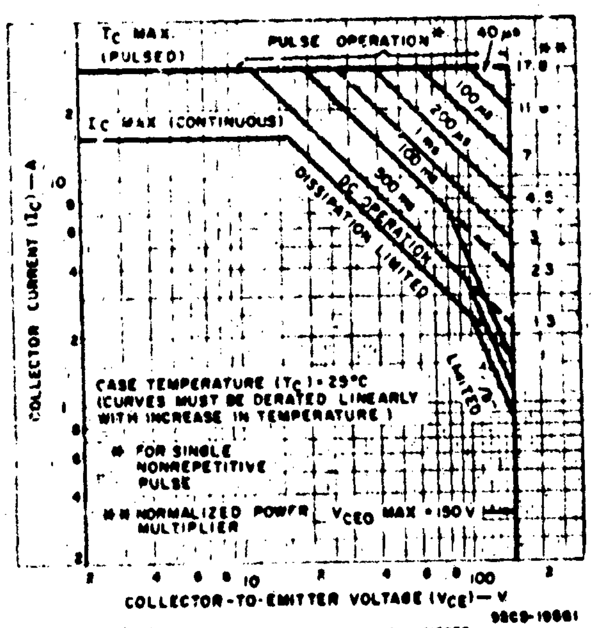


Fig. 14 Maximum operating areas for 2N6259.

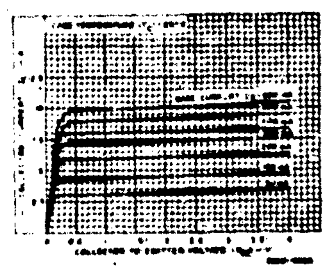


Fig. 15 - Typical output characteristics for 2N6259.

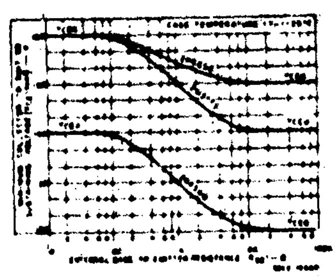


Fig. 16 - Sustaining voltage as a function of base-to-emitter resistance for all types.

Figure VII-10. 2N3773 Manufacturer Specification Sheet (Continued)

2N3773, 2N4348, 2N6259

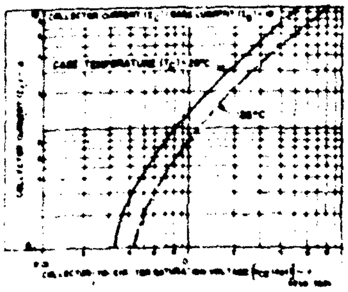


Fig. 17 · Typical saturation-voltage characteristics for 2N3773.

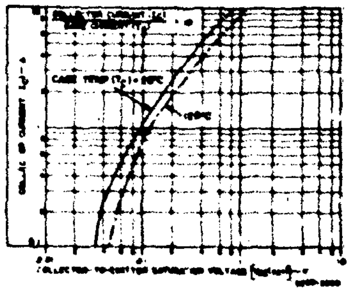


Fig. 18 · Typical saturation-voltage characteristics for 2N4348.

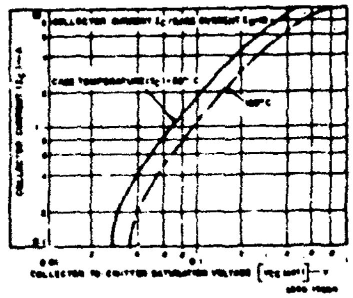


Fig. 19 · Typical saturation-voltage characteristics for 2N6259.

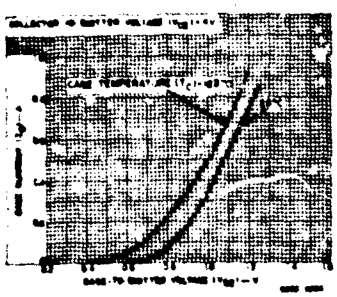


Fig. 20 · Typical input characteristics for 2N3773.

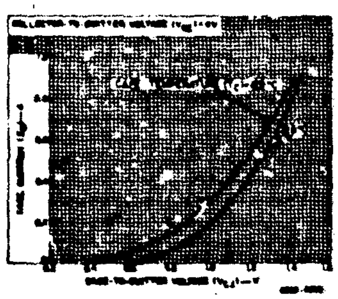


Fig. 21 · Typical input characteristics for 2N4348.

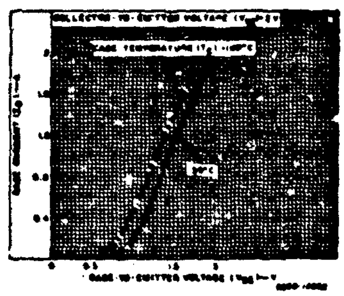


Fig. 22 · Typical input characteristics for 2N6259.

Figure VII-10. 2N3773 Manufacturer Specification Sheet (Concluded).

e. 741 Operational Amplifier

The model of the 741 operational amplifier was composed of a voltage controlled voltage source, an output impedance, and voltage swing limiting zener diodes. Values for the voltage source, which modeled the open loop gain of the device, and the output impedance were obtained in chapter VI. The op amp composite model is shown in figure VII-11.

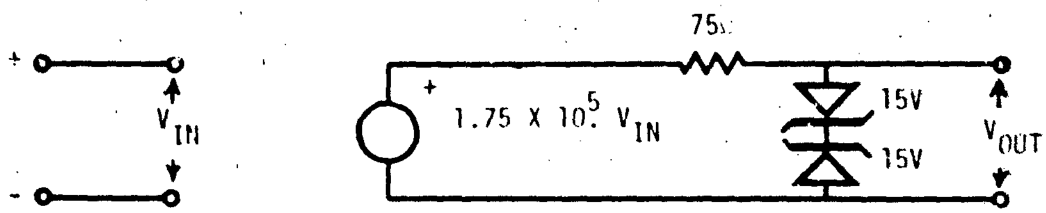


Figure VII-11. 741 Operational Amplifier Model

Only the features of a model which are determined necessary to correctly solve a problem need be included. For this reason, the model shown in figure VII-11 is sufficient as opposed to the more complex model developed in chapter VI. The 741 model developed in chapter VI would only add unnecessary complexity to the power regulator model.

f. 2N5061

The model used for the 2N5061 SCR was the two transistor equivalent circuit. The model SCR is shown in figure VII-12.

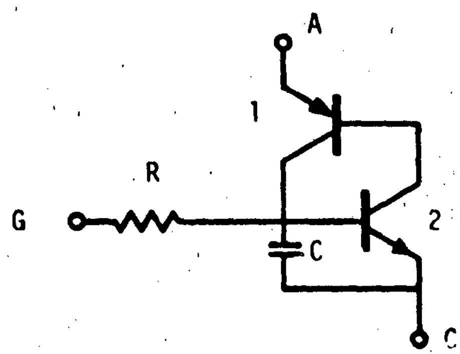


Figure VII-12. Model 2N5061

The manufacturer specification sheets for the 2N5061 (chapter V) are extremely conservative when listing trigger conditions producing much ambiguity in choosing parameters.

In the model which was selected, transistor 1 was chosen with a unity current gain and transistor 2 was chosen with a current gain of 100 which declines to a value of unity at a base and collector current of 1 μA. This implies that the sum of the two alphas will be unity at an anode current of 2 μA. This value is reasonably close to the actual experimental values.

Transistor 2 is based loosely on the 2N2222A model developed in chapter III. The characteristics of transistor 2 are shown in figure VII-13. The SPICE gain parameter C2 was chosen as 1000, a typical value. It can be seen that the other parameters are now fixed.

$$\text{Slope} = \frac{(\ell n\ 1\ \mu A - \ell n\ 3 \times 10^{-11}\ A)}{(0.45\ V - 0\ V)} = 23.1$$

$$N_{EL} = \frac{1}{(0.0259)(23.1)} = 1.67$$

From the 2N2222A model,

$I_S = 3 \times 10^{-14}$ amperes

$\beta_{FM} = 100$

Resistor R and capacitor C were chosen to yield a 1-microsecond time constant.

R = 100 Ω

C = 10 nF

2. Simulations

The first simulation made was simply a verification of correct electrical operation. The power supply was "turned on" and the output voltage was monitored. The computer results are listed in figure VII-14.

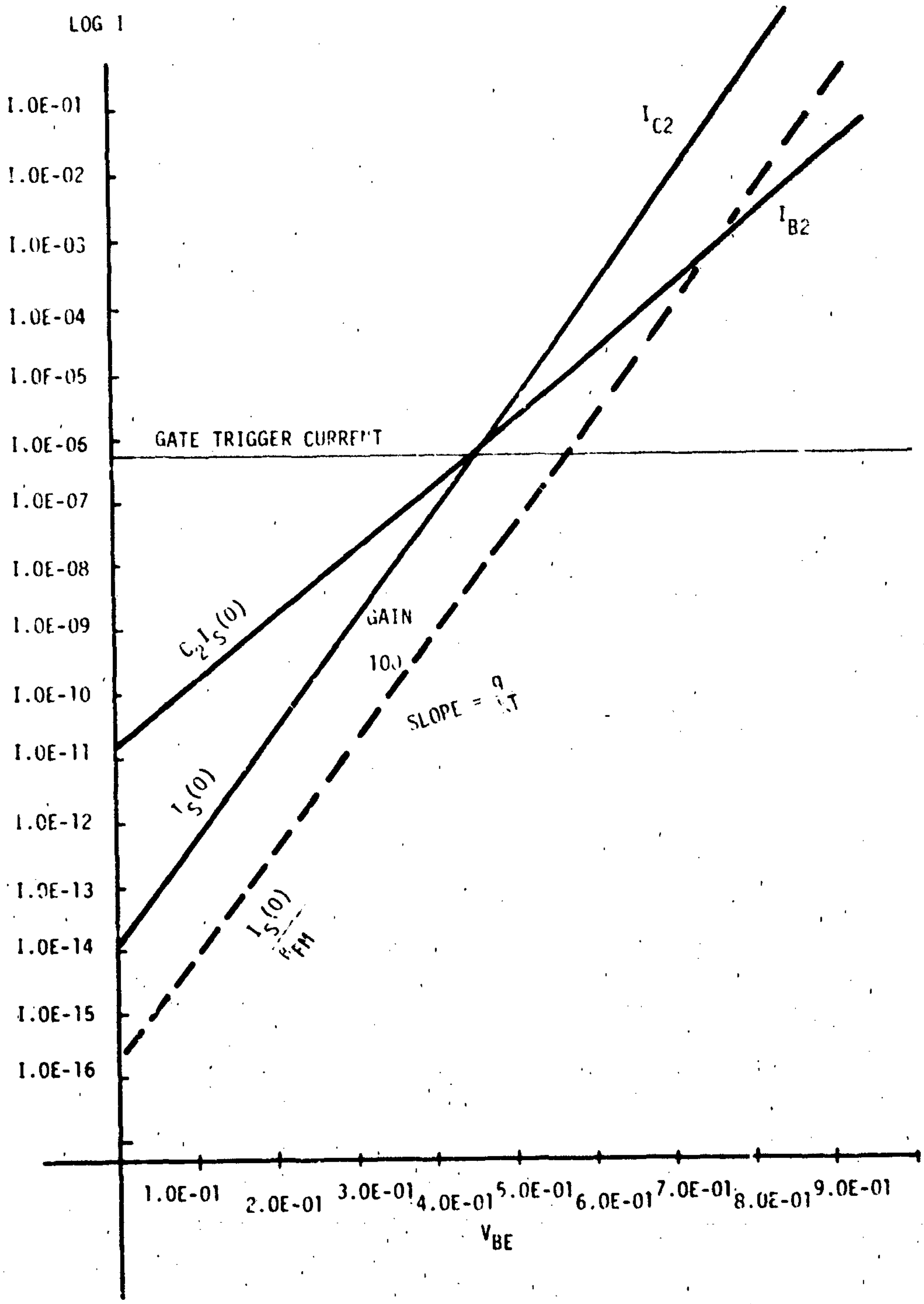


Figure VII-13. Characteristics of Transistor 2

```
***** 03/16/78 ******** SPICE 2D.2 (26SEP76) ******** 08.32.03.*****

*POWER SUPPLY EXAMPLE

     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

*******************************************************************************

.MODEL LIM D(IS=1.E-14 BV=15 IBV=1.E-3)
.MODEL D4001 D(IS=1.E-14)
.MODEL Q3773 NPN(BF=45.71 IS=1.23E-13)
.MODEL Q3053 NPN(BF=104 IS=4.09E-14)
.MODEL ZEN D(IS=1.E-14 BV=5.1 IBV=1.E-3)
.MODEL ZEN2 D(IS=1.E-14 BV=15 IBV=1.E-3)
.MODEL PSCR PNP(BF=1 IS=3.E-14)
.MODEL NSCR NPN(BF=100 IS=3.E-14 C2=1.E3 NE=1.67)
VEMP 19 0 0
VTRAN 1 19 SIN(0 28 400 0 0)
RTRAN 1 2 1
L1 2 0 1
L2 3 4 1
K L1 L2 1
D1 0 3 D4001
D2 3 5 D4001
D3 0 4 D4001
D4 4 5 D4001
L3 5 17 10.E-9
C3 17 0 100.E-6
R3 5 6 15
Q1 5 6 7 Q3773
Q2 6 8 0 Q3053
R4 20 8 100
ROUT 20 9 75
R5 7 11 500
D5 0 11 ZEN
R6 7 10 9600
R7 10 0 10000
L4 7 18 10.E-9
C5 18 0 100.E-6
C4 8 0 0.47E-6
E741 9 0 10 11 1.75E5
RSCR 7 14 1
CSCR 0 13 1.E-8
Q3 13 12 14 PSCR
Q4 12 13 0 NSCR
R8 15 0 1000
D6 15 7 ZEN2
RTHI 15 13 100
D7 20 16 LIM
D8 0 16 LIM
RL 7 0 2
.OPTIONS ITL5=10000
.TRAN 1.E-5 1.E-3
.PLOT TRAN V(7)
.END
```

Figure VII-14. Power Supply "Turn On"

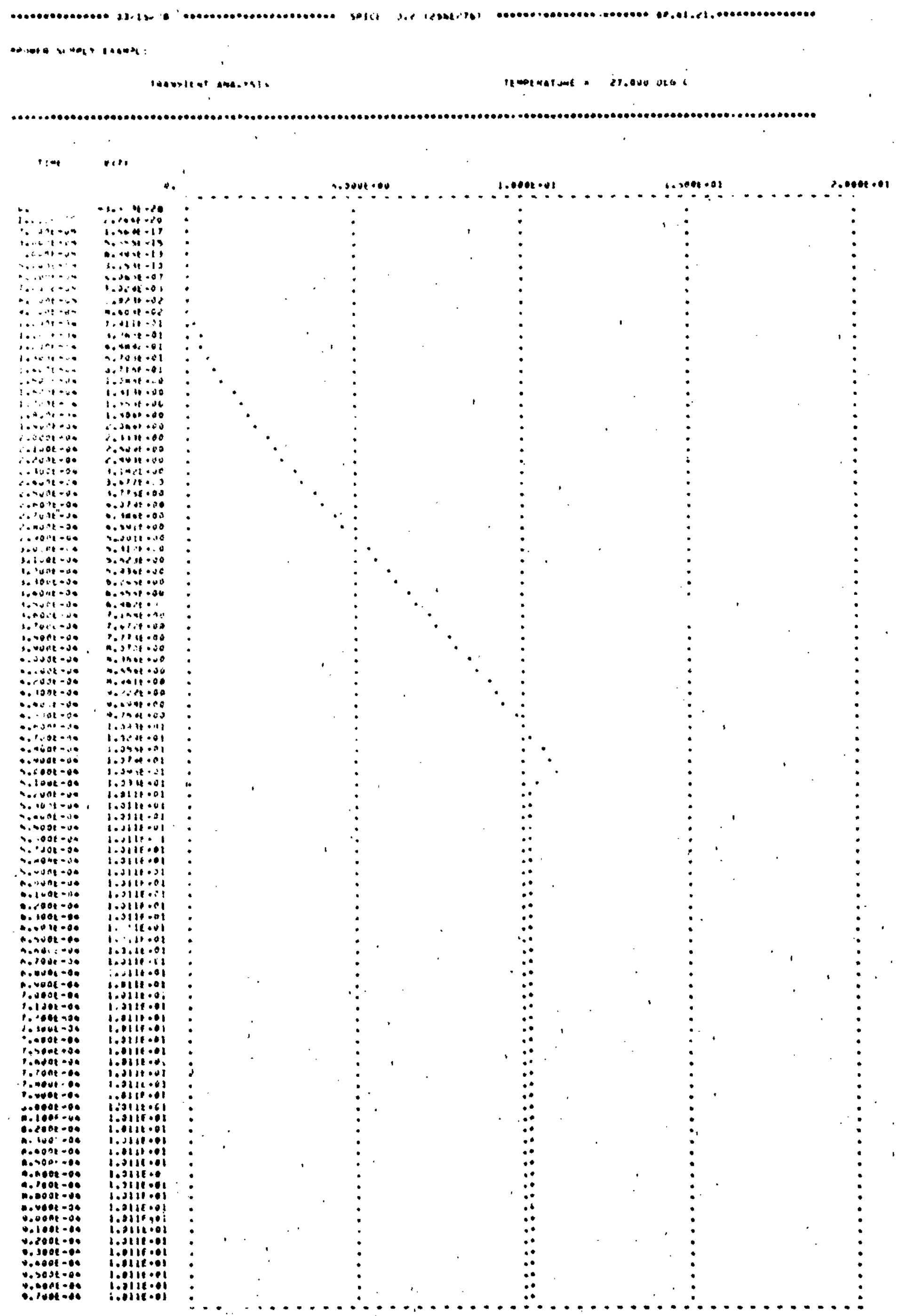


Figure VII-14. Power Supply "Turn On" (Concluded)

For the next simulation, the response of the power supply to a neutron fluence of 6×10^{11} cm^2 was desired. Because the f_T of the 2N3773 (200 kHz) is much lower than the f_T of the 2N3053 (100 MHz), the 2N3773 will be orders of magnitude more susceptible to neutron damage. Therefore, the simulation need only be concerned with the 2N3773 series pass transistor. At 6×10^{11} n/cm^2

$$\frac{1}{\beta_\phi} = \frac{(10^{-6})(6 \times 10^{11})}{2\pi\ (200\ \text{kHz})} + \frac{1}{45.71}$$

$$\beta_\phi = 2$$

The power supply output voltage was monitored with the degraded β value The computer simulation of figure VII-15 indicates that at a neutron fluence of 6×10^{11} n/cm^2, the power regulator will fail to supply 10 volts to a 2-ohm load.

Is it true that power regulators should be able to reject an overstress waveform coupled through the transformer? To test this idea, the overstress signal shown in figure VII-16 was applied to the transformer primary. An added complication to this simulation is the inductive behavior of electrolytic capacitors at high frequencies. This problem was solved with the addition of parasitic inductors in series with the 100 μF capacitors. The problem of parasitics should always be considered. Ideally, for EMP analysis, the parasitic structure of the transformer should be determined.

Figure VII-17 is the computer simulation of the problem. The output is a simultaneous plot of the power regulator output and the overstress signal. It can be seen that this particular overstress signal would not upset the power regulator.

The final simulation is a test to see if an ionizing dose rate of 1×10^{10} rad (Si)/sec is sufficient to cause the SCR to fire and shut down the power supply.

```
***** 03/15/78 ********  SPICE 2D.2 (26SEP76)  ******** 09.10.29.*****

*POWER SUPPLY EXAMPLE

     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

**********************************************************************


.MODEL LIM D(IS=1.E-14 BV=15 IBV=1.E-3)
.MODEL D4001 D(IS=1.E-14)
.MODEL Q3773 NPN(BF=2. IS=1.23E-13)
.MODEL Q3053 NPN(BF=104 IS=4.09E-19)
.MODEL ZEN D(IS=1.E-14 BV=5.1 IBV=1.E-3)
.MODEL ZEN2 D(IS=1.E-14 BV=15 IBV=1.E-3)
.MODEL PSCR PNP(BF=1 IS=3.E-14)
.MODEL NSCR NPN(BF=130 IS=3.E-14 C2=1.E3 NE=1.57)
IPP 12 13 0
VEMP 19 0 0
VTRAN 1 19 SIN(0 29 400 0 0)
RTRAN 1 2 1
L1 2 0 1
L2 3 4 1
K L1 L2 1
D1 0 3 D4001
D2 3 5 D4001
D3 0 4 D4001
D4 4 5 D4001
L3 5 17 10.E-9
C3 17 0 100.E-6
R3 5 6 15
Q1 5 6 7 Q3773
Q2 6 8 0 Q3053
R4 20 8 100
ROUT 20 9 75
R5 7 11 500
D5 0 11 ZEN
R6 7 10 9000
R7 10 0 10000
L4 7 18 10.E-9
C5 18 0 100.E-6
C4 8 0 0.47E-6
E741 9 0 10 11 1.75E5
RSCR 7 14 1
CSCR 0 13 1.E-8
Q3 13 12 14 PSCR
Q4 12 13 0 NSCR
R8 15 0 1000
D6 15 7 ZEN2
RTHY 15 13 100
D7 20 16 LIM
D8 0 16 LIM
RL 7 0 2
.OPTIONS ITL5=10000
.TRAN 1.E-4 1.E-2
.PLOT TRAN V(7)
.END
```

Figure VII-15. Power Supply Output After Neutron Exposure

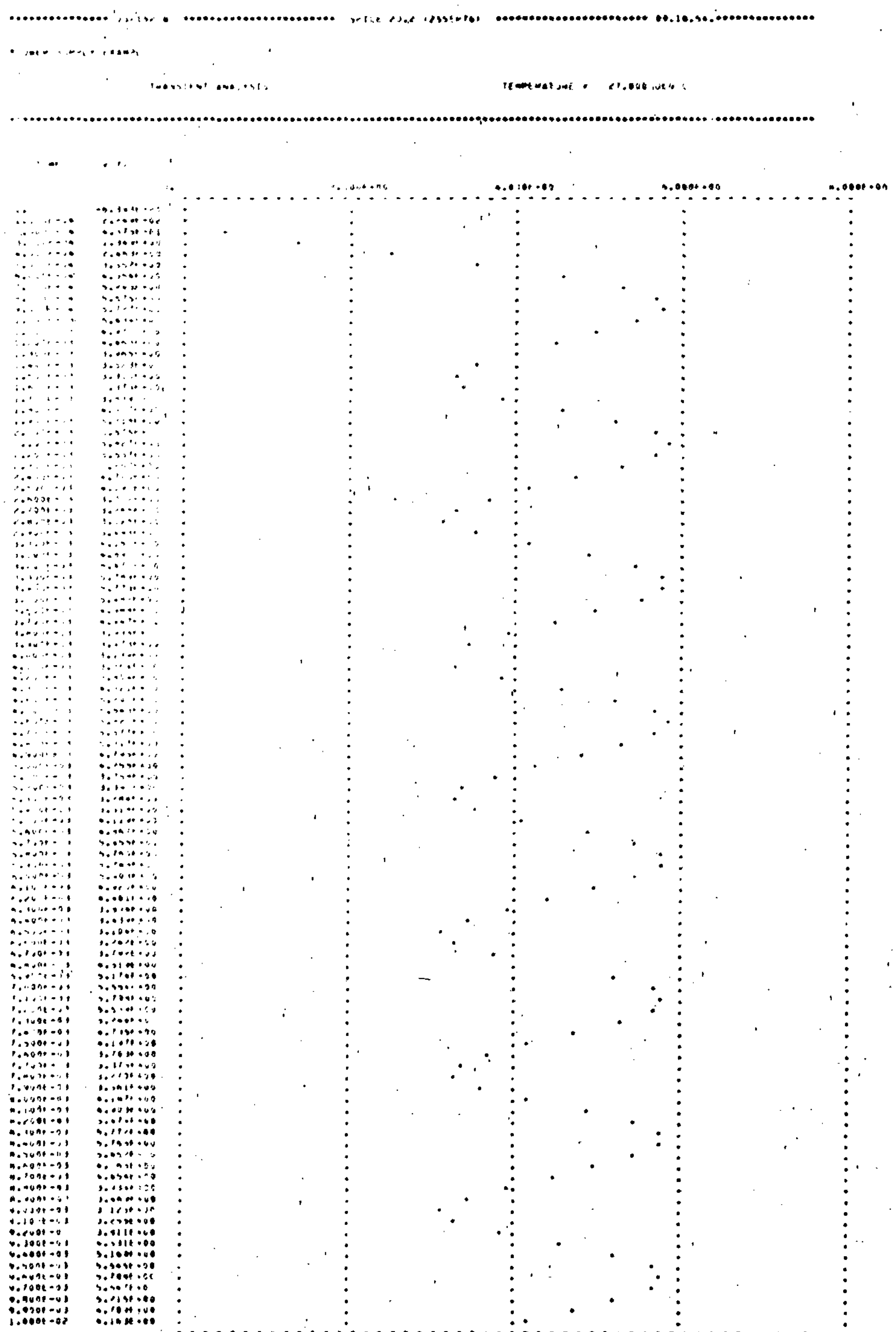


Figure VII-15. Power Supply Output After Neutron Exposure (Concluded)

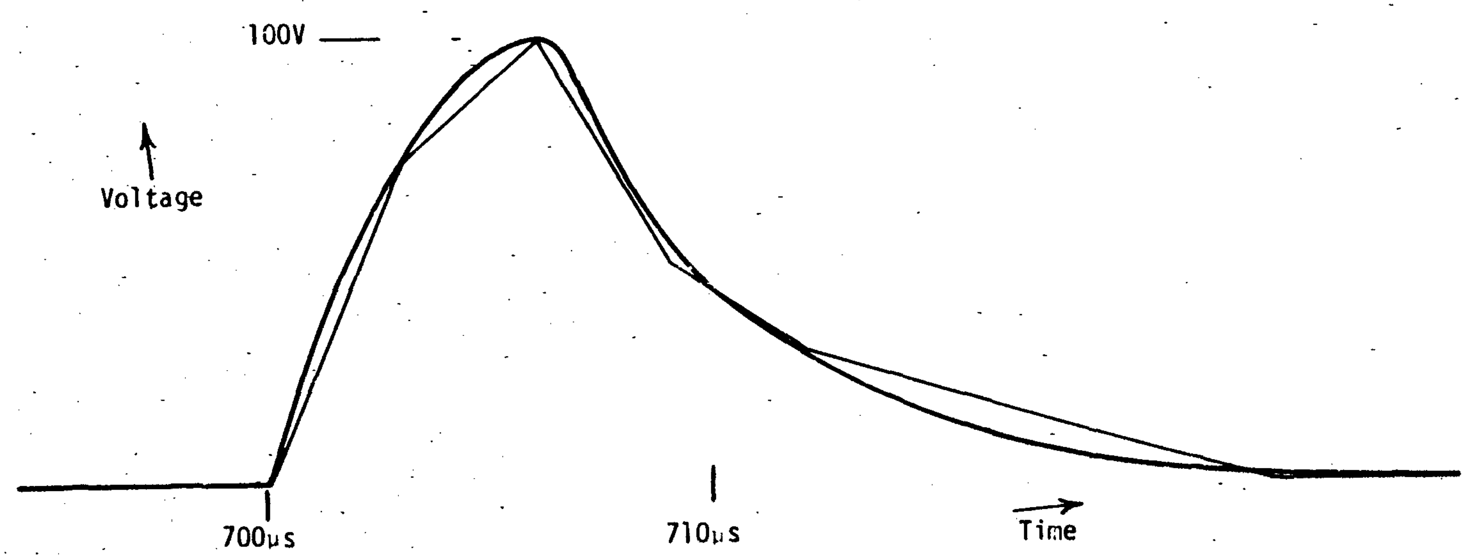


Figure VII-16. Overstress Signal and Tabular Representation

```
***** 03/16/78 ******** SPICE 2D.2 (26SEP76) ******** 09.21.45.*****

*POWER SUPPLY EXAMPLE

     INPUT LISTING                    TEMPERATURE =   27.000 DEG C

**********************************************************************

.MODEL LIM D(IS=1.E-14 BV=15 IBV=1.E-3)
.MODEL D4001 D(IS=1.E-14)
.MODEL Q3773 NPN(BF=45.71 IS=1.23E-13)
.MODEL Q3053 NPN(BF=104 IS=4.09E-14)
.MODEL ZEN D(IS=1.E-14 BV=5.1 IBV=1.E-3)
.MODEL ZEN2 D(IS=1.E-14 BV=15 IBV=1.E-3)
.MODEL PSCR PNP(BF=1 IS=3.E-14)
.MODEL NSCR NPN(BF=130 IS=3.E-14 C2=1.E3 NE=1.67)
IPP 12 13 0
VEMP 19 0 PWL(0 0 7.E-4 0 7.3E-4 70 7.5E-4 100 7.9E-4 30 8.2E-4 30
+        9.2E-4 0 1.E-3 0)
VTRAN 1 19 SIN(0 29 400 0 0)
RTRAN 1 2 1
L1 2 0 1
L2 3 4 1
K L1 L2 1
D1 0 3 D4001
D2 3 5 D4001
D3 0 4 D4001
D4 4 5 D4001
L3 5 17 10.E-9
C3 17 0 100.E-6
R3 5 6 15
Q1 5 6 7 Q3773
Q2 6 8 0 Q3053
R4 20 8 100
ROUT 20 9 75
R5 7 11 500
D5 0 11 ZEN
R6 7 10 9600
R7 10 0 10000
L4 7 18 10.E-9
C5 18 0 100.E-6
C4 8 0 0.47E-6
E741 9 0 10 11 1.75E5
RSCR 7 14 1
CSCR 0 13 1.E-8
Q3 13 12 14 PSCR
Q4 12 13 0 NSCR
R8 15 0 1000
D6 15 7 ZEN2
RTHY 15 13 100
D7 20 16 LIM
D8 0 16 LIM
RL 7 0 2
.OPTIONS ITL5=10000
.TRAN 1.E-5 1.E-3
.PLOT TRAN V(7) V(19)
.END
```

Figure VII-17. Response of Power Regulator to EMP

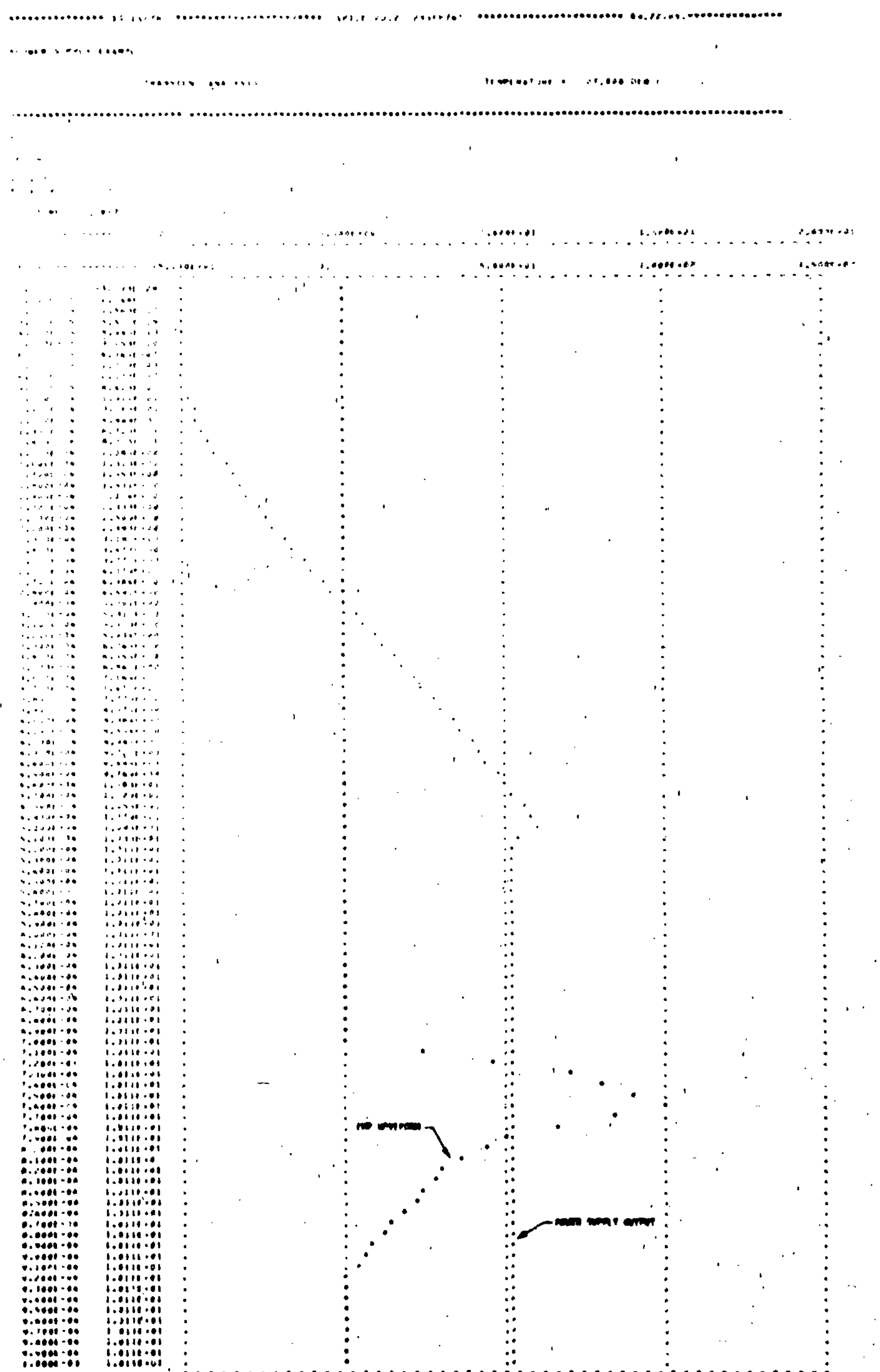


Figure VII-17. Response of Power Regulator to EMP (Concluded)

Experimental data for this test are in the form of the photograph shown in figure VII-18. The photograph represents the anode photocurrent produced at a dose rate of 1×10^{10} rad (Si)/sec. In the test configuration, the anode was supplied with 10 volts, the gate was grounded, and the cathode was left open. The anode current probe had a response of 5 mV/mA. The peak photocurrent produced is 600 mA.

This photocurrent can be included in the thyristor model as a current generator placed between the two transistor collectors (refer to chapter V).

To produce the observed 600 mA of anode current, the simple 2N5061 model photocurrent generator would be required to generate one-half of this value or 300 mA. This is expressed mathematically by:

$$I_A = I_E = (1 + \beta)\, I_B$$

where the parameters refer to the PNP transistor.

To see if the SCR will fire at a dose rate of 1×10^{10}, it was necessary to artificially set the photocurrent pulse length long enough to charge the arbitrarily chosen R-C model time constant of 1 microsecond. The simulated photocurrent waveform chosen was a triangular pulse rising to 300 mA in 1 microsecond and then falling to zero in 1 microsecond.

When making the simulation, it was discovered that the behavior of the 741 during the transient would cause the code to revert to a very small time step, effectively stopping simulation. This problem was alleviated by placing the voltage swing limiting diodes behind the 100 ohm resistor.

The results of the simulation are shown in figure VII-19. The predicted response is an SCR firing at a dose rate of 1×10^{10} rad (Si)/sec.

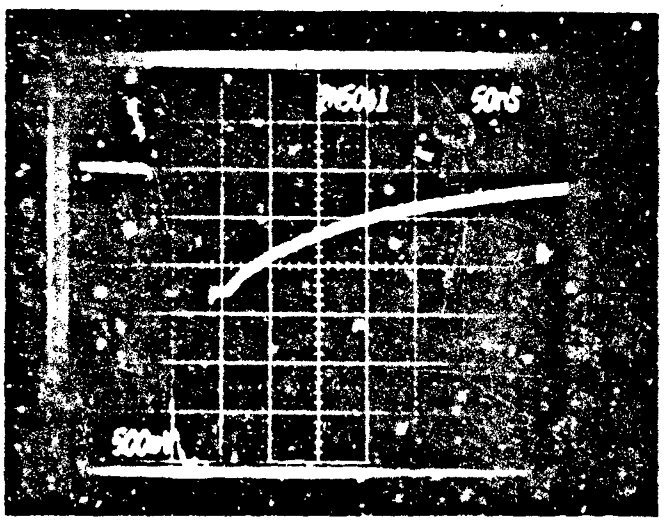


Figure VII-13. 2N5061 Radiation Response

```
***** 03/20/78 ********  SPICE 2D.2 (26SEP76)  ******** 08.21.33.*****

*POWER SUPPLY EXAMPLE

     INPUT LISTING                         TEMPERATURE =   27.000 DEG C

**************************************************************************

.MODEL LIM D(IS=1.E-14 BV=15 IBV=1.E-3)
.MODEL D4001 D(IS=1.E-14)
.MODEL Q3773 NPN(BF=55.71 IS=1.23E-13)
.MODEL Q3054 NPN(BF=104 IS=4.09E-14)
.MODEL ZEN D(IS=1.E-14 BV=5.1 IBV=1.E-3)
.MODEL ZEN2 D(IS=1.E-14 BV=15 IBV=1.E-3)
.MODEL PSCR PNP(BF=1 IS=3.E-14)
.MODEL NSCR NPN(BF=130 IS=3.E-14 C2=1.53 NE=1.67)
IPP 12 13 PWL(0 0 7.E-6 0 7.01E-6 0.3 7.02E-6 0 8.E-6 0)
VEMP 19 0 0
VTRAN 1 19 SIN(0 28 400 0 0)
RTRAN 1 2 1
L1 2 0 1
L2 3 4 1
K L1 L2 1
D1 0 3 D4001
D2 3 5 D4001
D3 0 4 D4001
D4 4 5 D4001
C1 5 17 10.E-9
C3 17 0 100.E-6
R1 5 6 15
Q1 5 6 7 Q3773
Q2 6 8 0 Q3054
R4 20 8 100
ROUT 20 9 75
R5 7 11 500
D5 0 11 ZEN
R6 7 10 9600
R7 10 0 10000
C4 7 18 10.E-9
C5 18 0 100.E-6
C6 8 0 0.47E-6
E741 9 0 10 11 1.75E5
RSCR 7 14 1
CSCR 0 13 1.E-8
Q3 13 12 14 PSCR
Q4 12 13 0 NSCR
R8 15 0 1000
D6 15 7 ZEN2
RTHY 15 13 150
D7 8 16 LIM
D8 0 16 LIM
RL 7 0 2
.OPTIONS ITL5=50000
.TRAN 1.E-5 1.E-3
.PLOT TRAN V(7)
.END
```

Figure VII-19. SCR Triggering by Ionizing Radiation

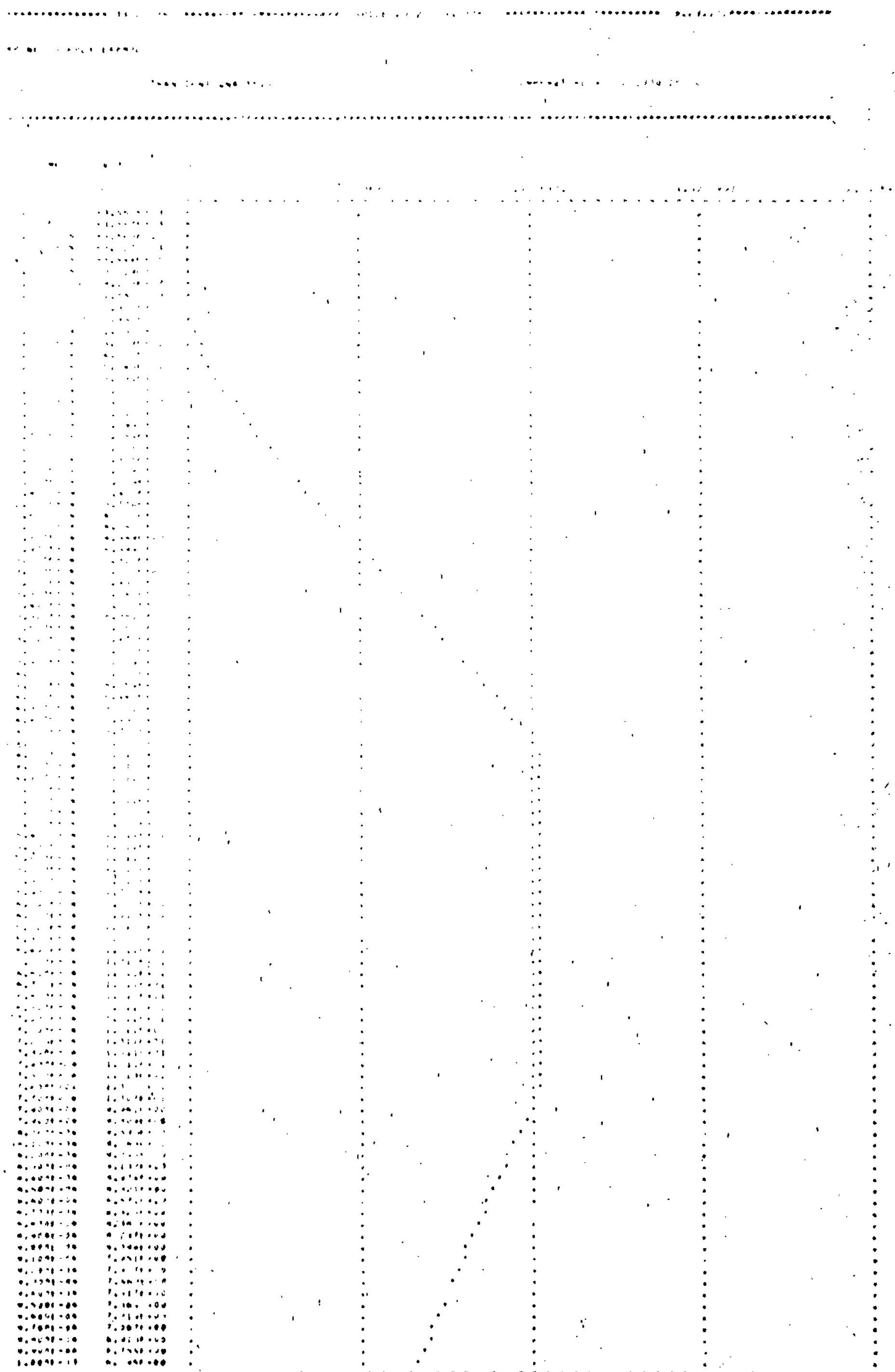


Figure VII-19. SCR Triggering by Ionizing Radiation (Concluded)

C. EFFECT OF IONIZING RADIATION ON ELECTRONIC INTEGRATOR

Simplified models require radiation responses to be built into the model. The information on which to base the radiation response must come from experimental data. This example illustrates how the transient ionizing response may be built into the model for the 741 operational amplifier.

The response of a μA741DC operation amplifier to transient ionizing radiation is desired. The op amp is in an integrator configuration as illustrated by figure VII-20. The op amp model is shown in figure VII-21.

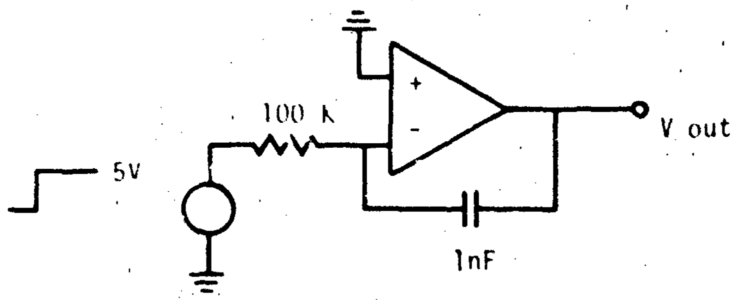
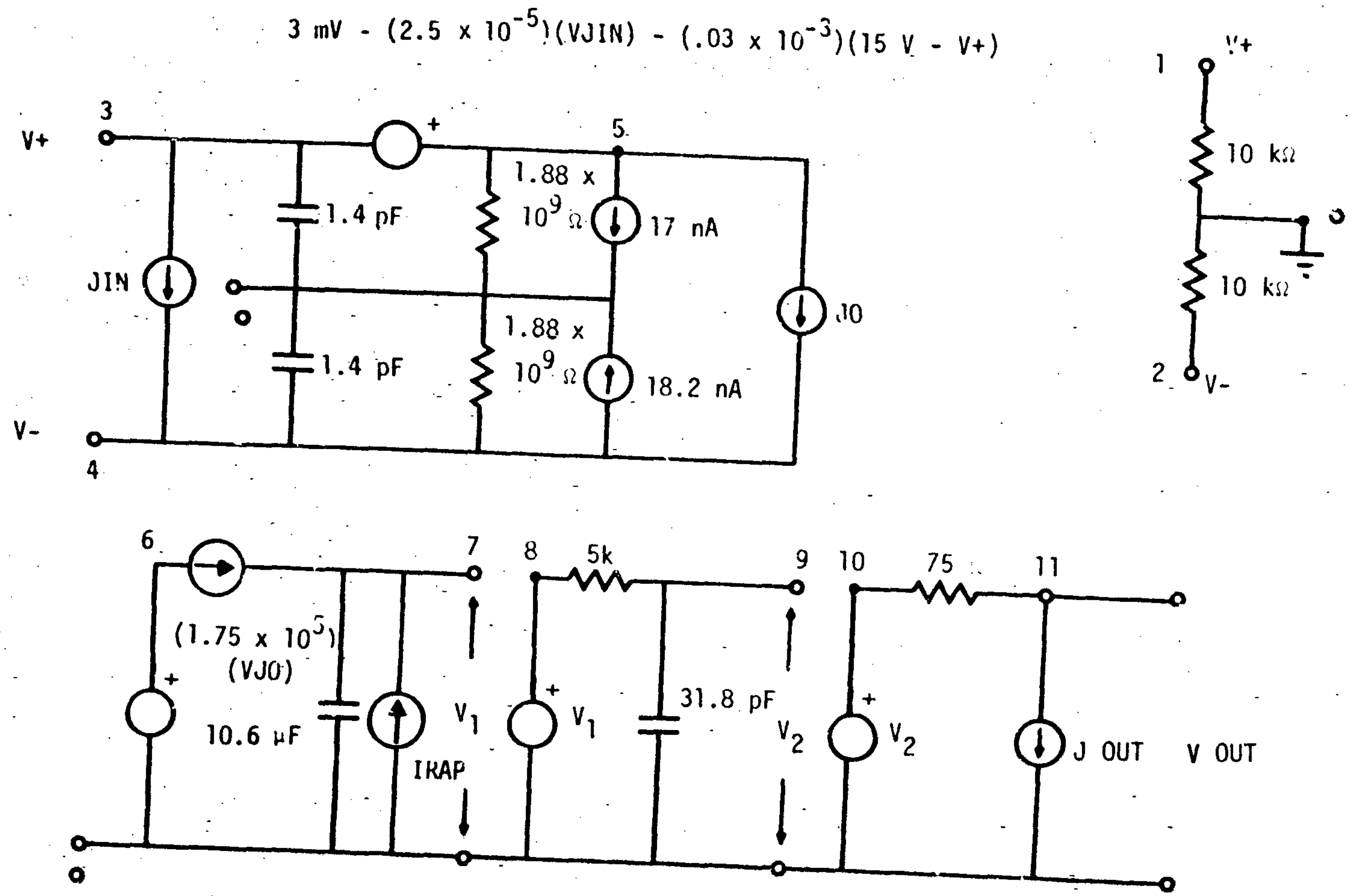


Figure VII-20. Integrator Circuit

In chapter VI.A.5, a method of building in a photoresponse of the 741DC operational amplifier model is discussed. The experimental waveform to be duplicated is from a test where the ionizing radiation caused the amplifier output to rise at a rate of 1 V/μs, saturate for 10 μs, and then recover at the slew rate.

To produce the 1 V/μs rise rate, a value of IRAD is required which satisfies (see chapter VI.A.5)

$$\frac{dV}{dT} = \frac{1\ V}{\mu s} = \frac{IRAD - 5.3\ A}{10.6\ \mu F}$$



IF V out > V(+)-1.0V, THEN Vout = V(+)-1V

IF V out < V(-)+2.5V, THEN Vout = V(-)+2.5V

Figure VII-21. Model µA741 with Photoresponse

An IRAD value of 15.9 amps will meet this condition. When the output voltage climbs above 15 V, saturation is modeled. However, the 10.6 μF capacitor charged by IRAD will continue to climb above 15 volts. IRAD must be stopped at the proper time so that the 10.6 μF capacitor, discharging at the slew rate of 0.5 V/μs, will fall below 15 V, 10 μs after first reaching 15 V, to model the saturation delay time. The amplifier will now recover at the slew rate which is desirable.

The complete simulation waveform is shown in figure VII-22. At time zero, IRAD is set to 15.9 amps. The output will rise at a rate of 1 V/μs and saturate in 15 μs. Setting IRAD back to zero in 18.33 μs will allow the op amp to recover at the slew rate, coming out of saturation in 25 μs or 10 μs after entering saturation. The op amp does not recover completely until 55 μs following the radiation pulse.

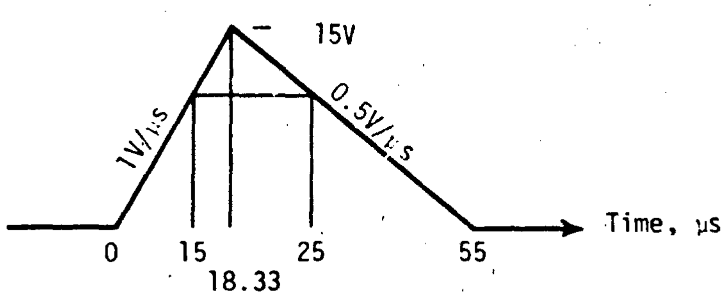


Figure VII-22. Op Amp Response

The response of the integrator may now be investigated. Figure VII-23 is the listing for the SCEPTRE run. Figure VII-24 is the predicted output response for the integrator.

The interesting result of this run is that following the radiation pulse, the integrator output is only slightly shifted. However, the error is propagated by the integrator for a time much longer than the amplifier upset time. What the integrator is driving now becomes important. If no error is to be tolerated, a seriously long upset has been produced.

```
SUBPROGRAM
      FUNCTION FOUT(VO,VP,VN)
      FOUT=VO
      VSP=VP-1.0
      VSN=2.5-VN
      IF (VO.GT.VSP) FOUT=VSP
      IF (VO.LT.VSN) FOUT=VSN
      IF (VO.GT.VSP.AND.VO.LT.VSN) FOUT=0
      RETURN
      END
CIRCUIT DESCRIPTION
ELEMENTS
RSS,1-0=10.E3
RPSS,0-2=10.E3
CINP,3-0=1.4E-12
CINN,0-4=1.4E-12
JIN,3-4=0
EINP,3-5=X1(3.E-3-2.5E-5*VJIN-30.E-6*(15.-VRSS))
RINP,5-0=1.88E9
RINN,0-4=1.88E9
JOFP,5-0=17.E-9
JOFN,4-0=18.2E-9
J0,5-4=0
E0,0-6=X2(1.75E5*VJ0)
J1,6-7=TABLE 1(VJ1)
C1,7-0=10.6E-6
E1,0-8=X3(VC1)
R2,8-9=5.E3
C2,9-0=31.8E-12
EOUT,0-10=FOUT(VC2,VRSS,VRPSS)
ROUT,10-11=75.
JOUT,11-0=0
EPLUS,0-1=15
EMINUS,2-0=15
R0,0-3=.001
ESIG,0-X=5.
RBIAS,X-4=1.E5
CBIAS,11-4=1.E-9
JRAD,0-7=TABLE 2(TIME)
FUNCTIONS
TABLE 1
-5.E4,-5.3,-2.66E4,-5.3,2.66E4,5.3,5.E4,5.3
TABLE 2
0,0,.5E-4,0,.5E-4,15.9,.6833E-4,15.9,.6833E-4,0,1.E-4,0
OUTPUTS
ESIG,EINP,EOUT,VJOUT,PLOT
RUN CONTROLS
STOP TIME=2.E-4
END
```

Figure VII-23. Listing for Integrator Response

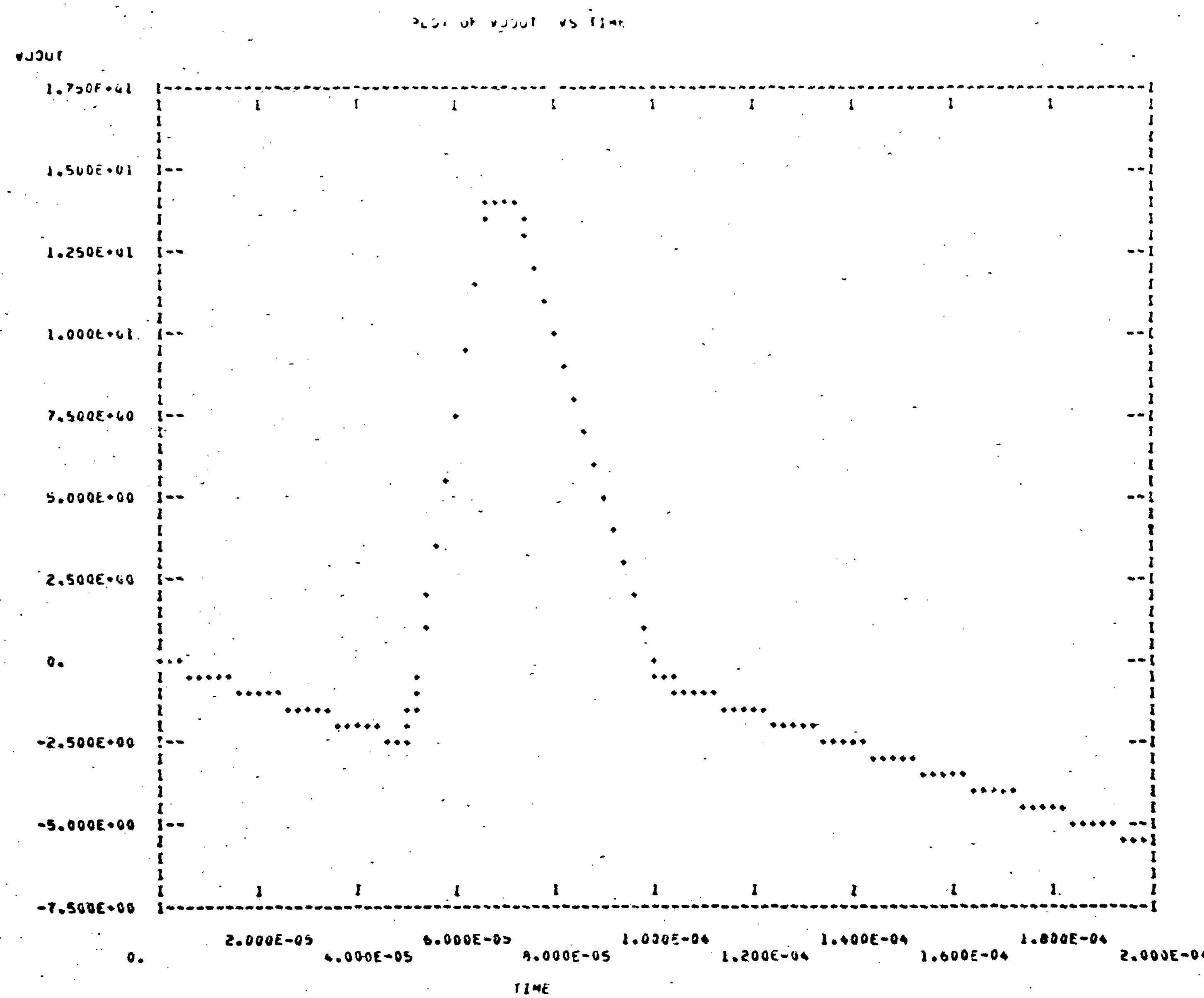


Figure VII-24. Predicted Integrator Response

This simulation represents a problem which would be difficult to solve through manual analysis. Computer simulation is useful for verifying manual analysis as well as solving the more difficult problems.

D. COMPUTER AIDED ANALYSIS AS A TOOL FOR HARDENING ELECTRONIC SYSTEMS

This example is an illustration of how computer aided analysis was applied to harden an electronic system. The circuit which was analyzed is the three stage amplifier shown in figure VII-25. The neutron degradation analysis concerned the power transistors T3, T4, and T5. At a neutron fluence of 5×10^{11} n/cm^2, the circuit was shown to be vulnerable. Failure was reached when the gain at 2 kHz fell below 10. Neutron degradation was estimated from information on device f_T.

To harden this circuit, piecepart substitutions were made until a fluence of 5×10^{11} n/cm^2 did not degrade the performance of the amplifier below design limits.

Parameters for the transistors were obtained from data sheet information. When parameters were not directly available from data sheets, default values were used.

Care was required in modeling transformers TR2 and TR3 and transistors T4 and T5 to avoid an unstable circuit. Since transistors T4 and T5 are operated near cutoff, the modeling of current gain as a function of base emitter voltage is important.

Transformer parameters such as turns ratio, winding inductance, winding resistance, coefficient of coupling, and frequency response were not available from the data sheets. The equipment manufacturer was very helpful in providing specifications for these devices. The ratio of coil inductance can be approximated from the rated primary and secondary impedances or turns ratio as:

$$\frac{L_2}{L_1} = \frac{Z_2}{Z_1} = \left(\frac{N_2}{N_1}\right)^2$$

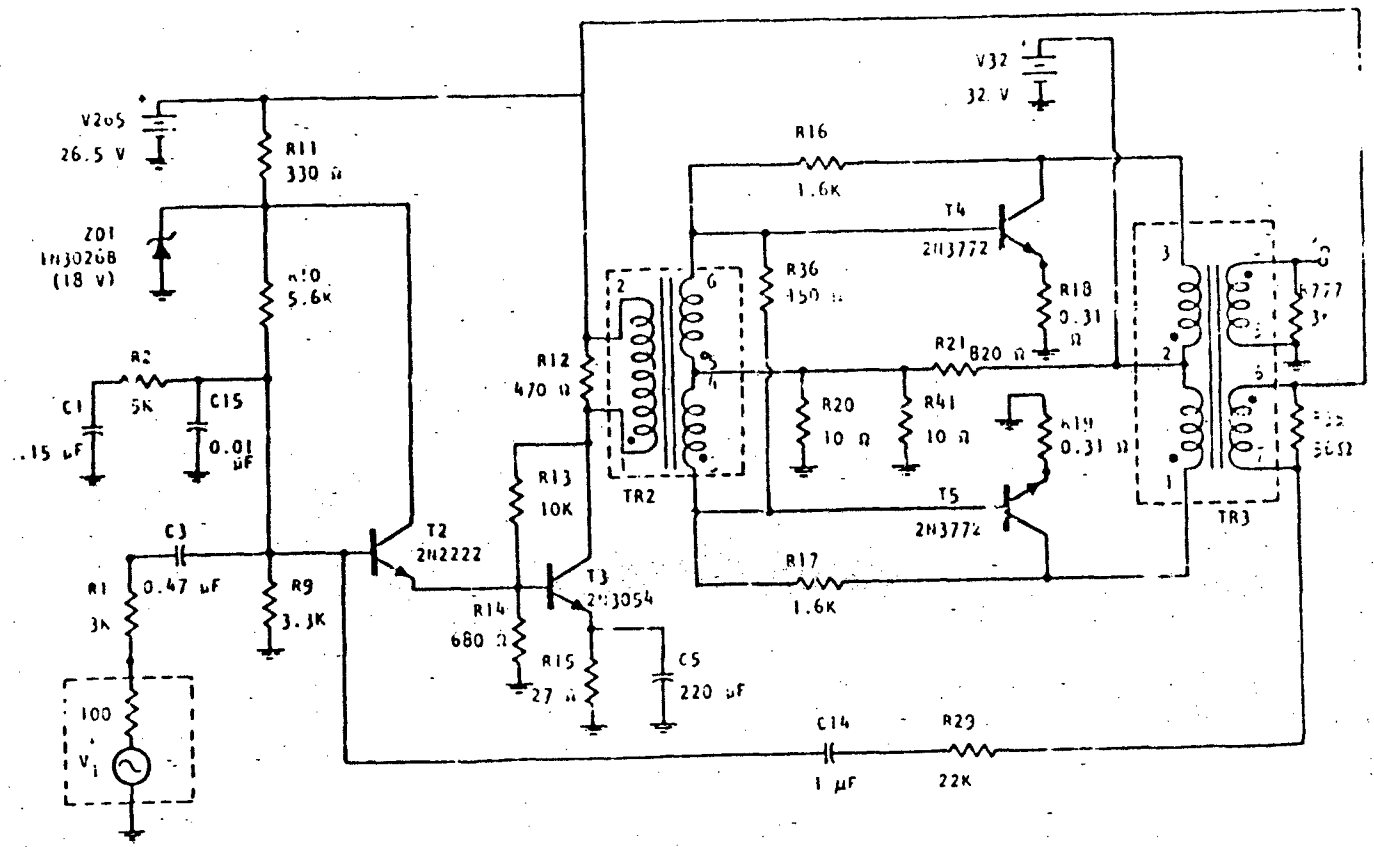


Figure VII-25. Three-Stage Amplifier

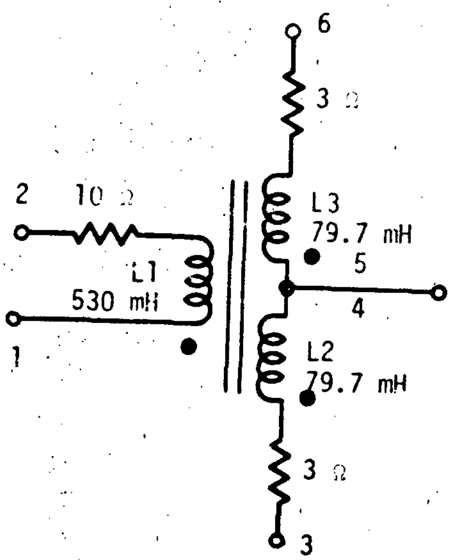
The values of inductance are not critical if they are large enough to present impedances greater than the rated driving source impedance within the required frequency range. The inductances were therefore chosen to yield an inductive reactance of 10 times the rated winding impedance at the low end of the rated transformer pass bands. The winding resistances were taken from the specification sheets for the transformers, and the coefficient of coupling was taken as high as possible. NET-2 requires K to be less than one. A K of 0.99 resulted in an unstable circuit, so K was chosen as 0.9. The transformer models are shown in figure VII-26.

The three stage amplifier was hardened by replacing the [illegible] and 2N3772 transistors with 2N5427 and 2N5038 transistors, respectively. Tables VII-1 and VII-2 give a comparison of the major parameters including cost. Except for the small decrease in rated power of the 2N5038 (140 watts) compared to that of the 2N3772 (150 watts), the substitute transistors are equally or higher rated in every category. Figure VII-27 shows the modified circuit.

The frequency domain capability of NET-2 was used to obtain the transfer characteristics of both amplifiers. Figure VII-28 shows the preirradiation frequency response of both the original and hardened amplifiers.

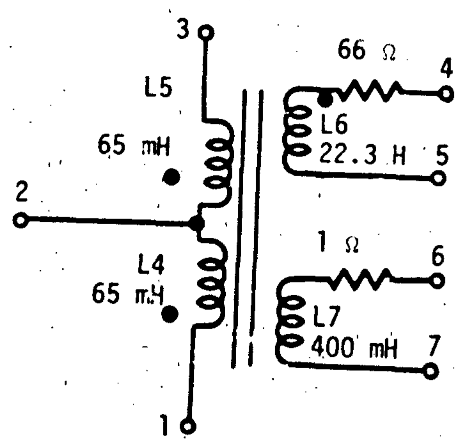
The peaked frequency response illustrates one of the major problems in circuit simulation, the lack of data to precisely model the circuit. For this example, the major problems were in modeling the transformers and transistors. The reactive characteristics of the transformers affect gain, bandwidth, and phase shift; therefore, the transformers affect circuit stability. Transistors T4 and T5 also present problems primarily because they are being operated near cutoff. Transistor current gain is a strong function of collector current at this bias. The manufacturer specification sheets are rarely adequate to model β in this region.

The NET-2 run illustrating the listing and output for the hardened amplifier is given in figure VII-29. This run is included as an example



COEFFICIENT OF COUPLING
BETWEEN EACH COIL PAIR IS
k = 0.9

(a) Transformer TR2



COEFFICIENT OF COUPLING
BETWEEN EACH COIL PAIR IS
k = 0.9

(b) Transformer TR3

Figure VII-26. Transformer Model for the Three Stage Amplifier

TABLE VII-1. COMPARISON OF SPECIFICATIONS FOR THE 2N3054 AND THE 2N5427 TRANSISTORS

	2N3054	2N5427	UNITS
P_D(case)	25	40	W
I_C	4	7	A
V_{CEO}	55	80	V
β_{MIN}	25	30	-
@I_C	0.5	0.5	A
f_{TMIN}	0.8	30	MHz
Cost* (< 100 Units)	0.94	5.96	$

TABLE VII-2. COMPARISON OF SPECIFICATIONS FOR THE 2N5038 AND THE 2N5038 TRANSISTORS

	2N3772	2N5038	UNITS
P_D(case)	150	140	W
I_C	20	20	A
V_{CEO}	60	90	V
β_{MIN}	15	20	-
@ I_C	10	12	A
f_{MIN}	0.2	60	MHz
Cost* (< 100 Units)	3.14-15.50	5.78-13.05	$

*The cost data were taken from the 1974 catalog of a major western distributor of electronic components. The price range shown for the 2N3772 and the 2N5038 indicates the range from standard JEDEC components to JANTX grade components.

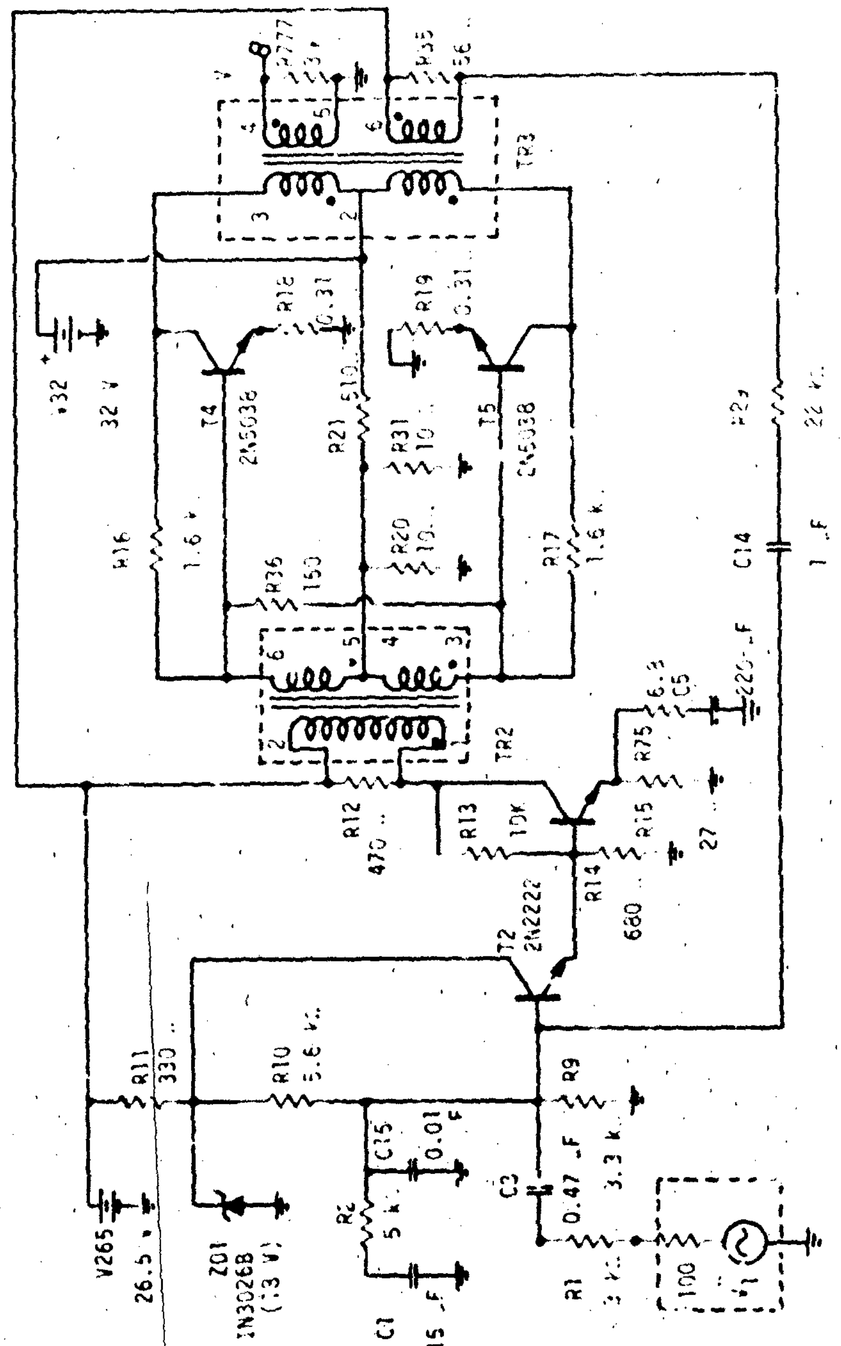


Figure VII-27. Hardened Three Stage Amplifier

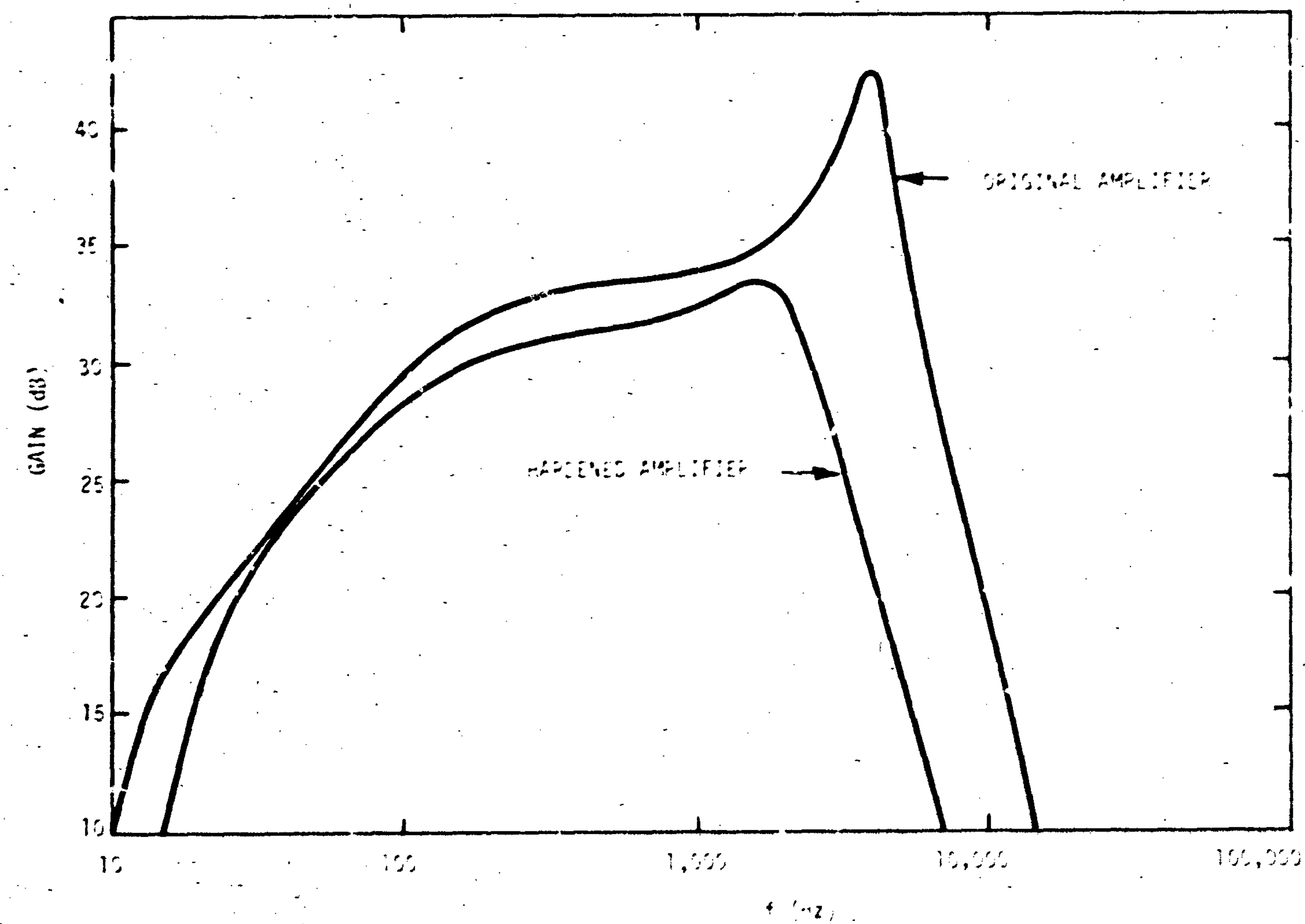


Figure VII-28. Frequency Response of the Three Stage Amplifier

Figure VII-29. NET-2 Listing of Three Stage Amplifier Model

```
[illegible]
FREQ .001
STATE1
STATE2
    TIME 3.
    FREQ 1.E-4 (50*) 1.E-1
    PRINT A1(23-0/25-0) A2(23-0/25-0) Z1(23-0/23-0) Z2(23-0/23-0) [illegible]
IC(T3) [illegible]
    PLOT (LOG3) A1(23-0/25-0) VS FREQ
    PLOT (LNL3) A2(25-0/23-0) VS FREQ
    PLOT (LOG3) Z1(23-0/23-0) VS FREQ
    PLOT (LNL3) Z2(23-0/23-0) VS FREQ
END
```

Figure VII-29. NET-2 Listing of Three Stage Amplifier Model (Continued)

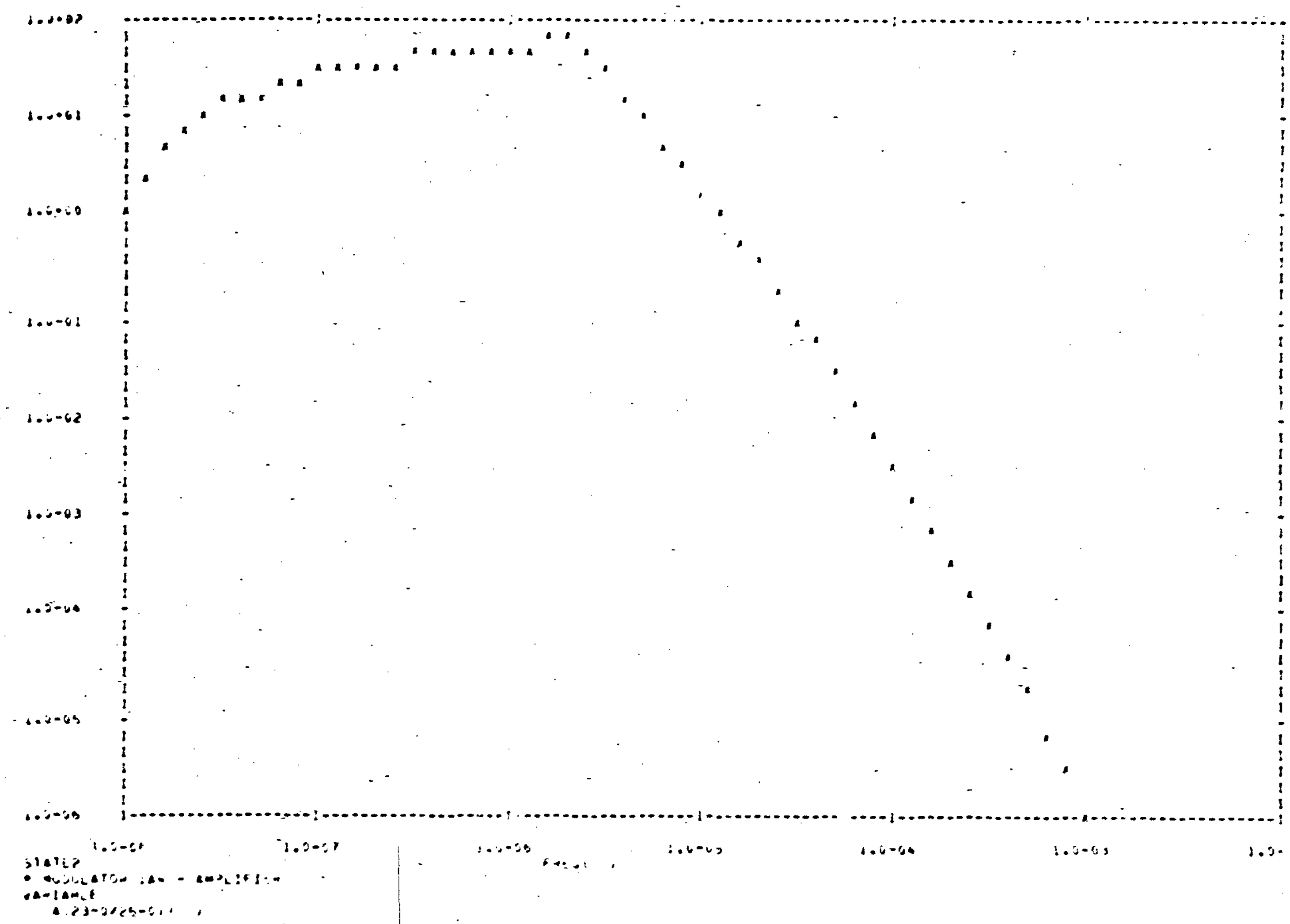


Figure VII-29. NET-2 Listing of Three Stage Amplifier Model (Concluded)

of the use of NET-2 for obtaining the frequency response of complex systems. The plot included in figure VII-29 is the frequency response of the amplifier as determined by NET-2.

E. ANALYSIS OF A LARGE SUBSYSTEM USING SIMPLIFIED AND COMPLETE MODELS

The incorporation of MSI/LSI components in subsystems subject to nuclear weapons effects poses several problems for the radiation effects analyst. The radiation response of the components themselves is quite complex, and the evaluation of the interactions between several such components is often beyond human capabilities. This is especially true when the circuit contains complex feedback paths, a large number of possible states, and nonlinear input and output characteristics.

In this investigation, three MOS integrated circuits of MSI complexity and several small scale integrated circuits were simulated using composite modeling techniques. They include:

(1) RCA CD4051, CMOS, 8-Channel Analog Multiplexer/Demultiplexer
(2) Motorola MC14024, CMOS, 7 Bit, Binary Ripple Counter
(3) Fairchild FS3349, PMOS, Silicon Gate, Hex, 32-bit Shift Register
(4) Harris H4000, CMOS, Dielectrically Isolated NOR Gate
(5) Fairchild μA710 Voltage Comparator

To demonstrate the range of electrical and radiation responses which may be included in a composite model, several of the more interesting aspects of the MC14024 simulation are described below.

The composite models discussed above were developed for use in the analysis of subsystem response. The circuit shown schematically in figure VII-30 was designed specifically to demonstrate the application of the modeling techniques.

The general circuit function is that of an A/D converter. The analog signal used in the conversion is provided by the resistive voltage divider associated with the CD4051A. The divider breaks the 5 V supply voltage into increments connected to the inputs of CD4051 multiplexer channels. Each multiplexer channel can be selected via the CD4051A

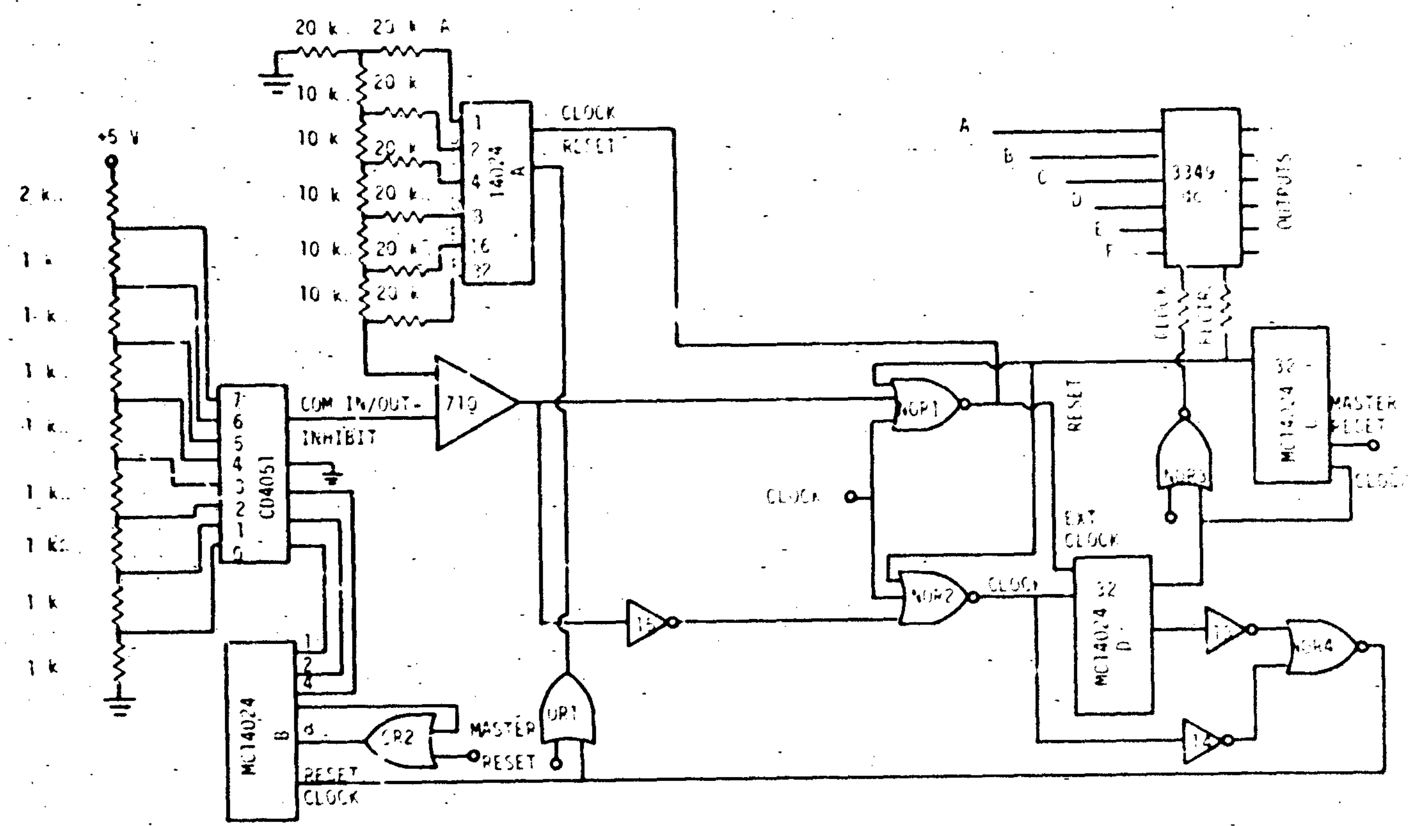


Figure VII-30. 6-Bit A/D Converter with 32-Word Storage

address line so that its input signal appears on the common in/out line. The analog signal appearing on the common in/out serves as the reference for the μA710 voltage comparator.

The conversion sequence for transforming the μA710 reference into a digital signal can best be understood by examining the circuit just after a master reset pulse has occurred. The master reset and the clock are externally applied signals which are brought out to simplify timing when the circuit is tested in a radiation environment. The master reset produces a low state on all outputs of the MC14024 circuits A, B, and C. The MC14024 circuit B is configured as an 8 counter, and drives the address inputs to the CD4051. Initially, channel 0 of the CD4051 is selected and approximately 0.5 V is applied to the reference of the μA710 comparator. The outputs of the MC14024 circuit A are connected to the noninverting input of the comparator through an R-2R resistive network. Since the MC14024 circuit A has been reset, the output of the R-2R network will be essentially ground. The output of the μA710 will be low. Thus, the gate NOR1 is enabled and NOR2 is disabled. With NOR1 enabled, the clock signal is applied to the clock input of MC14024 circuit A. As the MC14024 counts the clock pulses, the voltage output of the R-2R network is incremented. When the output of the R-2R network equals or exceeds the value of the reference signal, the A/D conversion is complete. The comparator output goes high, and the gate NOR1 is disabled while NOR2 is enabled. The outputs of the MC14024 circuit A represent the binary equivalent of the reference signal. The binary number is stored in the 3349DC hex 32-bit shift register. The storage is accomplished by routing one clock pulse via NOR3 into the clock terminal of the 3349DC. A subsequent pulse resets MC14024 circuit A and increments the count on circuit B by 1. As a result, channel 1 is selected for the CD4051, the μA710 output goes low, and the conversion cycle starts again. Note that eight conversion cycles (henceforth called octaves) are required to cover all the multiplexer channels. At the end of the eighth cycle, MC14024 circuit B is reset and the conversion process starts with channel 0 again. The 3349DC can store the results of four octaves. At the end of the fourth

octave, MC14024 circuit C disables the gates NOR1 and NOR2 and activates the recirculate of the 3349DC. The digital results of each conversion can then be examined by providing an external clock to the 3349DC.

Figure VII-31 shows a diagram of the input circuitry and the first two output stages of the MC14024 model. The elements appearing inside the heavy solid line are contained in the model. Elements outside on the line are used to exercise the model. Elements between the heavy solid line and the dashed line model the analog characteristics of the input and output terminals. Elements within the dashed line are included in the LOGIC portion of the model. Thresholding between the analog and LOGIC portions of the model is indicated by dashed interconnections. An abbreviated and annotated version of the SCEPTRE/LOGIC description of the MC14024 model is shown in figure VII-32.

The simplified models for the input circuits (clock and reset) are quite similar. In the case of the clock input, the element JC represents the breakdown characteristics of the input protection network as determined experimentally. The element is implemented with a table which describes the I/V characteristic shown in figure VII-33. The power dissipated in JC as a function of time can be monitored to determine if an electrical overstress pulse will damage the input. The elements CC and RC simulate the normal input impedance of the circuit. The element JPC simulates the photocurrent produced by the input circuitry. It is described by a standard photocurrent equation including both prompt and diffusion components.

The application of the analog clock input to the LOGIC network is interesting since it simulates the 70 percent noise immunity of the clock line. The threshold for transition from low to high is set at 7 volts. The LOGIC flip-flop element, BC, is used to maintain proper clock state until the appropriate transition threshold is reached.

The power supply terminal model also has some unique characteristics. The elements CP, RP, and JP simulate the normal I/V characteristics and the breakdown characteristics of the power supply input in much the same manner as described above. The photoresponse of the terminal

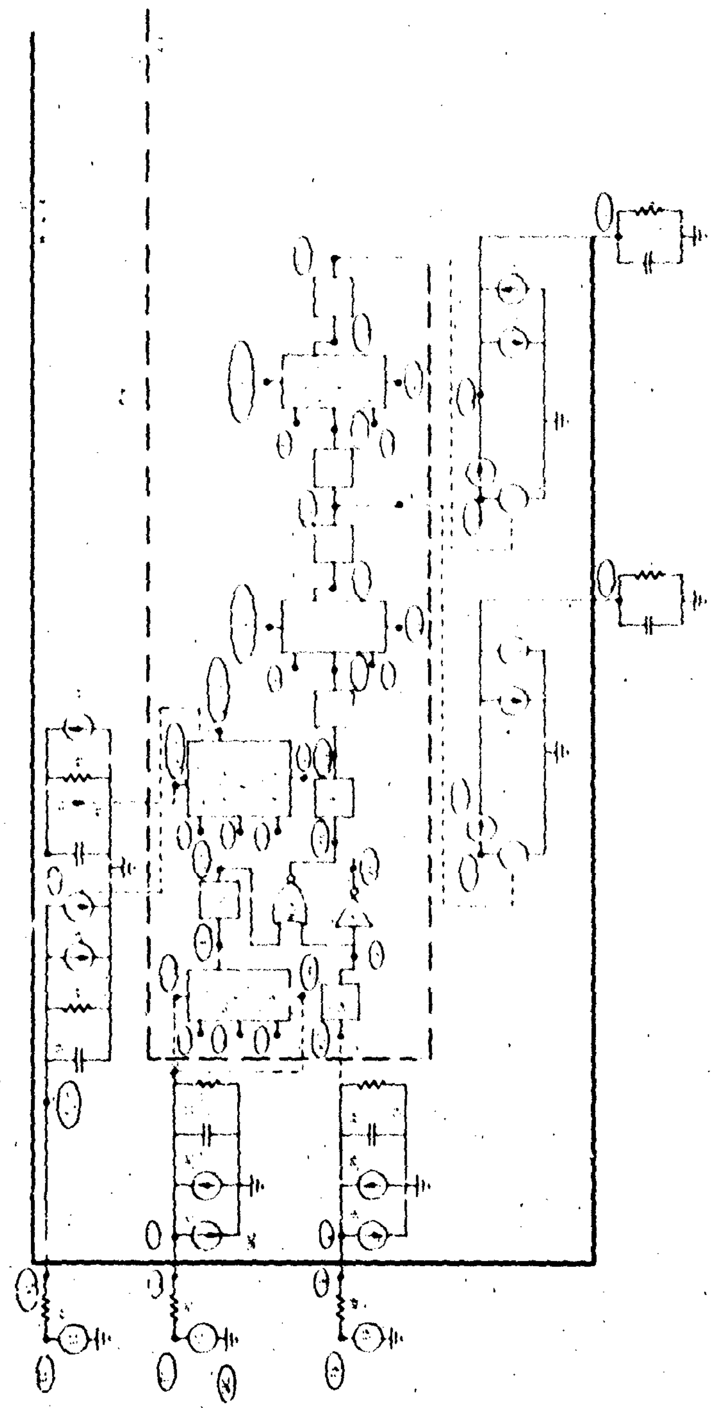


Figure VII-31. MC14024 Composite Model Diagram

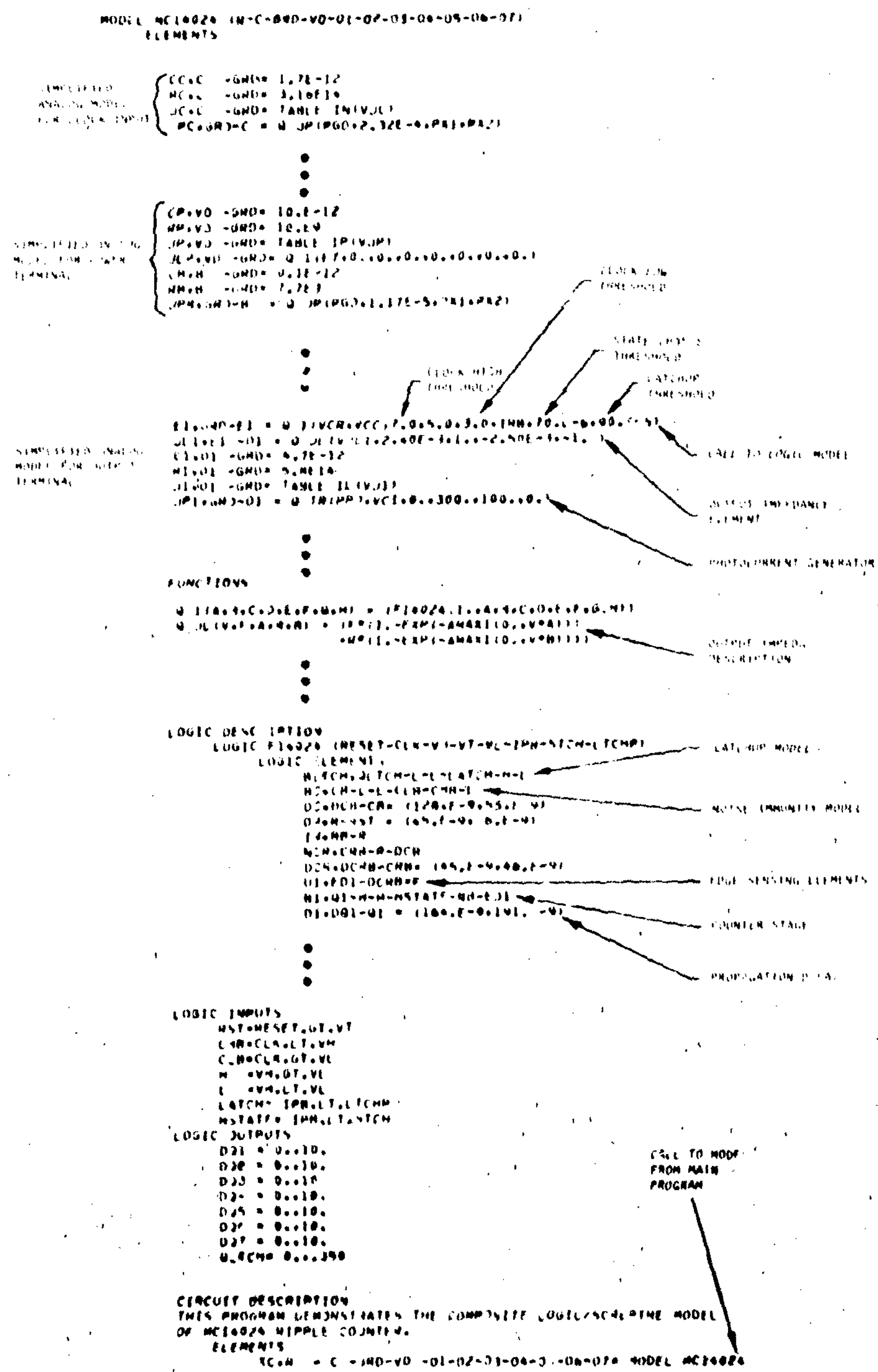


Figure VII-32. Abbreviated MC14024 SCEPTRE/LOGIC Description

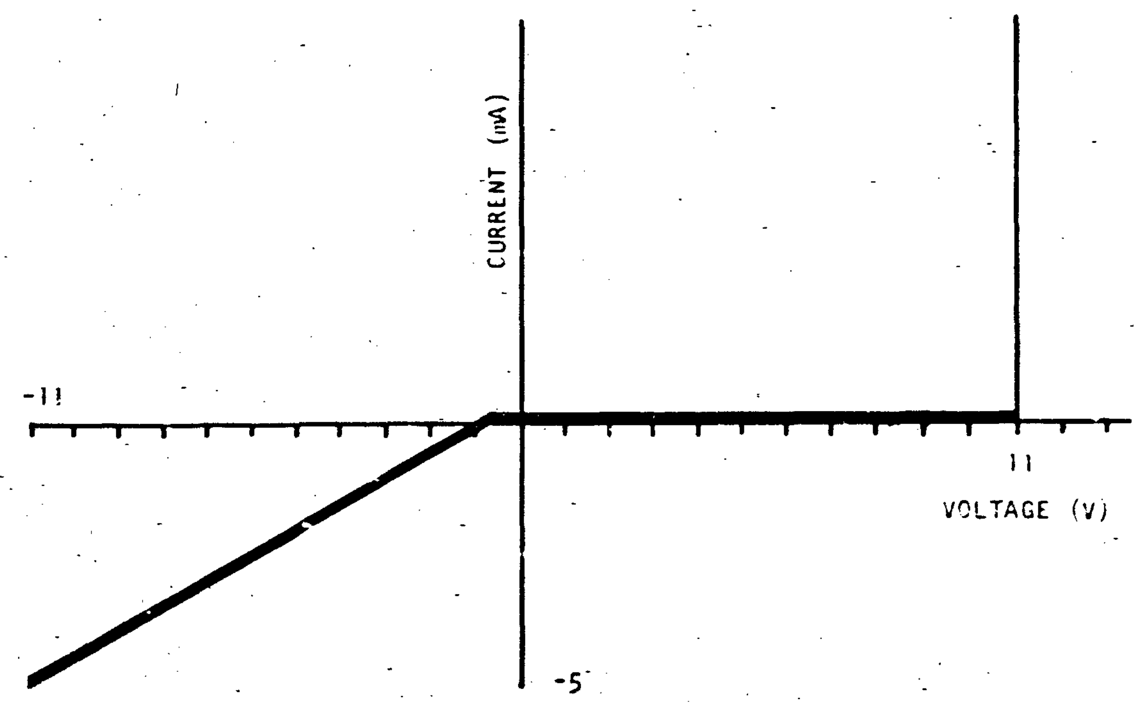


Figure VII-33. Simulated Input Breakdown Characteristic of MC14024

is more complex. The current source JPB is described by a standard photocurrent equation using an effective junction area to give a proper match to experimentally determined terminal photocurrent. The resulting value of current through RB (IRB) is compared against two threshold values to determine the circuit response. If IRB is greater than 70 μA (variable STCH) then the output of all stages are set high. If IRB is greater than 90 μA (variable LTCHP), the LOGIC element BLTCH is triggered. The output of BLTCH controls the value of the analog element JLP, which simulates the high power supply currents drawn when radiation induces a latchup in the MC14024. The existence and characteristics of the latchup in this circuit are simulations of experimental data resulting from flash x-ray and LINAC testing. The arrangement of the power supply simulation correctly models the pulse width and dose rate dependence of the latchup observations.

The output terminal models simulate nonlinear output impedances by applying appropriate voltage for high or low states (10 V or 0 V) to the voltage dependent current source represented by JL1. The current source J1 represents the breakdown characteristics of the output and the current source JP1 represents the output photocurrent response. The photocurrent is of special interest since it is a function of the output voltage. Figure VII-34 is a schematic of the output inverter circuit including the parasitic NPN bipolar transistor and the PN diode associated with the NMOS and PMOS drains respectively. The secondary photocurrent will flow when the voltage drop across the bulk resistance R_B exceeds the output voltage plus a diode drop (.6 V) as indicated in the equation below.

$$I_{SP} = I_{PP} - \frac{V_o + .6}{R_B} \beta$$

where β = parasitic transistor gain. This equation with appropriate limiting conditions is implemented in the current source represented by JP1.

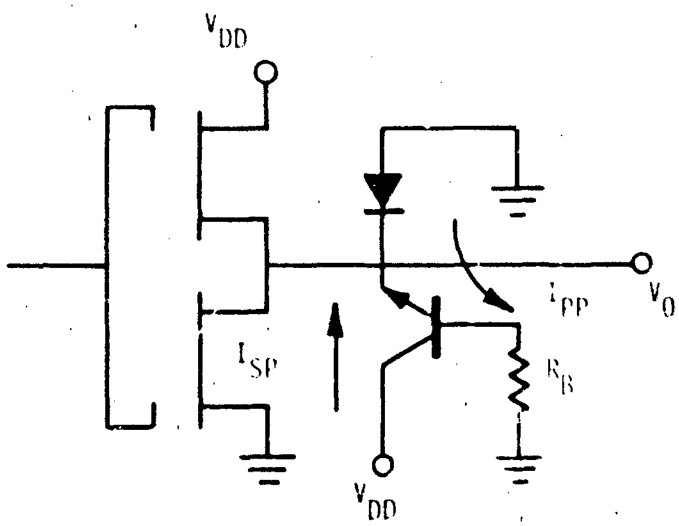


Figure VII-34. CMOS Output Inverter Schemat Showing Parasit

The LOGIC portion of the MC14024 model is a straightforward imple mentation of the circuit schematic. Each counter stage is modeled by a flip-flop with appropriate delay elements to simulate propagation delays. Different values can be utilized for low-to-high and high-to-low transitions. The values for internal delays were developed from detailed analyses of the internal cells. The elements designated as U1, U2, etc., are edge sensing elements which are used to simulate the negative edge trigger response found in the MC14024.

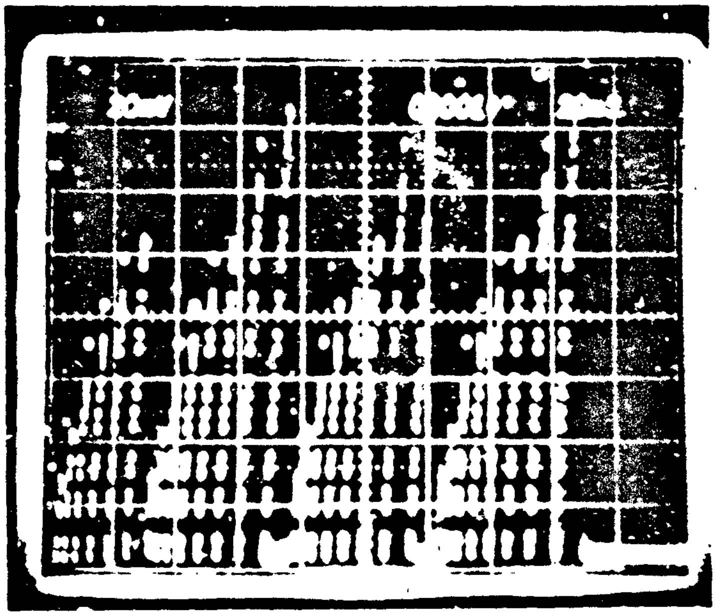
When attempting to simulate a large subsystem incorporating logic elements, there are practical considerations involved in running the problem which should be addressed. One of these involves the selection of a maximum step size. The step size must be small enough to insure the clock waveform is sampled during both its high and low state. This is analogous to the sampling theorem requirement for a sampling rate of twice the highest frequency. In practice, the solutions are better behaved if samples are taken five to six times during the clock period.

The second requirement is brought about by the characteristics of the delay elements. For a LOGIC model with a propagation delay, at least one time step is required to propagate a signal from the input to the

output of the model. Thus, if there is a feedback loop containing multiple LOGIC models, the solution around the loop will not have settled until the number of steps is greater than or equal to the number of LOGIC models in the loop. For example, there are seven models (NOR2, MC14024D, I3, NOR4, MC14024B, CD40S1, and I5) in the longest feedback loop of the A/D converter; thus there should be at least seven time steps for each of the solution points defined by the clock sample requirement (e.g., 7 steps/sample * 5 samples/clock period = 35 steps/clock period). The maximum step size is at most $\frac{\text{clock period}}{35}$.

In the solution of the composite model of the A/D converter, the "Gear" implicit integration routine was used for all runs. The step size for this routine is controlled by the rate of change of electrical signals and the circuit time constants. Since the output state changes are relatively fast and the RC time constants are small, the solution tends to slow down considerably with each state change. The solution time can be significantly decreased if the capacitive elements are removed from nodes experiencing numerous state changes (e.g., the 14024A clock node, the NOR1 output node, and the 14024D clock node). The removal of the capacitance will usually result in a computational delay, but this need not affect solution accuracy if the maximum step size is controlled. The controls based on the propagation delay element requirements mentioned above were generally sufficient to produce accurate solutions in the A/D converter example. For comparison, two solutions were performed for a single conversion octave -- one with capactiances at all nodes and the other with capacitances removed from nodes with frequent state changes. The former required 742 CP (central processor) seconds ($125) and the latter required 335 CP seconds ($57) on the CDC 7600 computer facility at the Air Force Weapons Laboratory.

The subsystem was tested by exposure to a flash x-ray during operation. A photograph of behavior of the subsystem during an x-ray burst is shown in figure VII-35.



VERT:

.5 V/div

HORIZ:

20 ms/div

Figure VII-25. R-2R Network Output

Results of the experimental tests were then compared to a simulated exposure of the subsystem to ionizing radiation. One such simulation is shown in figure VII-36. Initial comparisons revealed significant discrepancies.

Reexamination of the A/D converter model revealed the reason for the discrepancy in the prediction and experimental data. Since the H4000 gates were dielectrically isolated and showed no photoresponse approaching the noise margin of the MC14024 reset, their models were extensively simplified. The analog output consisted of a current source and a parallel fixed value resistance rather than the voltage source and a nonlinear voltage dependent current source discussed earlier in the example model for the MC14024 output. In actuality, the maximum output current of the H4000 devices used in this circuit was 780 μA. When the nonlinear output impedance was simulated correctly, the SCEPTRE/LOGIC analysis provided excellent agreement with the experimental data.

Examination of the results of the composite modeling investigation indicates that the technique is appropriate for analyses of subsystem circuits of significant complexity. The A/D converter required over 2000 electrical and logical elements. The solution times for the models appear long in comparison with some simple discrete component circuits, but the costs are not unreasonable when compared to the cost of breadboarding and testing of circuits containing MSI complexity components. Also, the entire conversion sequence of the model need not be run to investigate a particular time interval and radiation response. The analyst has an advantage of controlling time in the circuit simulation which the experimentalist does not enjoy. Furthermore, the analyst can monitor any node throughout the circuit without modifying the response with a probe connection.

The composite model can incorporate nonlinear input/output impedances which may significantly affect the overall circuit response and lead to results which are unexpected from testing of individual components. The effect of such impedances can be handled in a manual analysis but only with considerable complications in the computations.

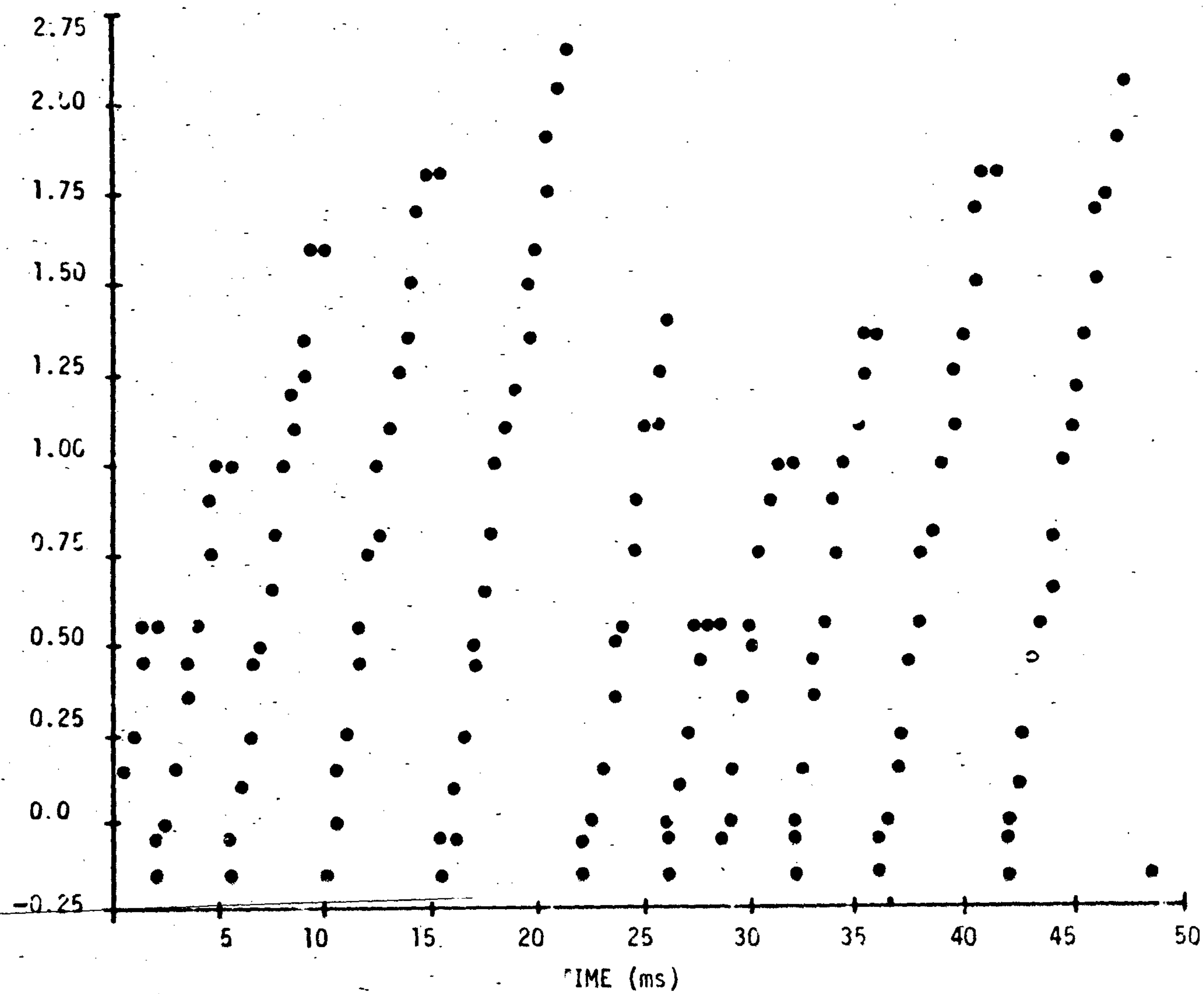


Figure VII-36. Results of Computer Analysis of AD Converter Photoresponse (R-2R Network Output)

The problem with the discrepancy between the initial A/D converter prediction and the experimental results is indicative of the general problem with modeling. The prediction is only as accurate as the simulation on which it is based. While composite modeling does not provide an error-free panacea for subsystem analysis problems, it does provide a formalism which can help the analyst structure an approach to the problem and provide assistance in complex calculations.

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ATTN: Code AT-6

Naval Weapons Support Center
ATTN: Code 20242, J. Munarin
ATTN: Code 7024, J. Ramsey
ATTN: Code 7024, T. Ellis

Office of Naval Research
ATTN: Code 220, D. Lewis
ATTN: Code 427, L. Cooper

Office of the Chief of Naval Operations
ATTN: OP 98 F

Strategic Systems Project Office
Department of the Navy
ATTN: NSP-2015
ATTN: NSP-27331, Spector
ATTN: NSP-2701, J. Pitsenberger
ATTN: NSP-23, D. Gold

DEPARTMENT OF THE AIR FORCE

Air Force Aero Propulsion Laboratory
ATTN: POD, P. Stover

Air Force Avionics Laboratory
ATTN: TEA, R. Conklin
ATTN: DHE, H. Hennecke

Air Force Geophysics Laboratory
ATTN: SULL S-29

Air Force Institute of Technology, Air University
ATTN: ENP, C. Bridgeman

Air Force Materials Laboratory
ATTN: LTE

Air Force Systems Command
ATTN: DLCAM, T. Seale
ATTN: DLW
ATTN: DLCA
ATTN: XRLA, R. Stead

Air Force Technical Applications Center
ATTN: TAE

Air Force Weapons Laboratory
ATTN: A. Loggins
ATTN: M. Knoll
ATTN: J. Ferry
Fcy ATTN: SUL
ATTN: J. Mullis
ATTN: R. Maier
ATTN: R. Simon

DEPARTMENT OF THE AIR FORCE (Continued)

Air Logistics Command
Department of the Air Force
ATTN: MMEDM, S. Mallory
ATTN: MMETH, T. Walter
ATTN: MMETH, R. Padfield
ATTN: MMETM, D. Stanger
ATTN: MMEDD, C. Graham
ATTN: MM, R. Blackburn
ATTN: MMGRW, G. Fry

Electronic Systems Division, AFSC
ATTN: Technical Library

Foreign Technology Division, AFSC
ATTN: TQTD, B. Ballard
ATTN: PDJV

Rome Air Development Center, AFSC
ATTN: RBRP, C. Lane
ATTN: RBRM, J. Brauer

Rome Air Development Center, AFSC
ATTN: ESR, P. Vail
ATTN: ESER, R. Buchanan
ATTN: ESR, W. Shedd
ATTN: ETS, R. Dolan
ATTN: ESE, A. Kahan

Space and Missile Systems Organization, AFSC
ATTN: AWSC
ATTN: AW, W. Schlosser
ATTN: AWSR, W. Blakney
ATTN: DYS, L Darda
ATTN: SKJ, Capt Barry
ATTN: SZJ, R. Davis
ATTN: C. Kelly

Space and Missile Systems Organization, AFSC
ATTN: MNNH, J. Tucker
ATTN: MNNL, S. Kennedy
ATTN: MNNG

Strategic Air Command
ATTN: NRI-STINFO Library
ATTN: XPFS, M. Carra

DEPARTMENT OF ENERGY

Albuquerque Operations Office
ATTN: WSSB/OSD

Department of Energy
ATTN: Office of Military Application
(Classified Library)

OTHER GOVERNMENT AGENCIES

Central Intelligence Agency
ATTN: OSI/RD-5G48 HQ

NASA
Goddard Space Flight Center
ATTN: V. Danchenko
ATTN: J. Adolphsen

NASA
George C. Marshall Space Flight Center
ATTN: L. Hamiter
ATTN: EG02
ATTN: H. Yearwood
ATTN: M. Nowakowski

OTHER GOVERNMENT AGENCIES (Continued)

NASA
ATTN: J. Murphy

NASA
Lewis Research Center
ATTN: M. Saddour

NASA
Ames Research Center
ATTN: G. DeYoung

DEPARTMENT OF ENERGY CONTRACTORS

Lawrence Livermore Laboratory
ATTN: Technical Information Department

Los Alamos Scientific Laboratory
ATTN: J. Freed

Sandia Laboratories
ATTN: E. Coppage
ATTN: W. Dawes
ATTN: J. Hood
ATTN: J. Barnum
ATTN: R. Gregory

DEPARTMENT OF DEFENSE CONTRACTORS

Advanced Microdevices, Inc.
ATTN: J. Schlageter

Advanced Research and Applications Corp.
ATTN: R. Armistead

Aerojet Electro-Systems Co.
ATTN: T. Hanscome

Aerospace Corp.
ATTN: D. Fresh
ATTN: W. Willis
ATTN: S. Bower

Aerospace Industries Assoc. of America, Inc.
ATTN: S. Siegel

Battelle Memorial Institute
ATTN: R. Thatcher

BMD Corp.
ATTN: R. Pease
ATTN: D. Wunch
ATTN: D. Alexander
ATTN. P. Young
ATTN: R. Antinone

Bendix Corp.
ATTN: E. Meeder

Boeing Co.
ATTN: D. Egelkrout

Boeing Co.
ATTN: W. Rumpza
ATTN: I. Arimura
ATTN: C. Rosenberg
ATTN: A. Johnston

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Burr-Brown Research Corp.
ATTN: H. Smith

California Institute of Technology
Jet Propulsion Lab
ATTN: A. Shumka
ATTN: W. Price
ATTN: A. Stanley

Charles Stark Draper Lab, Inc.
ATTN: A. Schutz
ATTN: P. Greiff
ATTN: R. Bedingfield
ATTN: C. Lai
ATTN: R. Ledger

Cincinnati Electronics Corp.
ATTN: L. Hammond
ATTN: C. Stump

Control Data Corp.
ATTN: J. Meehan

University of Colorado
ATTN. Sec. Officer for T. Venditti

E-Systems, Inc.
ATTN: K. Reis

Electronic Industries Association
ATTN: J. Hessman

EMM Corp.
ATTN: F. Krch

Exp. and Math. Physics Consultants
ATTN: T. Jordan

Fairchild Camera and Instrument Corp.
ATTN: D. Myers
ATTN: R. Marshall

Ford Aerospace and Communications Corp.
ATTN: Technical Information Services
ATTN: J. Davison

Ford Aerospace and Communications Corp.
ATTN: D. Cadle

Franklin Institute
ATTN: R. Thompson

Garrett Corp.
ATTN: R. Weir

General Dynamics Corp.
ATTN: W. Hanson

General Dynamics Corp.
ATTN: R. Fields
ATTN: O. Wood

General Electric Co.
ATTN: R. Casey
ATTN: J. Peden
ATTN: L. Sivo
ATTN: D. Long

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

General Electric Co.
Re-entry and Environmental Systems Div.
ATTN: Technical Library
ATTN: R. Benedict
ATTN: W. Patterson
ATTN: J. Palchefsky, Jr.

General Electric Co.
Ordnance Systems
ATTN: J. Reidl

General Electric Co.
Aircraft Engine Business Group
ATTN: R. Helien

General Electric Co.
Aerospace Electronics Systems
ATTN: W. Patterson
ATTN: D. Cole
ATTN: J. Gibson

General Electric Co.
ATTN: D. Pepin

General Electric Company—TEMPO
Center for Advanced Studies
ATTN: DASIAC
ATTN: M. Espic

General Electric Company—TEMPO
Alexandria Office
ATTN: DASIAC

General Research Corp.
ATTN: Technical Information Office
ATTN: R. Hill

Georgia Institute of Technology
ATTN: R. Curry

Georgia Institute of Technology
Office of Contract Administration
ATTN: H. Denny

Goodyear Aerospace Corp.
ATTN: Security Control Station

Grumman Aerospace Corp.
ATTN: J. Rogers

GTE Sylvania, Inc.
Electronics Systems Grp-Eastern Div.
ATTN: C. Thornhill
ATTN: L. Pauples
ATTN: L. Blaisdell

GTE Sylvania, Inc.
ATTN: J. Waldron
ATTN: H and V Group
ATTN: H. Ullman
ATTN: P. Fredrickson

Harris Corp.
ATTN: J. Cornell
ATTN: C. Anderson

Honeywell, Inc.
ATTN: R. Gumm

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Honeywell, Inc.
Avionics Division
ATTN: C. Cerulli

Honeywell, Inc.
Radiation Center
ATTN: Technical Library

Honeywell, Inc.
Defense Systems Division
ATTN: K. Gaspard

Hughes Aircraft Co.
ATTN: R. McGowan
ATTN: J. Singletary

Hughes Aircraft Co.
El Segundo Site
ATTN: E. Smith
ATTN: W. Scott

IBM Corp.
ATTN: H. Mathers
ATTN: T. Martin
ATTN: F. Fietse

IIT Research Institute
ATTN: I. Mindel

Institute for Defense Analyses
ATTN: Technical Information Services

Intel Corp.
ATTN: M. Jordan

IBM Corp.
Thomas Watson Research Center
ATTN: J. Ziegler

International Tel. and Telegraph Corp.
ATTN: Dept. 608
ATTN: A. Richardson

Intersil Inc.
ATTN: D. MacDonald

IRT Corp
ATTN: J. Harrity

JAYCOR
ATTN: L. Scott

Johns Hopkins University
ATTN: P. Partridge

Kaman Sciences Corp.
ATTN: J. Lubell

Litton Systems, Inc.
ATTN: G. Maddox

Lockheed Missiles and Space Co., Inc.
ATTN: F. Smith
ATTN: P. Bene
ATTN: H. Phillips
ATTN: C. Thompson

Lockheed Missiles and Space Co., Inc.
ATTN: J. Crowley
ATTN: J. Smith

M.I.T. Lincoln Lab
ATTN: P. McKenzie

Martin Marietta Corp.
Orlando Division
ATTN: H. Cates
ATTN: W. Janocko
ATTN: W. Brockett
ATTN: R. Gaynor

Martin Marietta Corp.
Denver Division
ATTN: E. Carter

McDonnell Douglas Corp.
ATTN: Library
ATTN: D. Dohm
ATTN: M. Stitch

McDonnell Douglas Corp.
ATTN: J. Holmgrem
ATTN: D. Fitzgerald

McDonnell Douglas Corp.
ATTN: Technical Library

Mission Research Corp.
ATTN: C. Longmire

Mission Research Corp.—San Diego
ATTN: J. Raymond
ATTN: R. [illegible]rger
ATTN: J. Azarewicz
ATTN: V. Va[illegible] Lint

Mitre Corp.
ATTN: M. Fitzgerald

Motorola, Inc
Government Electronics Division
ATTN: A. Christensen

Motorola, Inc.
Semiconductor Group
ATTN: J. Clark

National Academy of Sciences
ATTN: R. Shane

National Semiconductor Corp.
ATTN: R. Wang
ATTN: A. London

University of New Mexico
Electrical Engineering and Computer Science Dept.
ATTN: H. Southward

Northrop Corp.
Northrop Research and Technology Ctr.
ATTN: P. Eisenberg
ATTN: T. Jackson
ATTN: J. Spour

Northrop Corp.
Electronic Division
ATTN: L. Apodaca
ATTN: P. Gardner
ATTN: D. Strobel

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Physics International Co.
ATTN: Division 6000
ATTN: J. Shea
ATTN: J. Huntington

R&D Associates
ATTN: R. Poll
ATTN: C. MacDonald
ATTN: S. Rogers

Rand Corp.
ATTN: C. Crain

Raytheon Co.
ATTN: J. Ciccio

Raytheon Co.
ATTN: A. Van Doren
ATTN: H. Flescher

RCA Corp.
Government Systems Division
ATTN: G. Brucker
ATTN: V. Mancino

RCA Corp.
David Sarnoff Research Center
ATTN: D. O'Connor
ATTN: Office N103

RCA Corp.
Government Systems Division
Missile and Surface Radar
ATTN: R. Killion

RCA Corp.
Camden Complex
ATTN: J. Saultz
ATTN: E. Van Keuren

RCA Corp.
Somerville Plant, Solid State Div.
ATTN: W. Allen

Renssalaer Polytechnic Institute
ATTN: R. Gutmann

Research Triangle Institute
ATTN: M. Simons, Jr.

Rockwell International Corp.
ATTN: J. Bell
ATTN: V. De Martino
ATTN: G. Messenger
ATTN: V. Strahan
ATTN: T. Oki

Rockwell International Corp.
Space Division
ATTN: D. Stevens

Rockwell International Corp.
ATTN: TIC BA08
ATTN: T. Yates

Sanders Associates, Inc.
ATTN: M. Aitel
ATTN: L. Brodeur

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Science Applications, Inc.
ATTN: V. Verbinski
ATTN: J. Naber
ATTN: V. Ophan

Science Applications, Inc.
ATTN: W. Chadsey

Science Applications, Inc.
ATTN: D. Stribling

Singer Co.
ATTN: J. Brinkman

Singer Co.
Data Systems
ATTN: R. Spiegel

Sperry Rand Corp.
Sperry Microwave Electronics
ATTN: Engineering Laboratory

Sperry Rand Corp.
Sperry Division
ATTN: R. Viola
ATTN: C. Craig
ATTN: P. Maraffino
ATTN: [illegible]. Scaravaglione

Sperry Rand Corp.
Sperry Flight Systems
ATTN: D. Schow

Sperry Univac
ATTN: J. Inda

Spire Corp.
ATTN: R. Little

SRI International
ATTN: A. Whitson
ATTN: P. Dolan

DEPARTMENT OF DEFENSE CONTRACTORS (Continued)

Teledyne Ryan Aeronautical
ATTN: J. Rawlings

Texas Instruments, Inc.
ATTN: A. Peletier
ATTN: R. Stehlin

TRW Defense and Space Sys. Group
ATTN: H. Haid
ATTN: P. Guilfoyle
ATTN: O. Adams
ATTN: R. Kingsland
ATTN: A. Pavelko
ATTN: H. Holloway
ATTN: R. Schnieder
ATTN: A. Witteles

TRW Defense and Space Sys. Group
San Bernardino Operations
ATTN: F. Fay
ATTN: M. Gorman
ATTN: R. Kitter

TRW Systems and Energy
ATTN: G. Spehar
ATTN: D. Millward

Vought Corp
ATTN: R. Tomme
ATTN: Library
ATTN: Technical Data Center

Westinghouse Electric Co.
Aerospace and Electronic Systems Div
ATTN: L. McPherson

Westinghouse Electric Corp.
Defense and Electronic Systems Ctr.
ATTN: H. Kalapaca
ATTN: D. Crichi